The Impact of Inverse Narrow Width Effect on Sub-threshold Device Sizing

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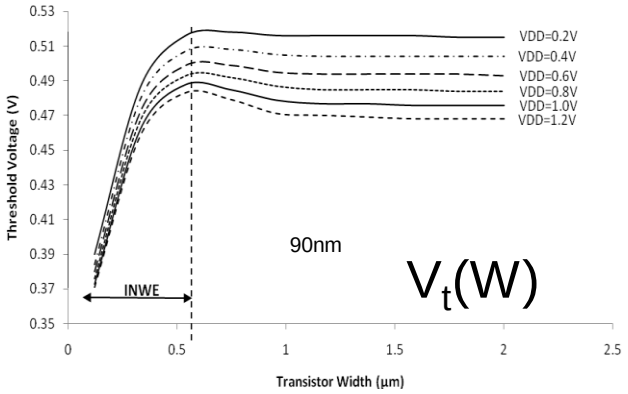
Overview

- Inverse narrow width effect (INWE)
- Transistor sizing at sub-threshold region
- INWE-based sizing in logic cell libraries
- Effect on functional yield
- Test design; power and area results
- Conclusions

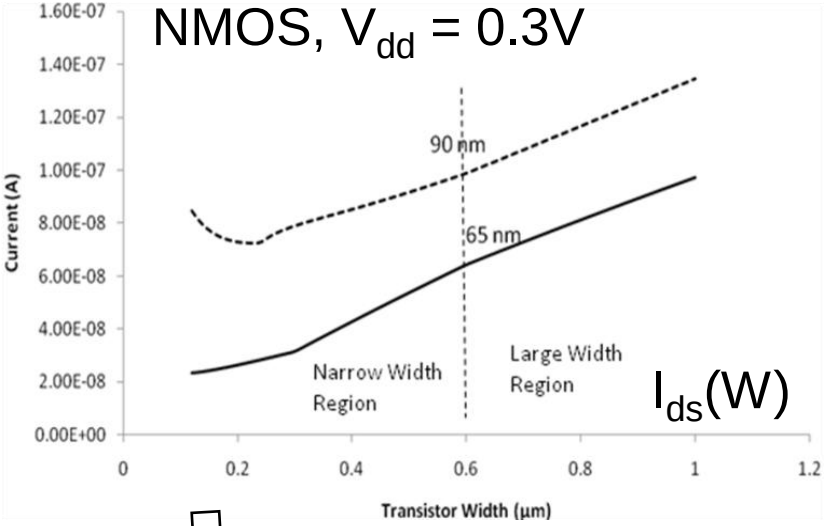
Inverse Narrow Width Effect

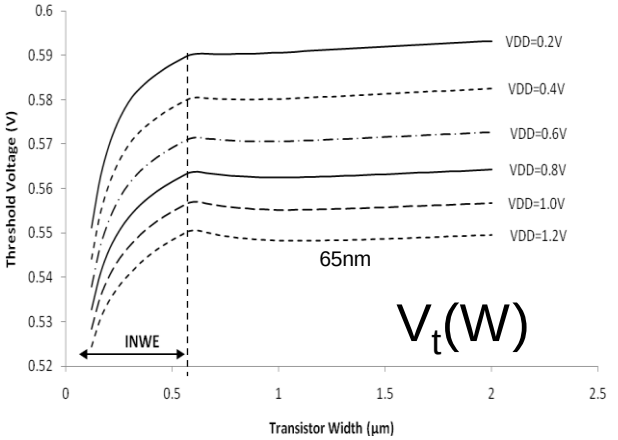


- Lower threshold voltage at small width due to Shallow Trench Isolation
- Ids(W) is non-linear!

Sub-threshold Current Equation:

$$I = I_0 \frac{W}{L} e^{\frac{V_{GS} - V_t}{mV_T}} (1 - e^{-\frac{V_{DS}}{V_T}})$$





Different transistor sizing story in sub-threshold region for optimal speed, power, and silicon variation!

Transistor Sizing at Sub-Threshold

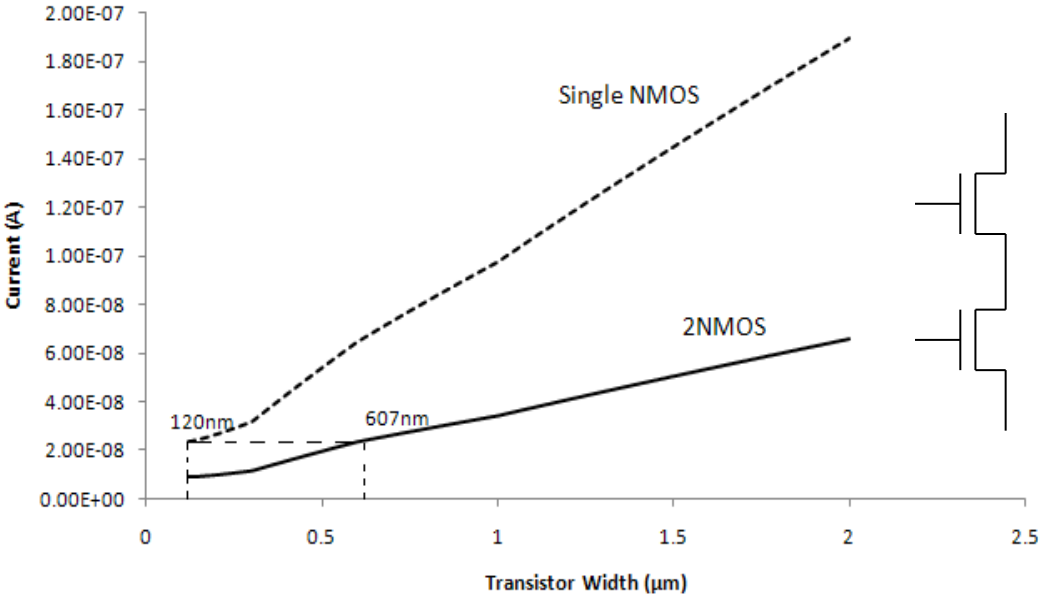
- Transistor sizing for sub-threshold logic (e.g. 0.3V)
  - PMOS and NMOS currents should be **equal**, because of:
    - high performance
    - low power consumption
    - high functional yield
  - We want to **minimize W** and L for low power operation
    - non-linear relation between transistor current and width
    - threshold voltage lower at small W
      (true at least in 90nm, 65nm, 45nm technologies)
  - **Imbalance** in PMOS and NMOS currents
    - especially apparent in sub-threshold operation

Transistor Sizes in Stacks

- Transistor width when stacking **two** transistors
  - In super-threshold: x *2*
  - In sub-threshold: x (*1*+*α*) (Kwong: $\alpha = e^{\frac{-\lambda_d V_{dd}}{m V_T}}$)
  - With INWE added: x (*1*+*α*)$e^{\Delta V_t / m V_T}$

- Example 65nm

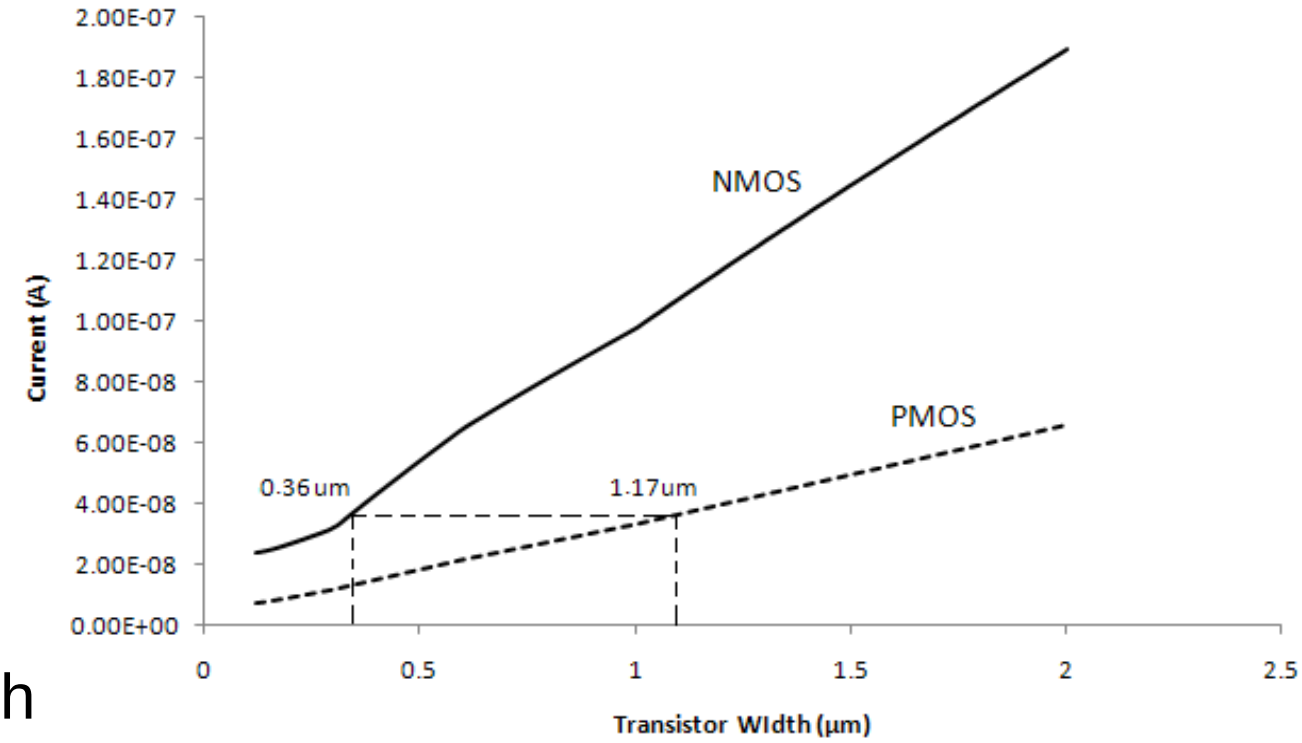
  (W_{min} = 0.12µm, V_{dd} = 0.3V)
  - W_{stack} = **5** x W_{single}



Wp/Wn Width Ratio in Sub-Threshold

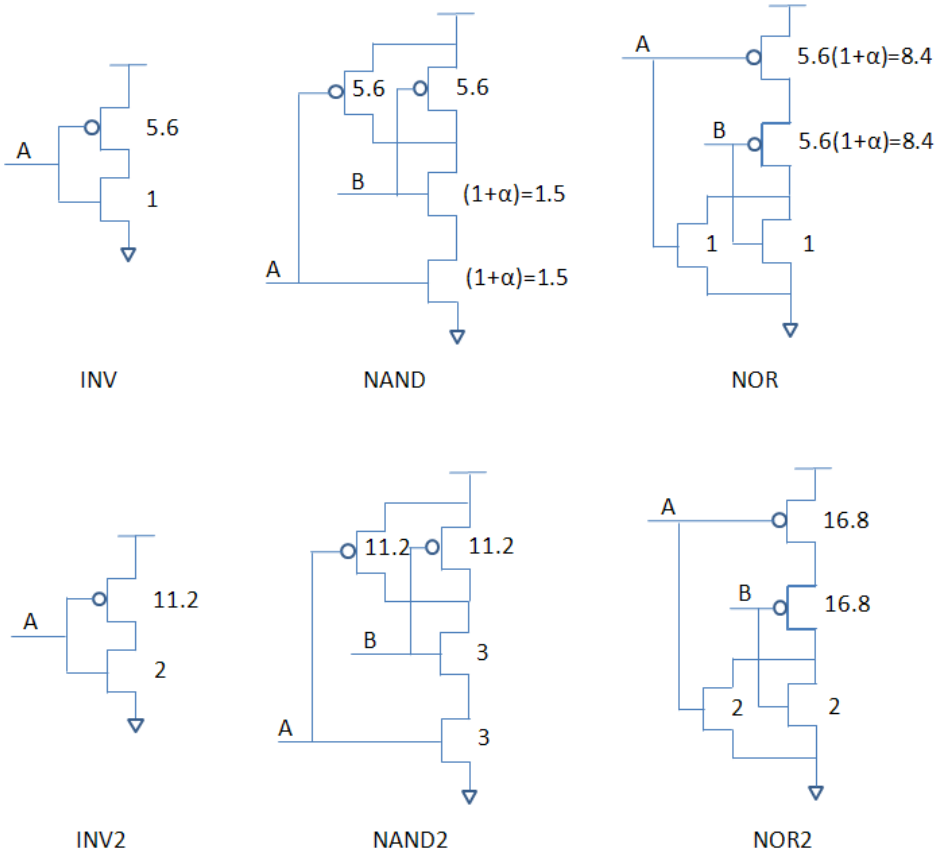
- 180nm: W_p/W_n = **12** fixed (Calhoun) → large area
- 65nm: W_p/W_n = **3.25** (example) → small area

- Small ratio
  (at V_{dd} = 0.3V)
  - small area
  - low power
- Ratio varies
  - drive strength

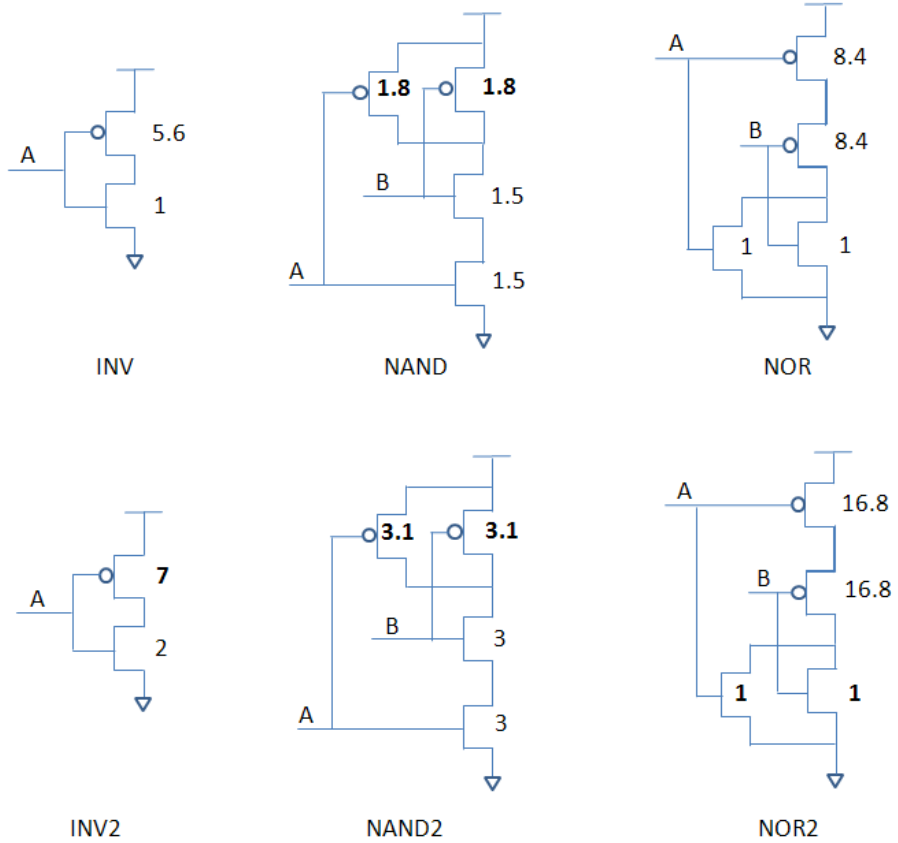


Sub-Threshold Sizing in Cell Library

- Without considering INWE
  - normalized to W_{min} = 0.12µm



- Taking INWE into account
  - normalized to W_{min} = 0.12µm



Experimental Results

- INWE-based method versus conventional method
  - Technology 65nm, V_{dd} = 0.3V, W_{min} = 0.12µm
  - Fanout = 4

Logic gate	Delay reduction	PD Product reduction	Area reduction
INV	0%	0%	0%
NAND	30%	68%	53%
NOR	0%	0%	0%
INV2	18%	43%	39%
NAND2	35%	73%	57%
NOR2	1.5%	6.0%	5.3%

Effect on Delay Chain

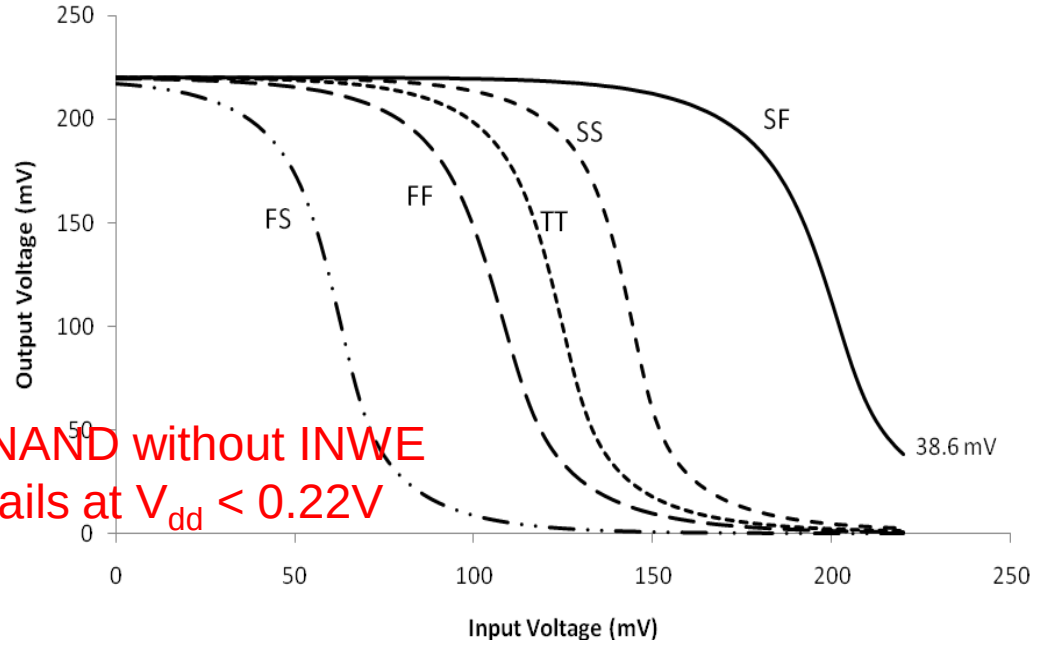
- 10-Stage delay chain
  - One cell = INV2 + NAND2 + NOR2
  - V_{dd} = 0.3V

Sizing	Delay (µs)	Power (nW)	PDP (fJ)
Without INWE	3.2	3.8	12.2
Proposed sizing	2.8	3.0	8.4

  - Power-delay product improvement: **30%**

Effect on Functional Yield

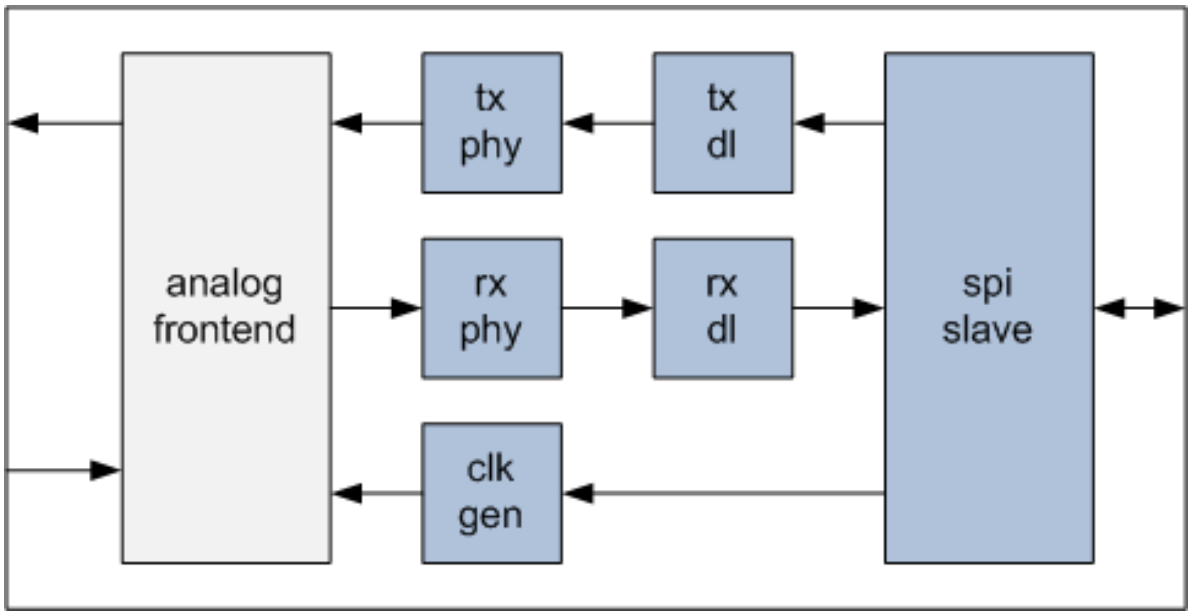
- Better symmetry in PMOS and NMOS currents
  - Allows for lower supply voltage
    - e.g. 0.22V instead of 0.24V when considering INWE
      - → 1 – (0.22/0.24)^2 = **16%** less dynamic power dissipation



	Without considering INWE	With INWE taken into account
INV	0.21	0.21
NAND	0.24	0.22
NOR	0.21	0.21
INV2	0.20	0.19
NAND2	0.22	0.20
NOR2	0.20	0.20

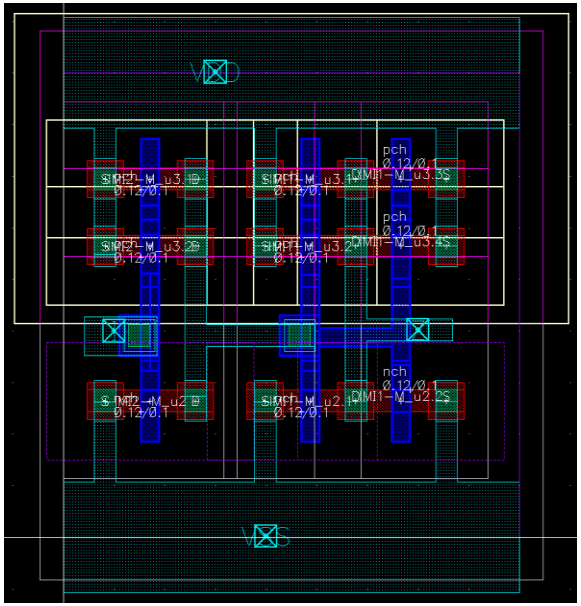
Test Design

- Narrow Band radio digital baseband design
  - 90nm CMOS
  - Low clock frequency 6MHz
  - No SRAM
  - ~50 kgates
  - V_{dd} = 0.4V
  - SVT



INWE-Based Sub-Threshold Cell Library

- Basic cells
  - ND2, NR2, INV, AOI222, IOA22, AO22, MUX, XOR2, DFCNQX1, DFSNQX1, DFX1, DEL0, DEL4, BUFF, BUFFX1, BUFFX2, LHCNX1, LevelShifter, ClockGate
- Supply voltage
  - 0.3V ... 1.2V
- Minimum length and width
  - W = 120nm
  - L = 90nm



Power and Area Results

- Total power reduction by factor **9x** at 0.4V

Power	Current design (1.2V)	Sub-threshold design (0.4V)
Active Power	234 µW	26.0 µW
Leakage Power	3.0 µW	0.7 µW
Total Power	**237 µW**	**26.7 µW**

- Area increases marginally by 1.2x due to limited number of standard cells in the library

Current design (mm^2)	Sub-threshold design (mm^2)
0.36	0.43

Conclusions

- Inverse Narrow Width Effect (INWE) affects threshold voltage
- Must take this into account when sizing transistors to balance rise and fall delays in sub-threshold, especially when using minimum transistor sizes
- Strong positive effect on performance, power, and functional yield
  - 73% reduction in power-delay product (NAND cell)
  - 8% lower supply voltage possible for same yield
  - 9x power reduction on test design (NB digital baseband)
    - just V_{dd} scaling, but achieving 6MHz at 0.4V in 90nm