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Vertical Interconnects Squeezing in Symmetric 3D Mesh Network-on-Chip

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Outline

- Background
- Motivation
- TSV Squeezing Scheme
- Experiments
- Conclusion

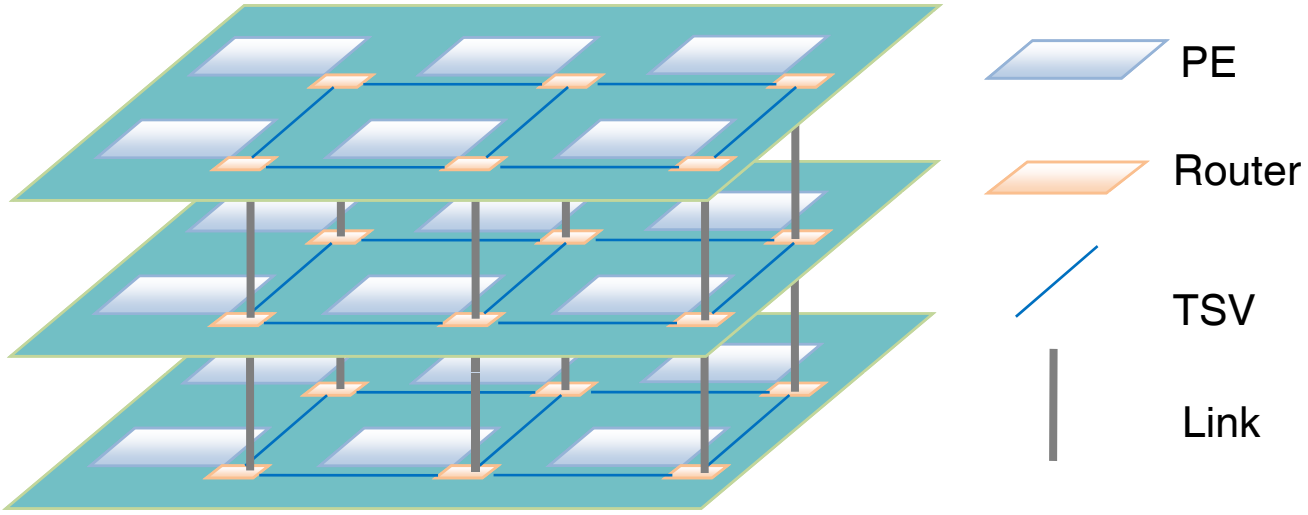
Background

- 3D Technique
  - Low latency
  - Heterogeneous integration
  - Manufacture challenge
- Network-on-Chip
  - High bandwidth
  - Excellent scalability
  - Large p2p latency

- 3D Network-on-Chip
  - High bandwidth
  - Excellent scalability
  - Manufacture challenge
  - Low latency
  - Heterogeneous integration

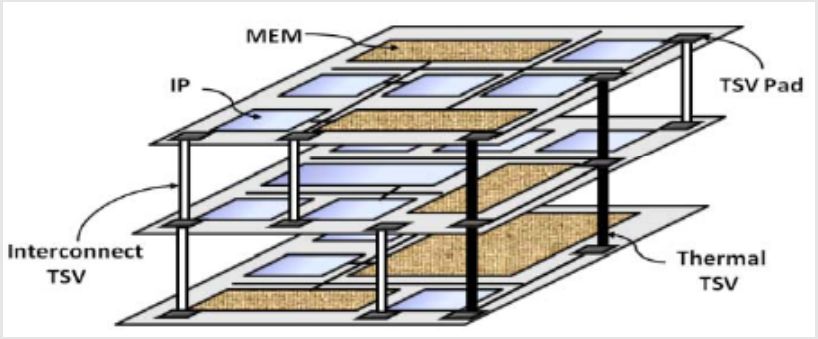
3D Network-on-Chip

- 3D Mesh-bus hybrid architecture
- True 3D fabric architecture
- 3D symmetric architecture

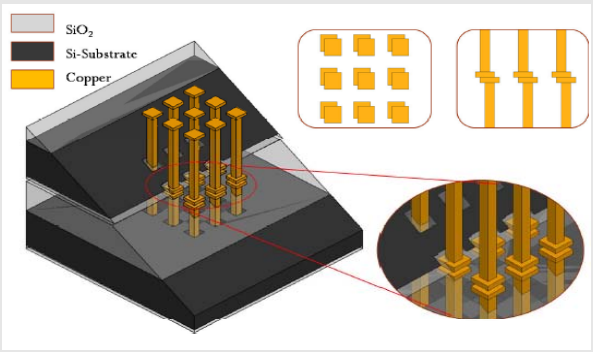


3D IC Manufacture Challenges

3D IC *DAC09*



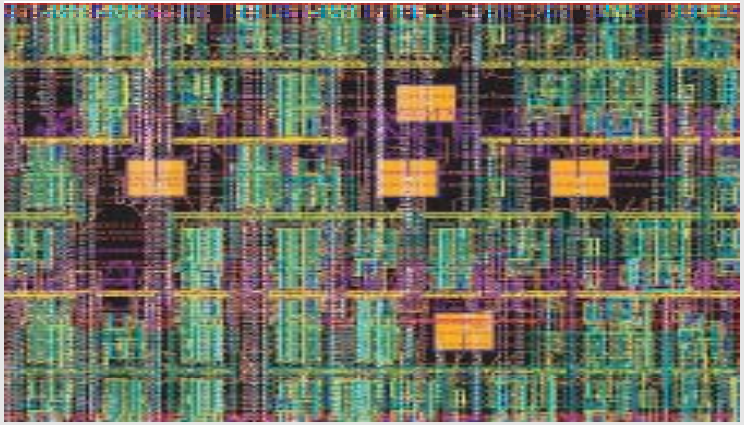
Reliability challenge *ICCAD08*



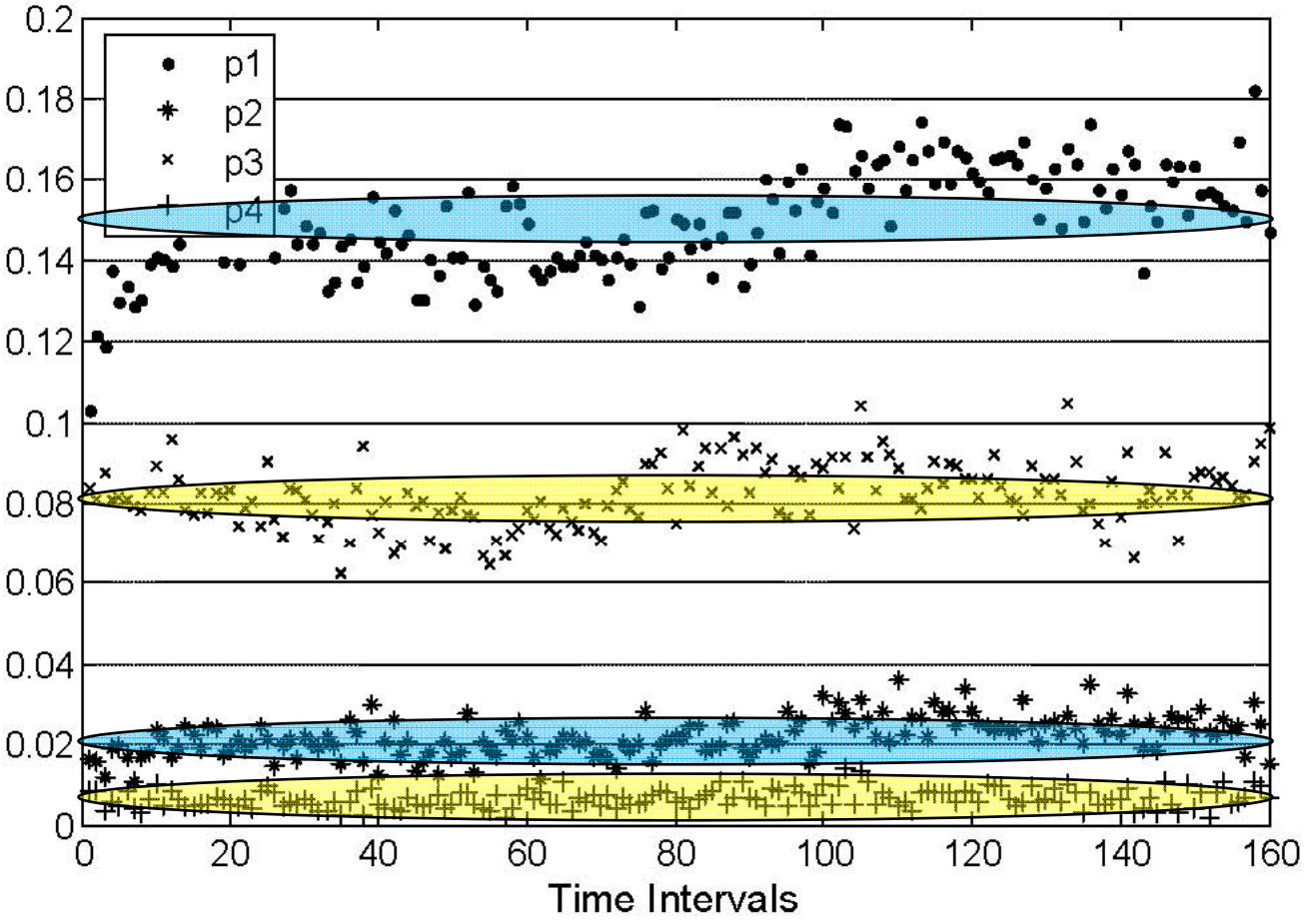
Chip area challenge *ITRS09*

	TSV for 3D-SOC	TSV for 3D-SIC	Transistor Size
2009	TSV pitch 8-16um	TSV pitch 2-4um	ASIC M1 0.054um
2015	TSV pitch 4-8um	TSV pitch 1.6-3.0um	ASIC M1 0.021um

Routing congestion *SLIP09*



Observation



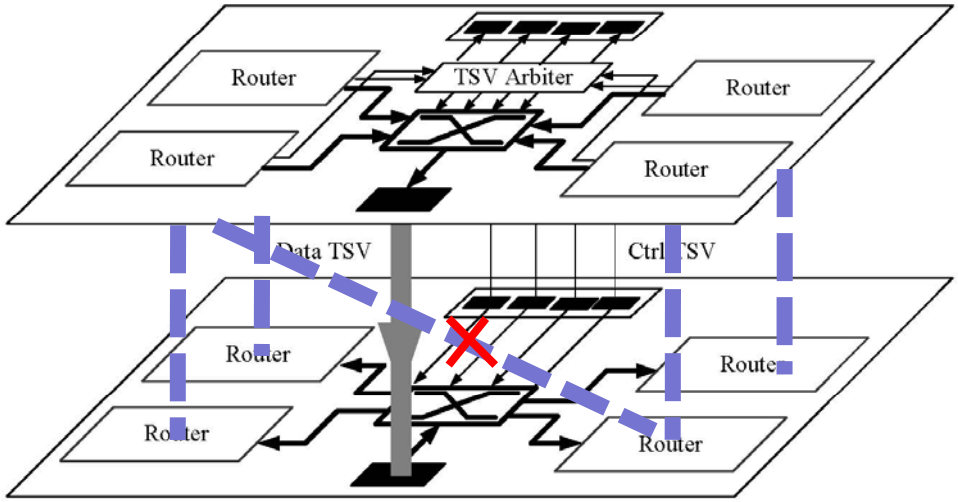
TSV utilization = **0.15** when load = 0.3

TSV utilization = **0.08** when load = 0.1

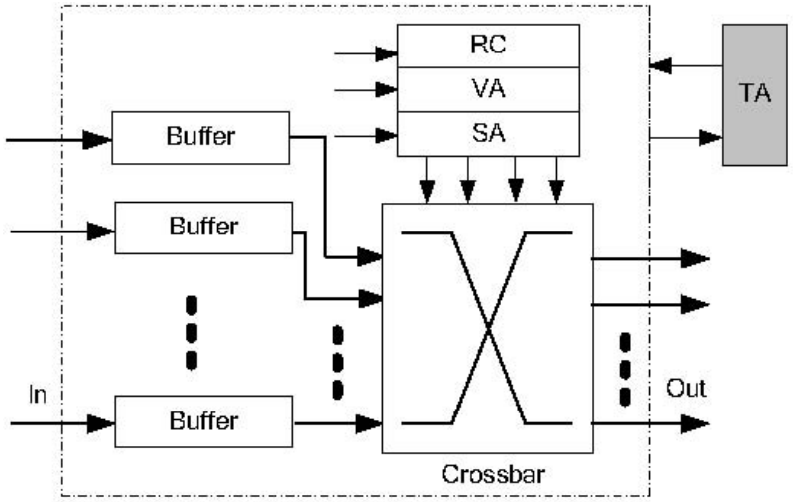
TSV confliction = **0.02** when load = 0.3

TSV confliction = **0.01** when load = 0.1

TSV Squeezing Scheme

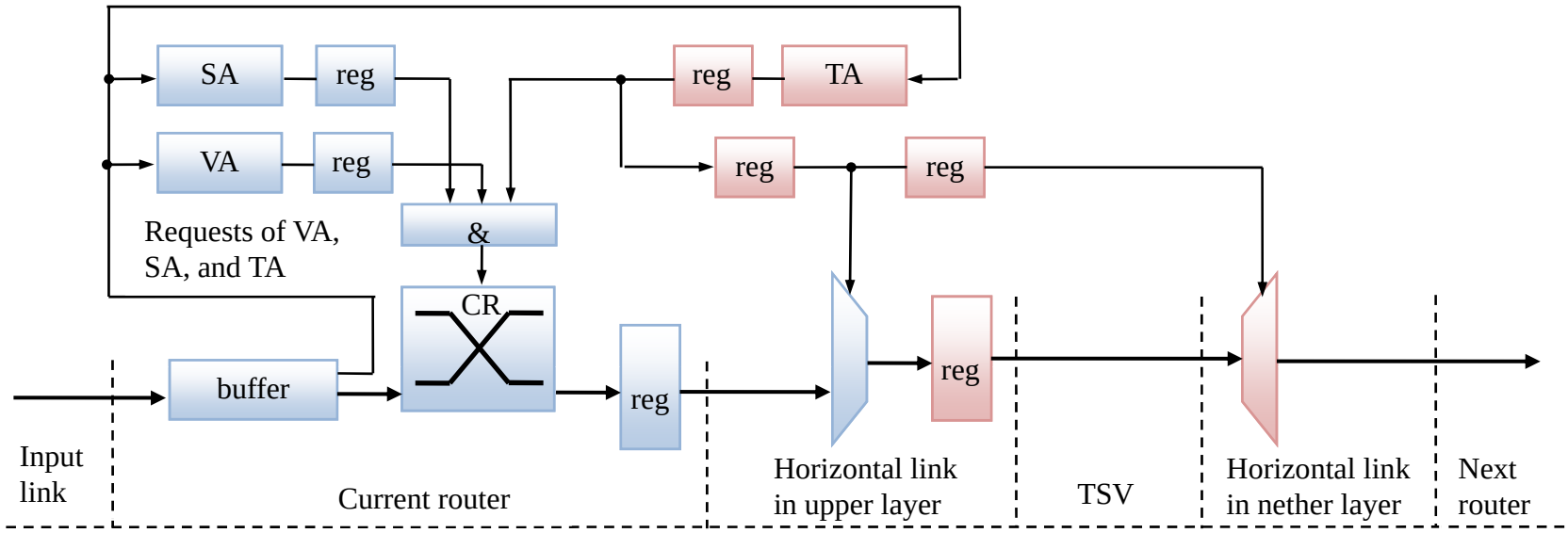


Squeezing Scheme with 4:1

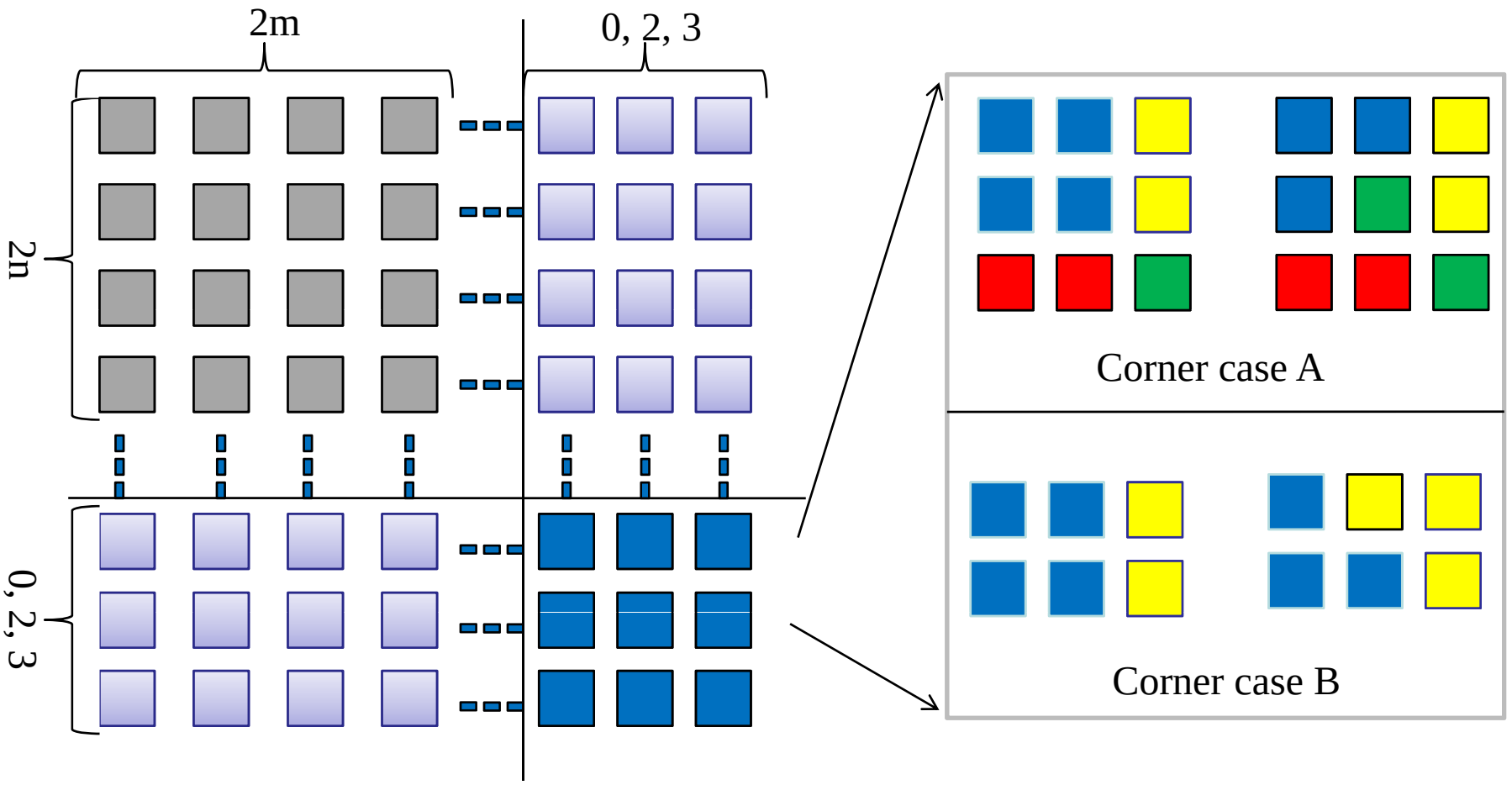


Router Modification

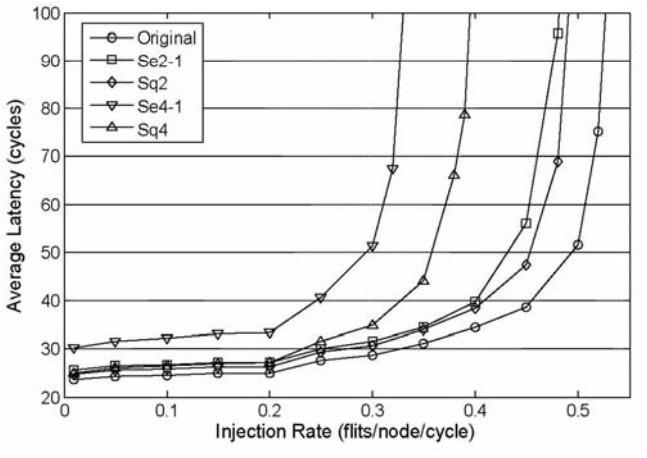
Router Microarchitecture



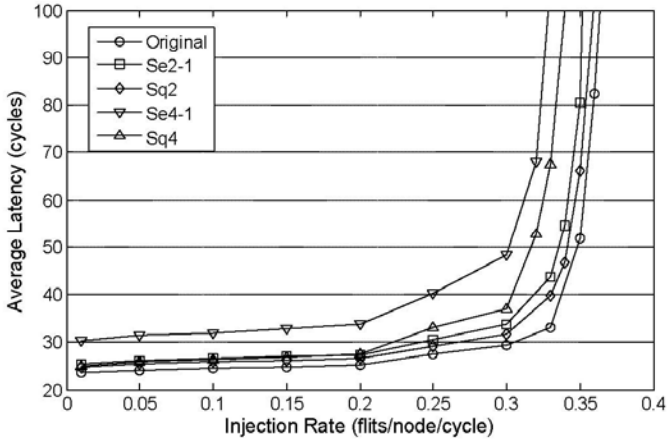
NoC Organization for TSV Squeezing



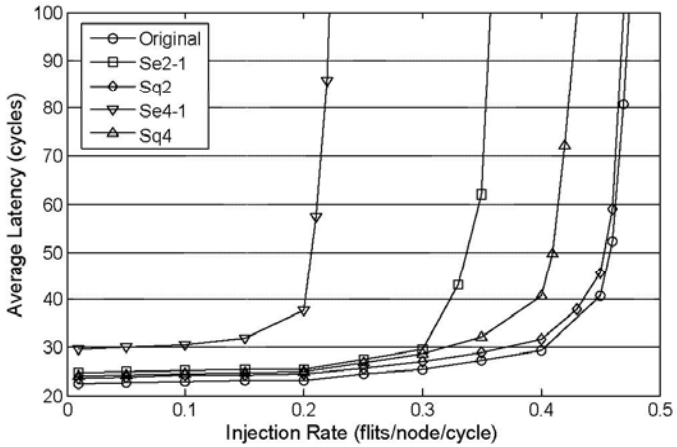
Experiments



a) Uniform



b) Shuffle



c) Hotspot

Experiment set up

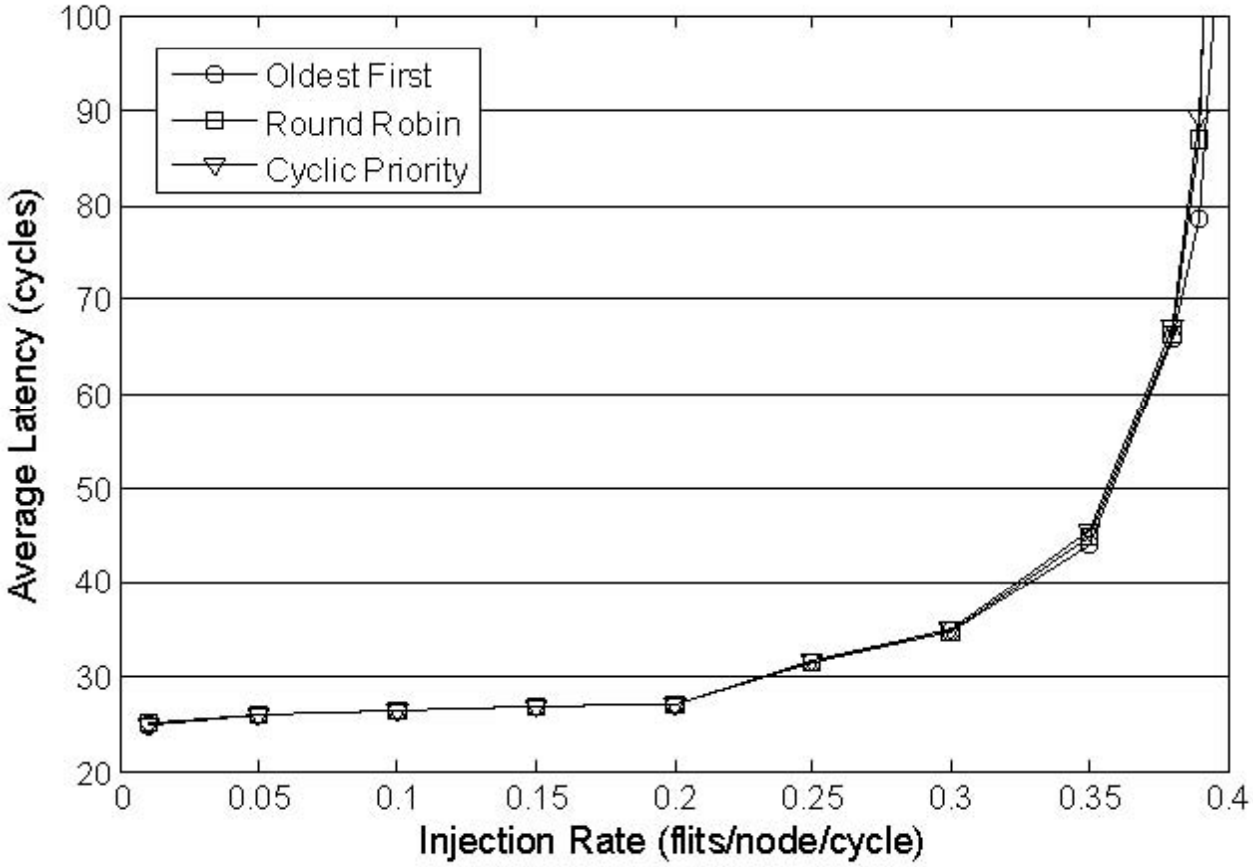
Topology: 4x4x2 Mesh

Buffer: 2VC x 8flits per port

Router: Two-staged Pipeline

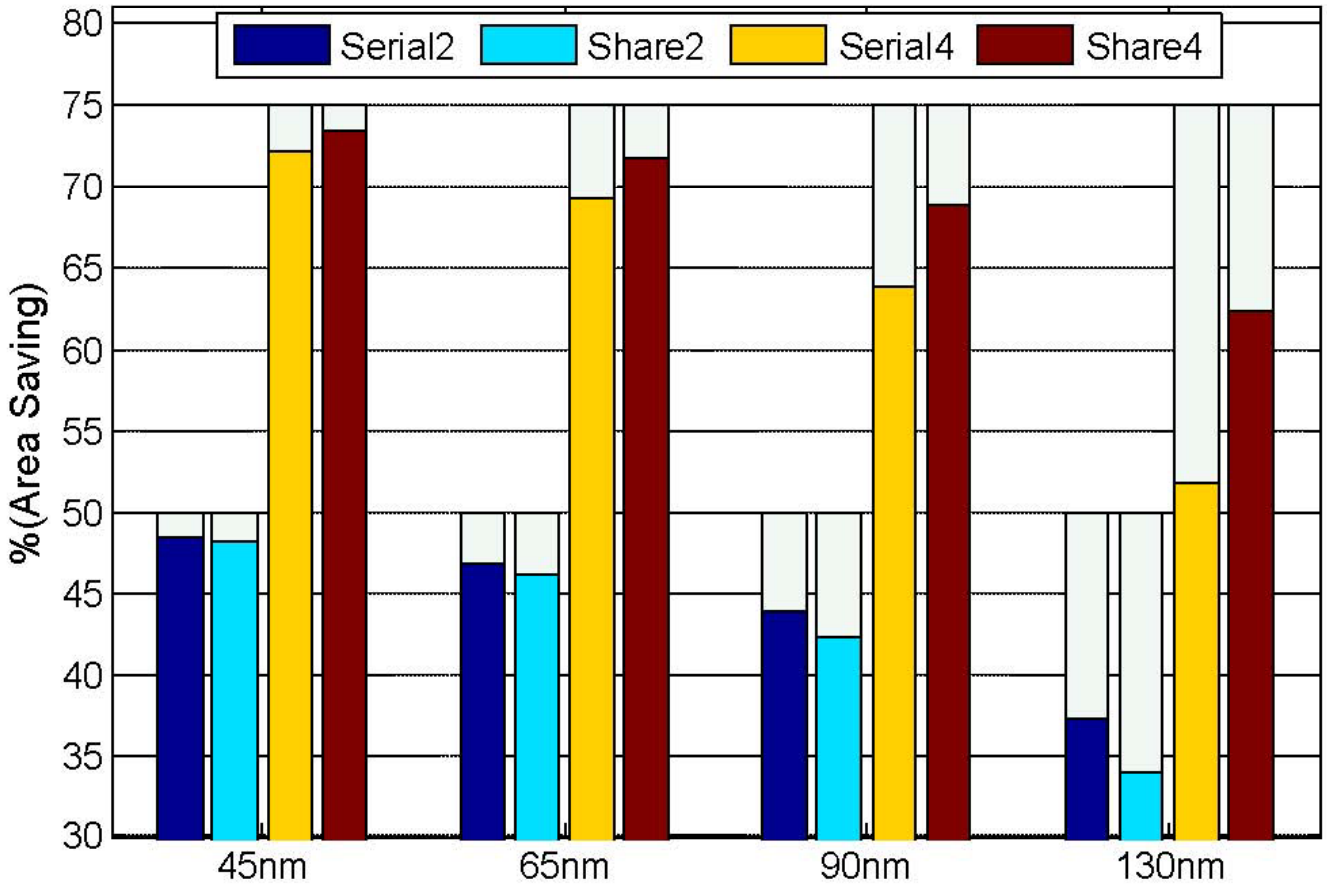
Routing: DOR (XYZ)

Arbitration Analysis



Uniform

Area Overhead



Conclusion

- Propose a TSV squeezing scheme according to the observation of TSV utilization
- Save more than 60% TSV footprint
- Less performance penalty including network latency especially zero-load latency, throughput compared with previous work

Questions?

Thank You!