Area-Efficient FPGA Logic Elements: Architecture and Synthesis

Jason Anderson and Qiang Wang[1]

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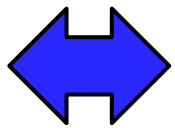
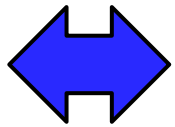
XILINX®

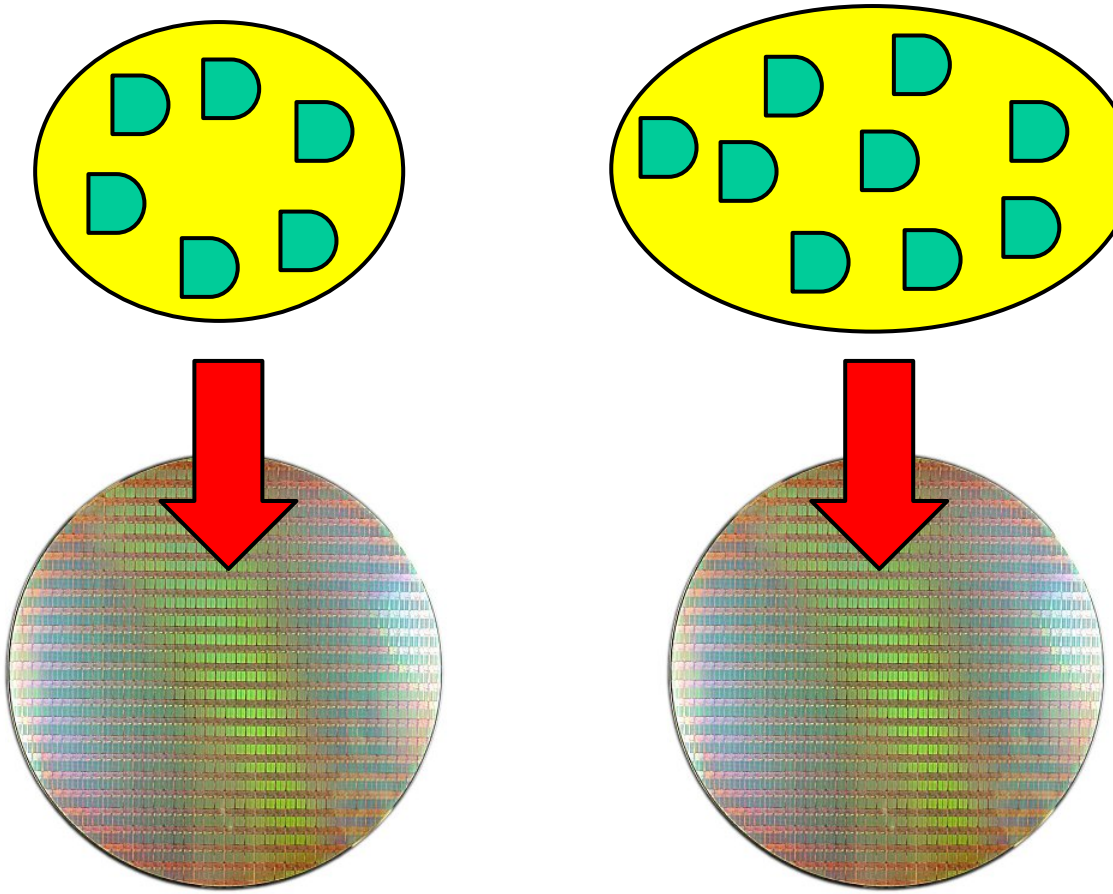
[1]Q. Wang is now with Huawei Technologies (America).

Want More for Same Money!





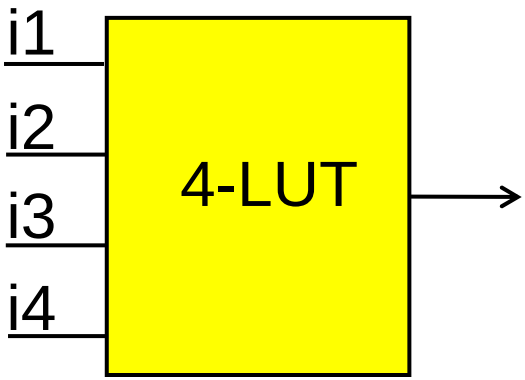
Logic Density Objective



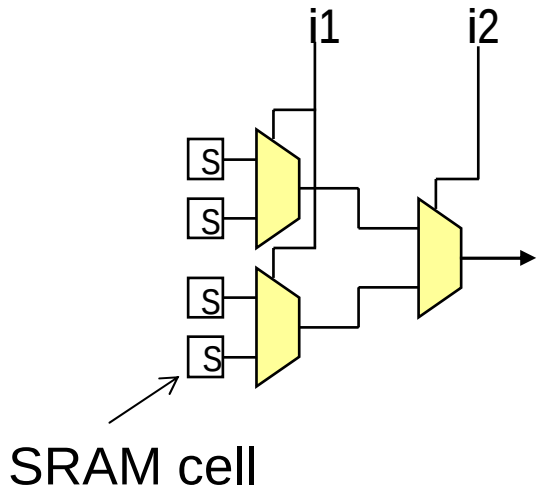
Goal: Implement more gates per unit area of silicon.

FPGA Logic Blocks

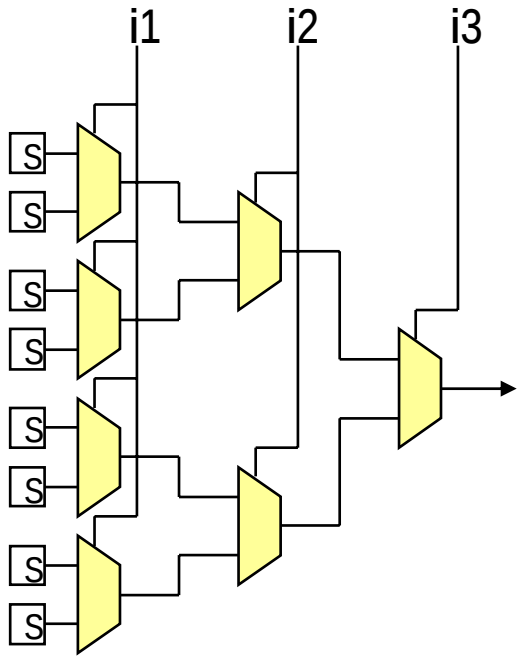
- Use LUTs to implement logic functions.



Can realize *any* 4-input function



2-LUT



3-LUT

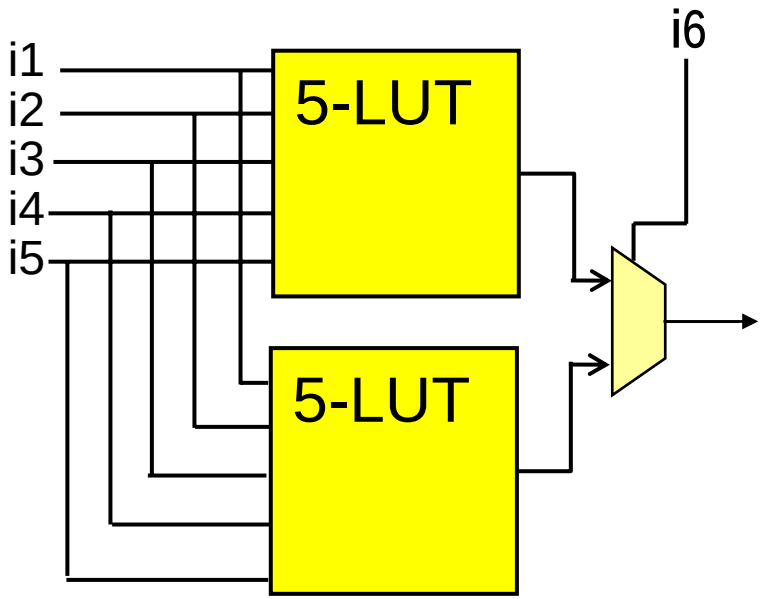
LUT size doubles with each input added.

Today's FPGAs

- Modern FPGAs use 6-LUTs:
  - Fewer levels of logic vs. 4-LUTs $\rightarrow$ leads to higher speed.
  - But, many logic functions use < 6 inputs $\rightarrow$ is hard to efficiently utilize 6-LUTs.
- 6-LUTs in modern chips "fracturable" to improve logic density.

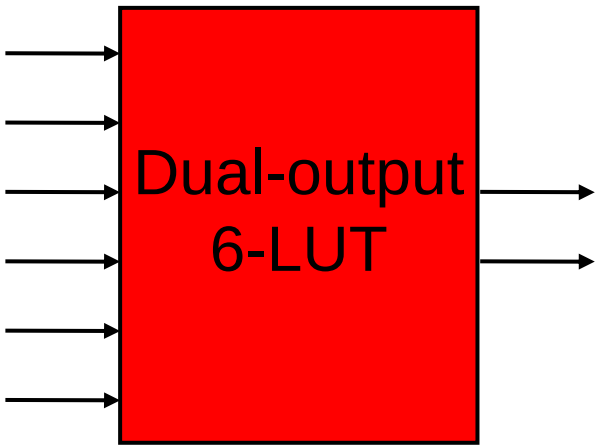
6-LUT Implementation

- 64 SRAM cells.
- 63 2-to-1 multiplexers in the tree.



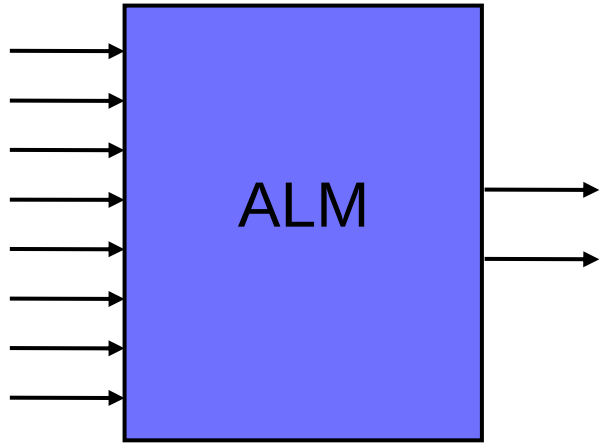
6-LUTs in Commercial Chips

Xilinx Virtex-6 LUT



One 6-input function
or any two
functions that use
up to 5 inputs.

Altera Stratix-IV ALM



One 6-input function,
two 4-input functions,
one 5-input function+
one 3-input function,
others.

Shannon Decomposition

- Consider Boolean function of n variables:

$$g = f(x_1, x_2, \ldots, x_i, \ldots, x_n)$$

Can decompose w.r.t. one of its variables x_i:

$$g = x_i \cdot f(x_1, x_2, \ldots, 1, \ldots, x_n) + \overline{x}_i \cdot f(x_1, x_2, \ldots, 0, \ldots, x_n)$$

Shannon Decomposition

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1-cofactor (g_{x_i})

0-cofactor ($g_{\overline{x}_i}$)

Co-Factor Properties

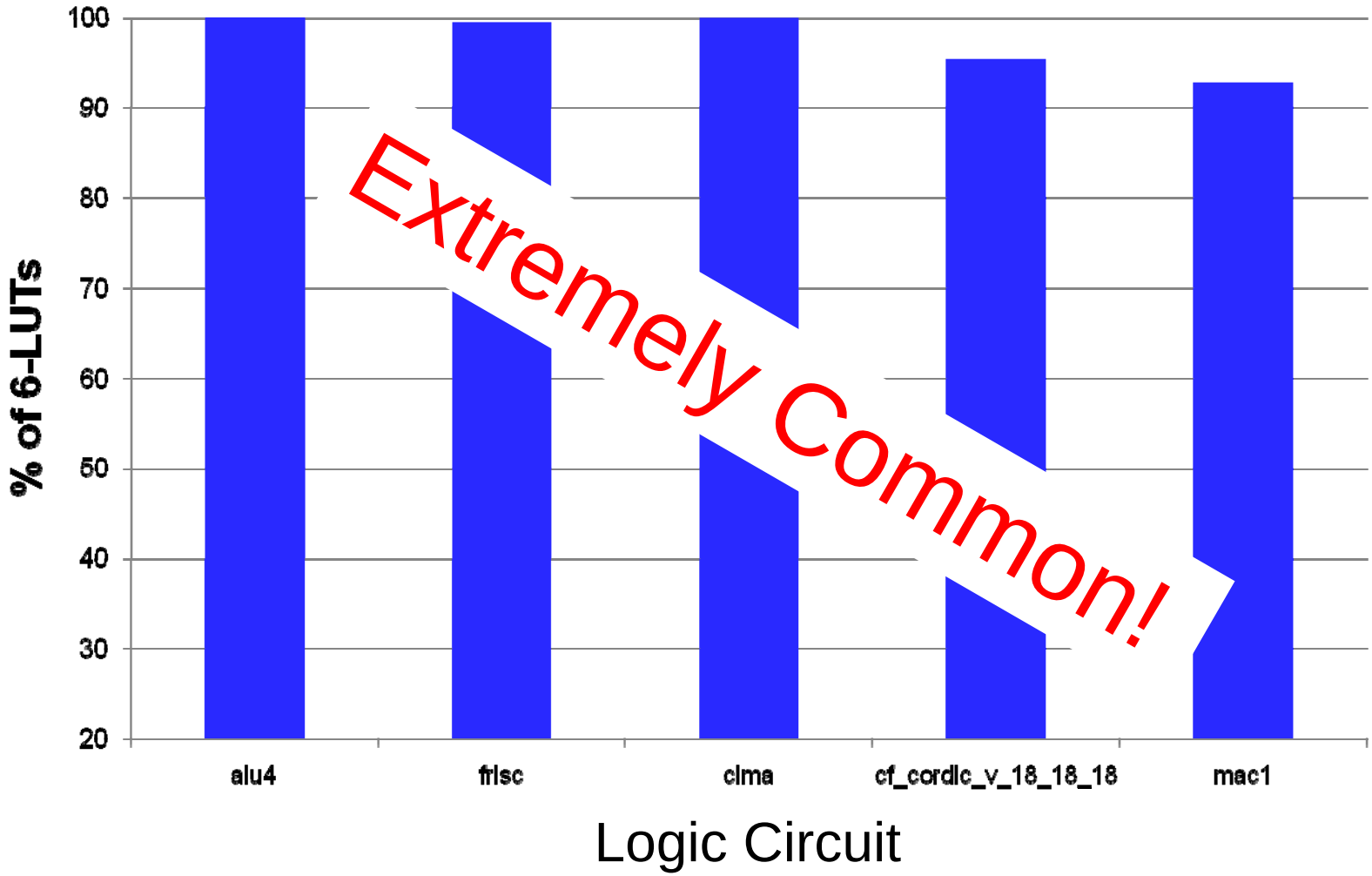
- Use $| g_{x_i} |$ to represent the # of variables in the co-factor:
  - *Size* of the co-factor.

Trimming Input Concept

- A **k**-variable logic function, $g = f(x_1, \ldots, x_k)$ has a *trimming input* x_i if either $| g_{x_i} | < \mathbf{k} - 1$, or if $| g_{\overline{x}_i} | < \mathbf{k} - 1$.

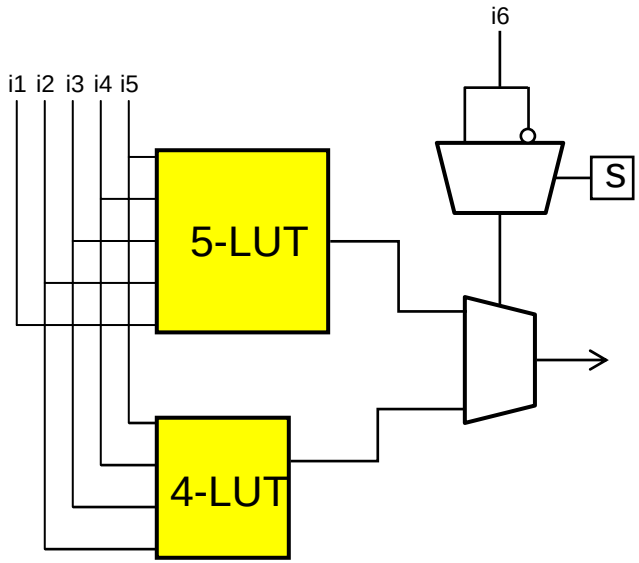
- **Example (4 variables):**
  $g = ac + a'b'd + d'a$
  1-cofactor: $g_d = ac + a'b'$ (3 variables)
  0-cofactor: $g_{d'} = ac + a = a$ (1 variable)
- **d is a trimming input.**

How Common Are Trimming Inputs?



Proposed 5+4-LUT Architecture

- 6-variable functions with a trimming input can fit into:



Contains:

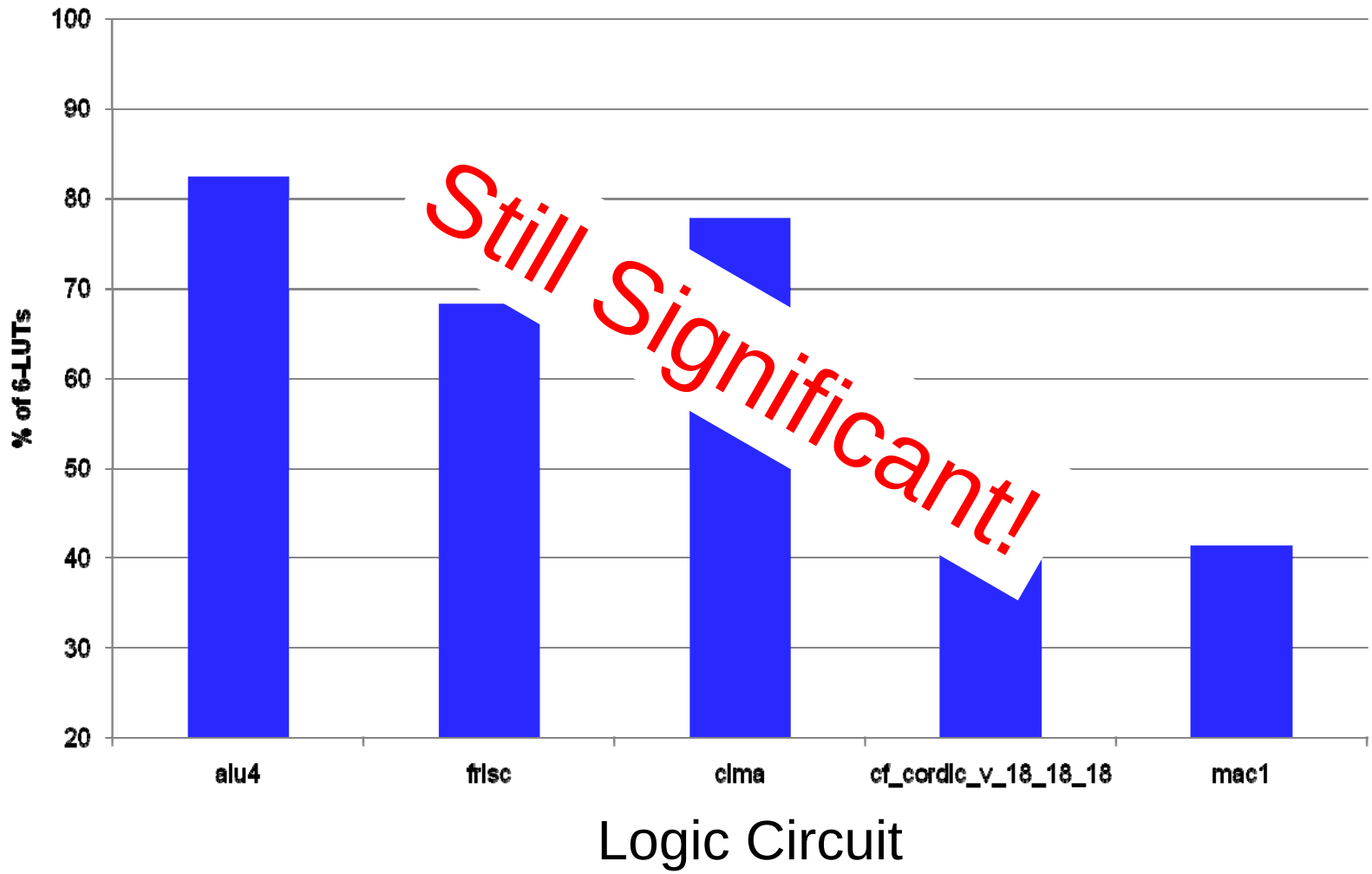
32 + 16 + 1 = 49 SRAM cells (vs. 64 in 6-LUT)

31 + 15 + 2 = 48 2-to-1 multiplexers (vs. 63 in 6-LUT)

Gating Input Concept

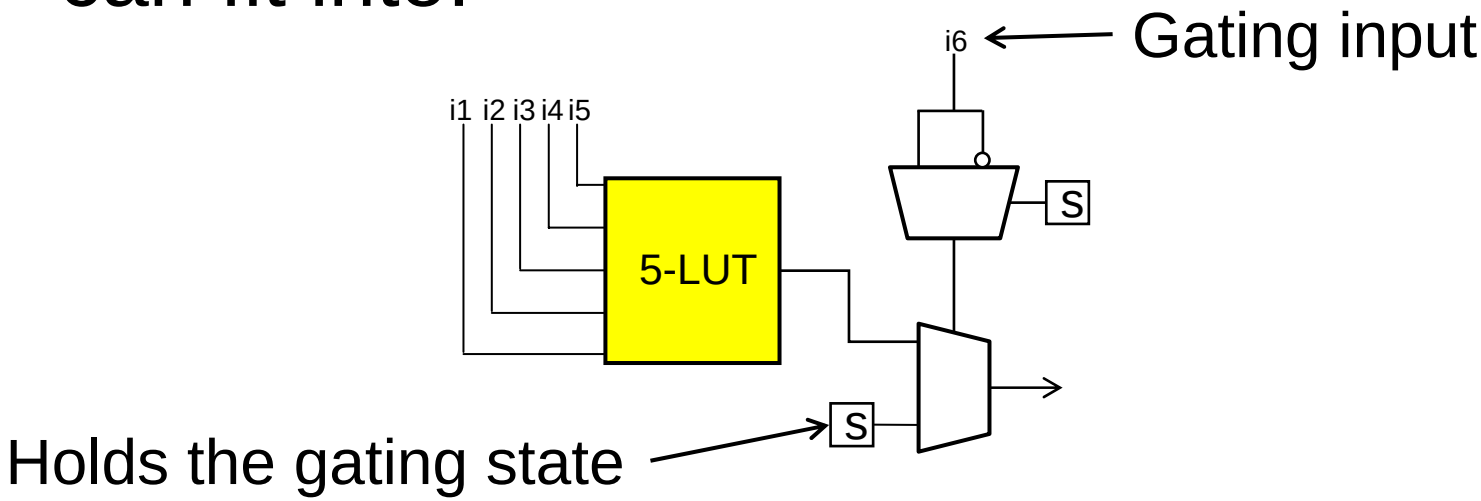
- A k-variable logic function,
  $g = f(x_1, \ldots, x_k)$ has a *gating input* x_i
  if either $| g_{x_i} | = 0$, or if $| g_{\overline{x}_i} | = 0$.
- *Interpretation:* The (gating) state of x_i
  causes g to be logic-0 or logic-1.
- Example (4-variables):
  $g = (a+b+c)d$
  1-cofactor: $g_d = a+b+c$ (3 variables)
  0-cofactor: $g_{d'}$ = logic-0 (0 variables)

How Common are Gating Inputs?



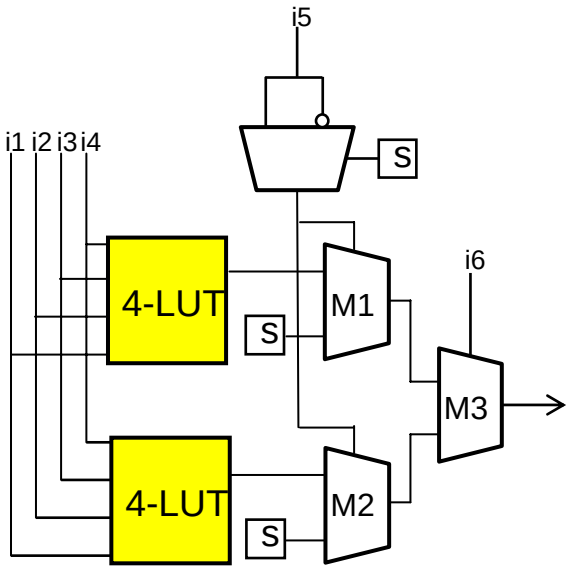
Proposed Extended 5-LUT Architecture

- 6-variable functions with a gating input can fit into:



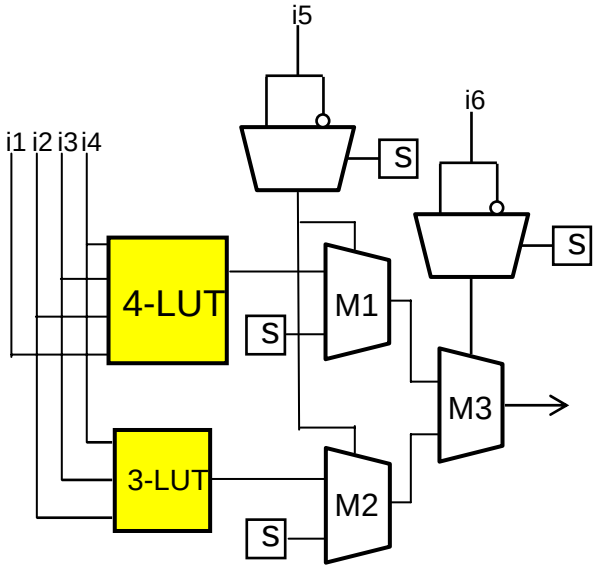
Contains:
32 +2 = 34 SRAM cells (vs. 64)
31 + 2 = 33 2-to-1 multiplexers (vs. 63)

Additional Architectures



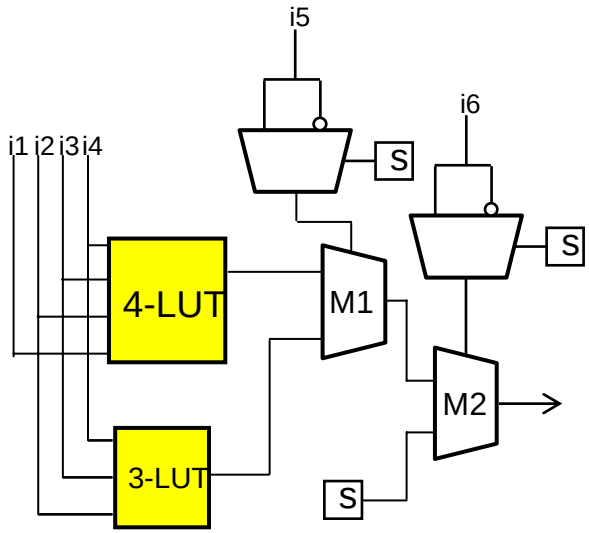
Two extended 4-LUTs

35 SRAM cells



Extended 4-LUT + extended 3-LUT

28 SRAM cells



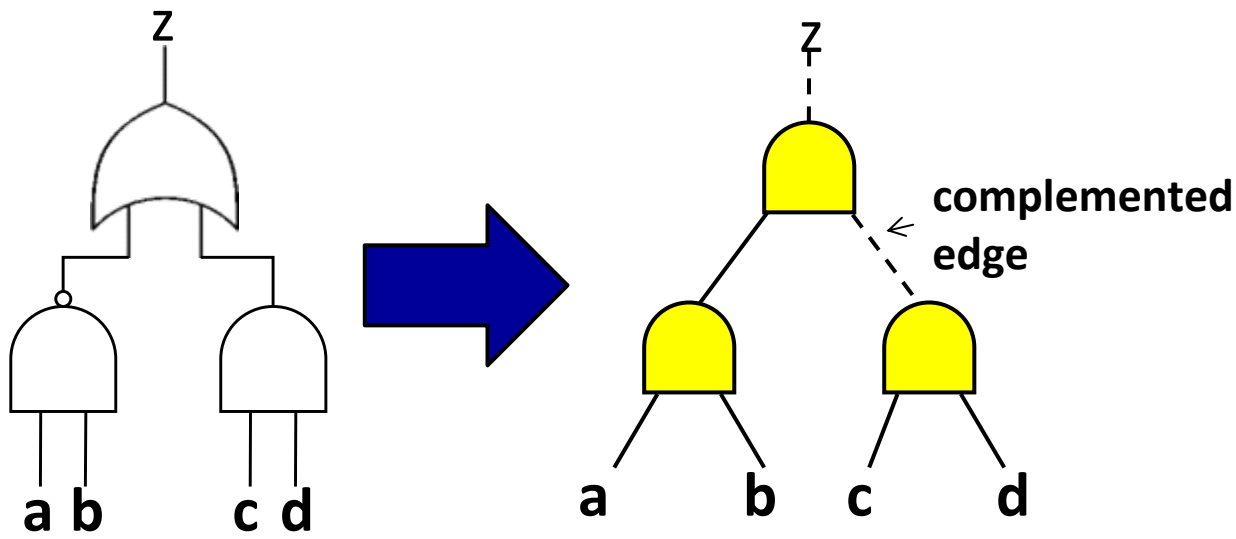
Extended 4+3-LUT

27 SRAM cells

ABC Logic Synthesis

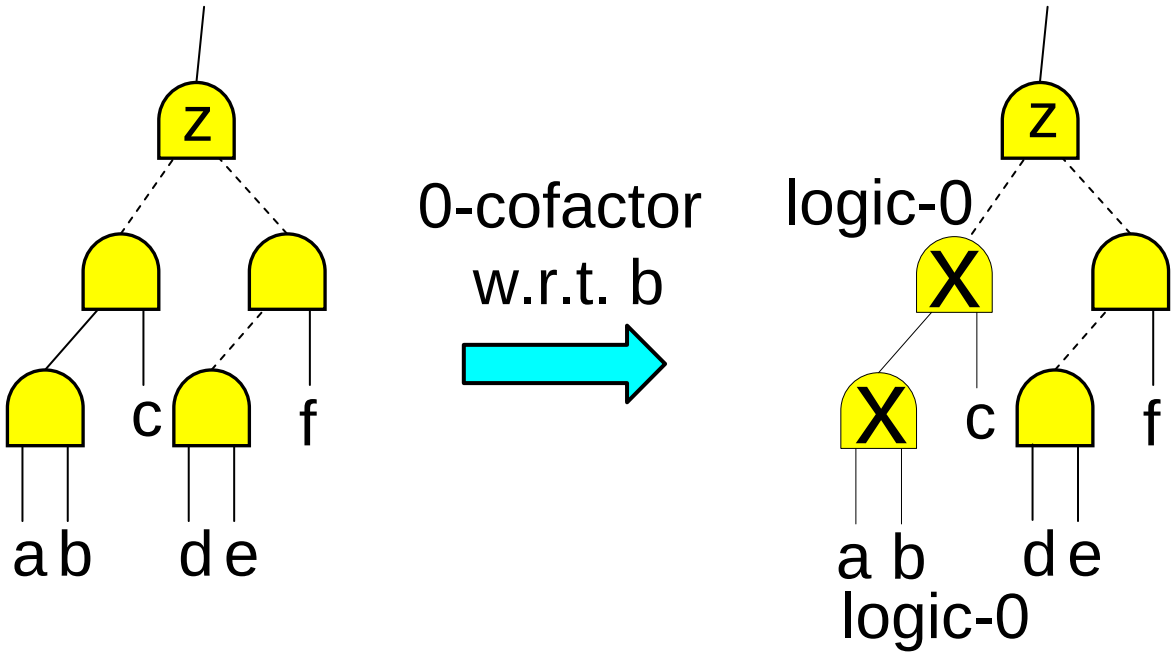
- Mainly developed at UC Berkeley

  [Primary developer: Mishchenko starting 2005/2006].
- Uses an **AND-INVERTER graph (AIG)**:



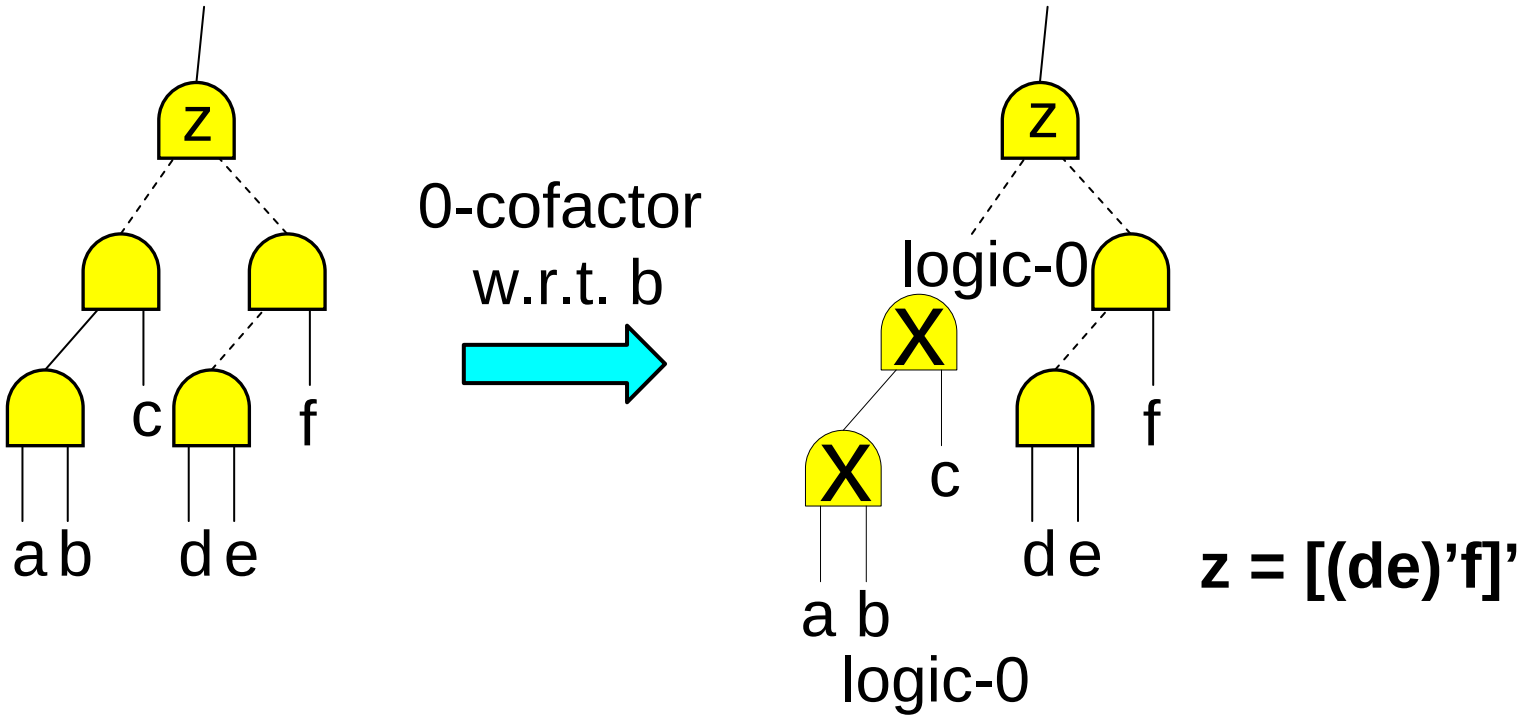
- Quality LUT mapping solutions.

Finding Shannon Co-Factors is Easy in ABC



Observation: setting an AIG input to logic-0 or logic-1 simply “eliminates”a chunk of the AIG.

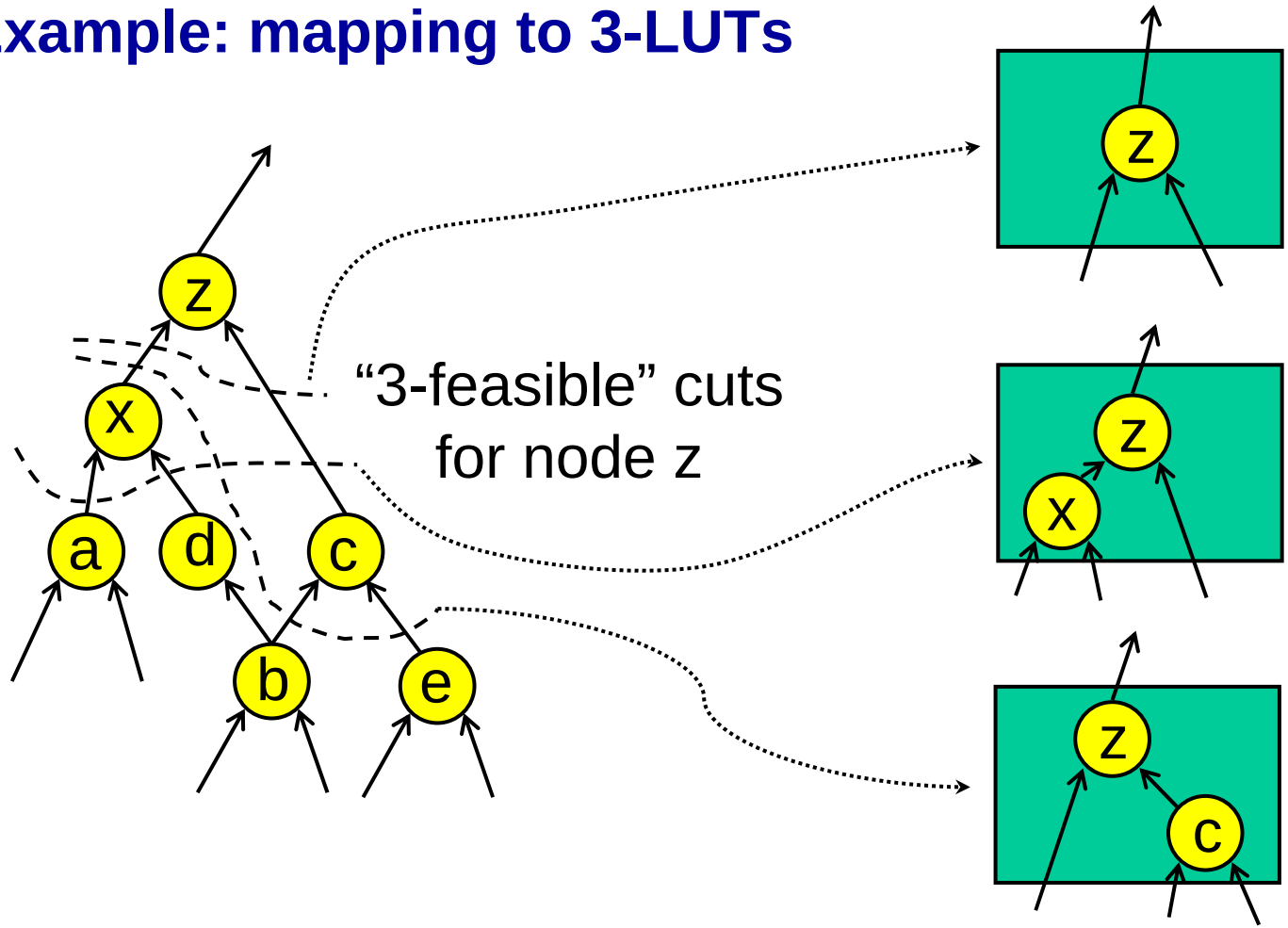
Finding Shannon Co-Factors is Easy in ABC



Observation: setting an AIG input to logic-0 or logic-1 simply "eliminates"a chunk of the AIG.

FPGA Technology Mapping

Based on notion of “cuts”.
Example: mapping to 3-LUTs

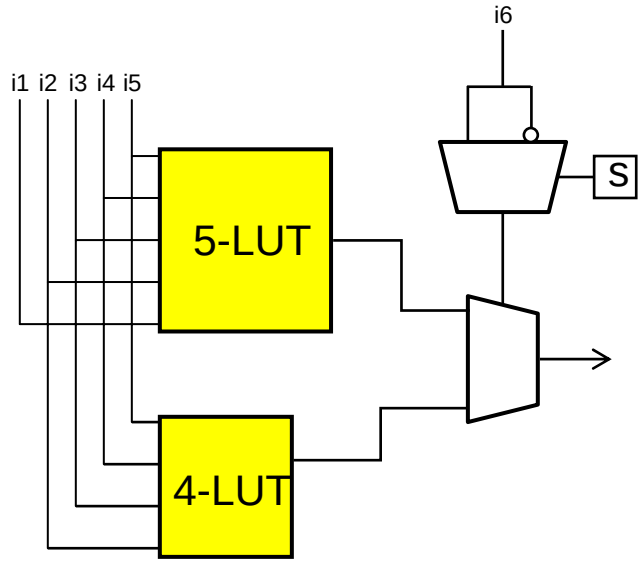


Tech Mapping to K-LUTs

1. Walk circuit DAG from PIs to POs:
   - Compute K-feasible cuts for each node.
   - Select a “best” cut for each node:
     - Best: area, depth, power, etc.
2. Walk circuit DAG from POs to PIs:
   - Construct mapped network by instantiating the selected best cuts.

Technology Mapping

- Discard cuts that do not meet requirements of target architecture.
  - Easy check with AIGs/Shannon decomp.
- **Example:**

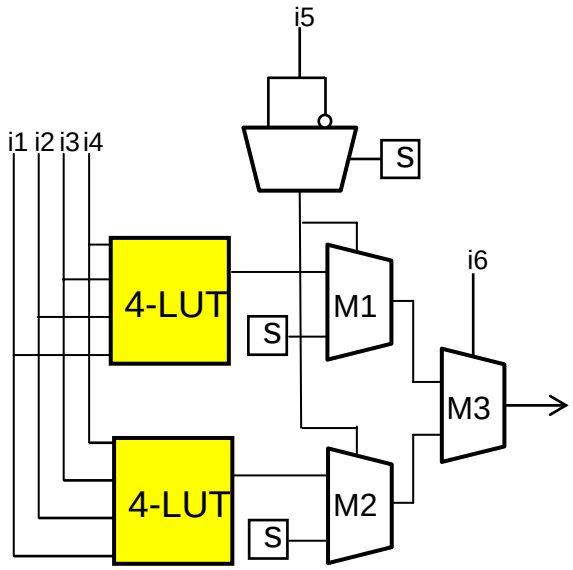


5+4-LUT architecture

Consider a cut C for function g:
1)If |Inputs(C)| < 6, C qualifies.
2)If |Inputs(C)| = 6, C qualifies iff
$\exists$ i $\in$ Inputs(C) such that
$|g_i| < 5$ or $|g_i| < 5$.

Technology Mapping

- Example 2:



Two extended 4-LUTs

Which functions can fit?

1)Any function that uses $\leq$ 4 inputs.
2)Any 5-input function.
3)Any 6-input function where:
a) both co-factors w.r.t. an input require no more than 4 distinct variables OR
b) both co-factors w.r.t. an input have a (different) gating input.

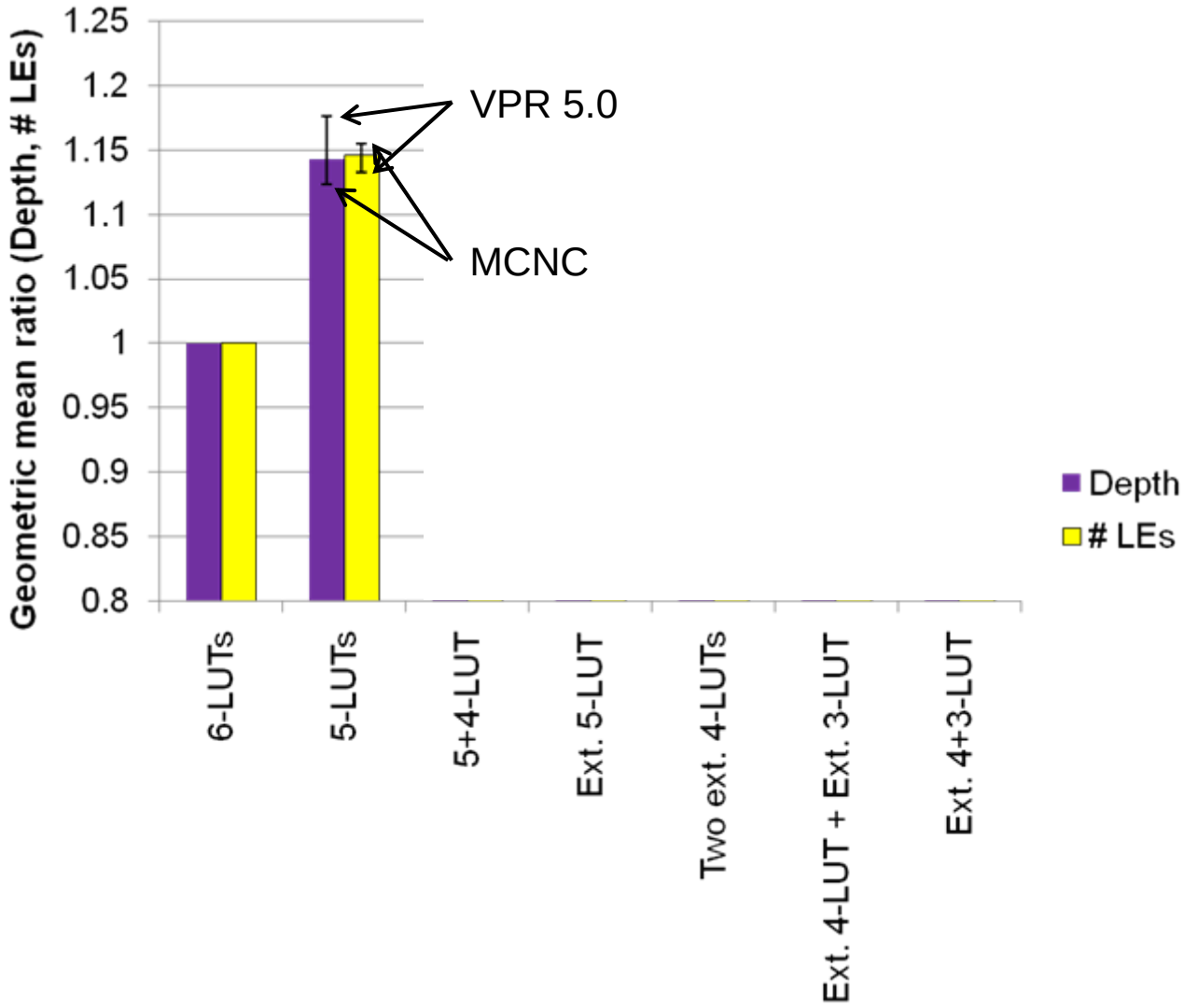
Methodology

- Two metrics:
  - # of logic elements (area).
  - Mapped circuit depth
    [# of logic elements on the critical path]
    (speed).

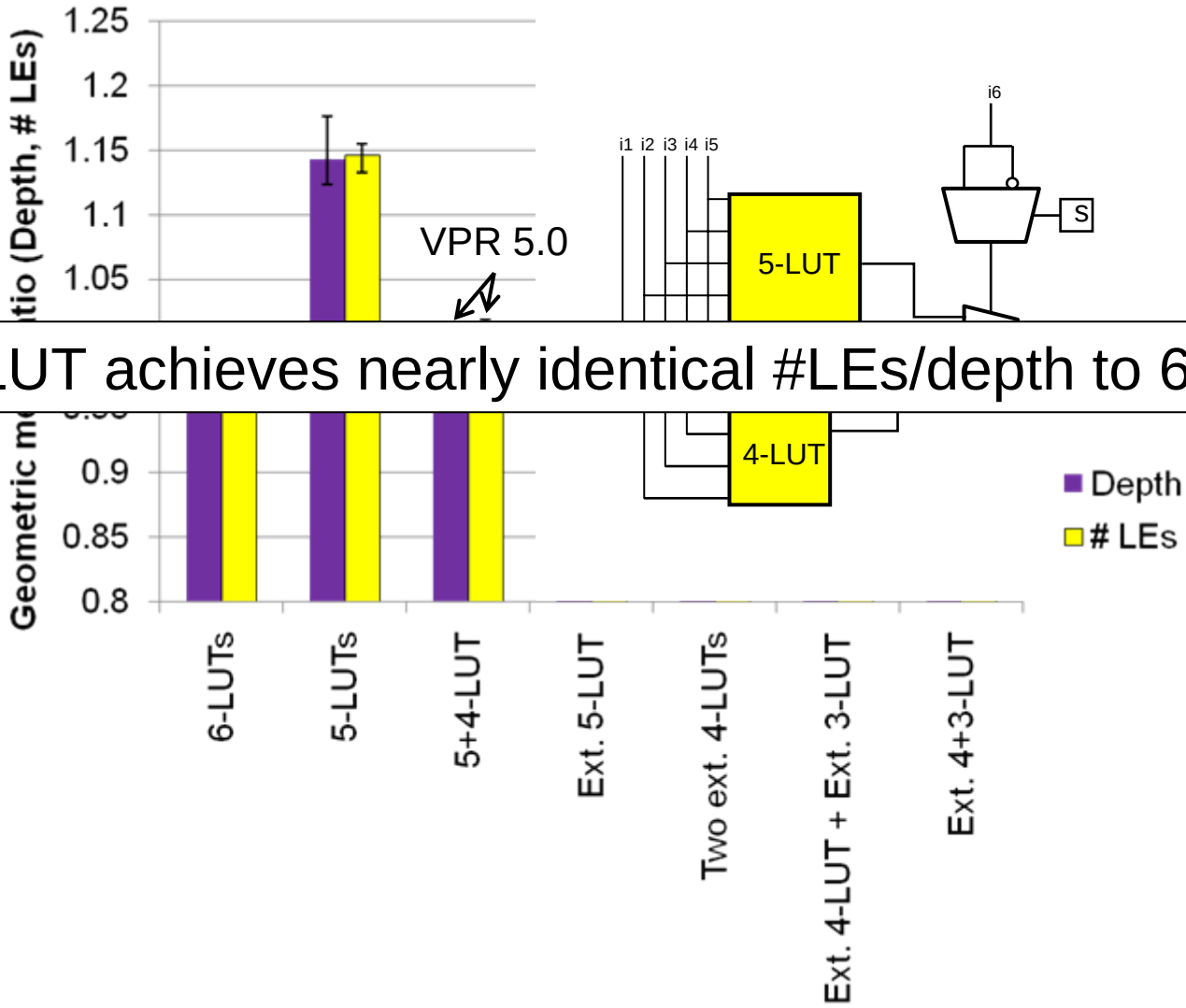
Methodology

- 20 MCNC circuits; 13 VPR 5.0 circuits.
  - VPR 5.0 circuits synthesized to BLIF using Quartus 9.1 / QUIP.
- Baseline mapper: priority cuts [ICCAD'07] (`if` command in depth mode).
- `resyn2` tech. independent synthesis.
- Tech. indep. synth. + mapping run 6 times for each cct & best result taken.

Results

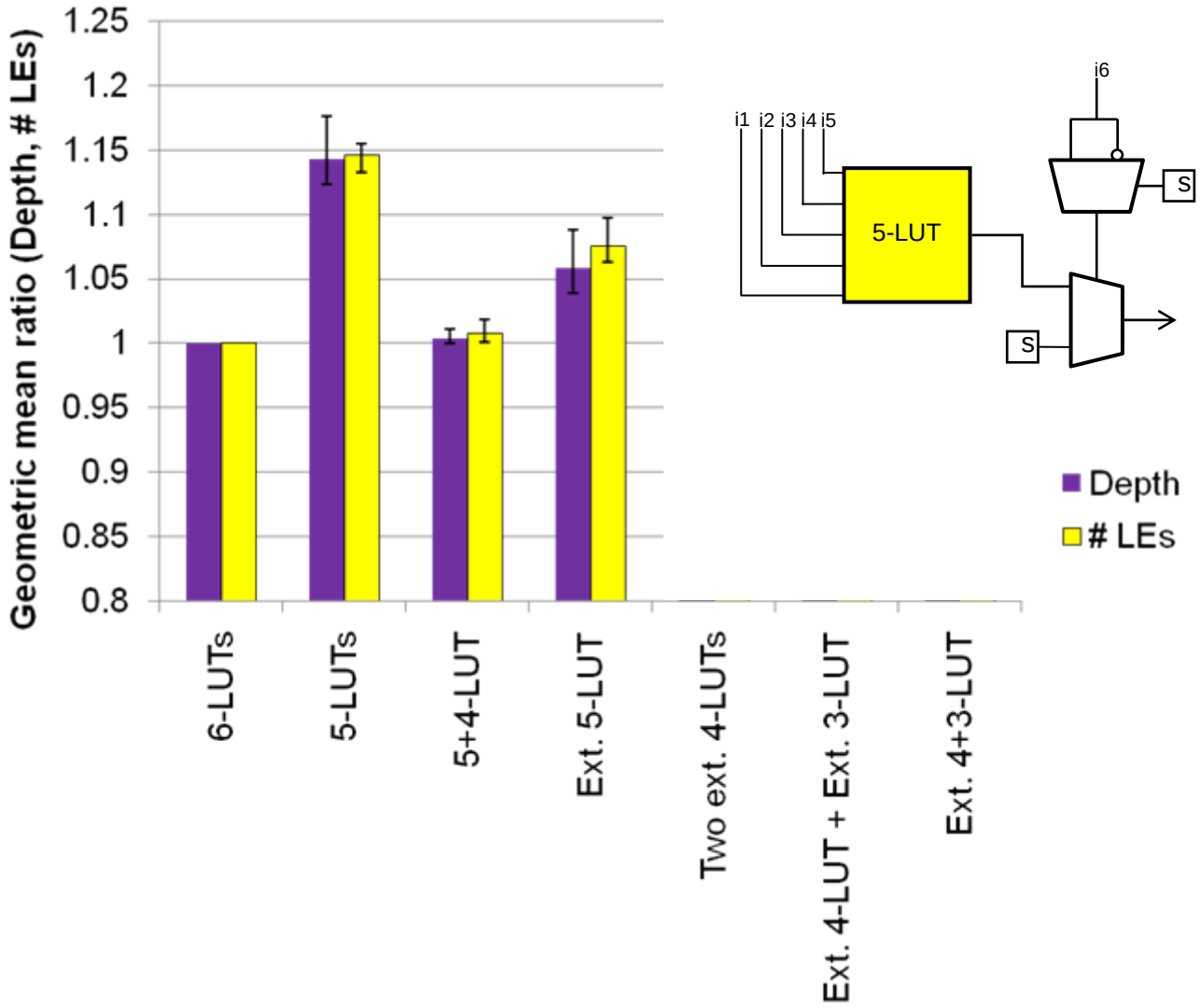

Geometric mean ratio (Depth, # LEs)
1.25
1.2
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
VPR 5.0
MCNC
6-LUTs
5-LUTs
5+4-LUT
Ext. 5-LUT
Two ext. 4-LUTs
Ext. 4-LUT + Ext. 3-LUT
Ext. 4+3-LUT
Depth
LEs

Results



5+4-LUT achieves nearly identical #LEs/depth to 6-LUT

Results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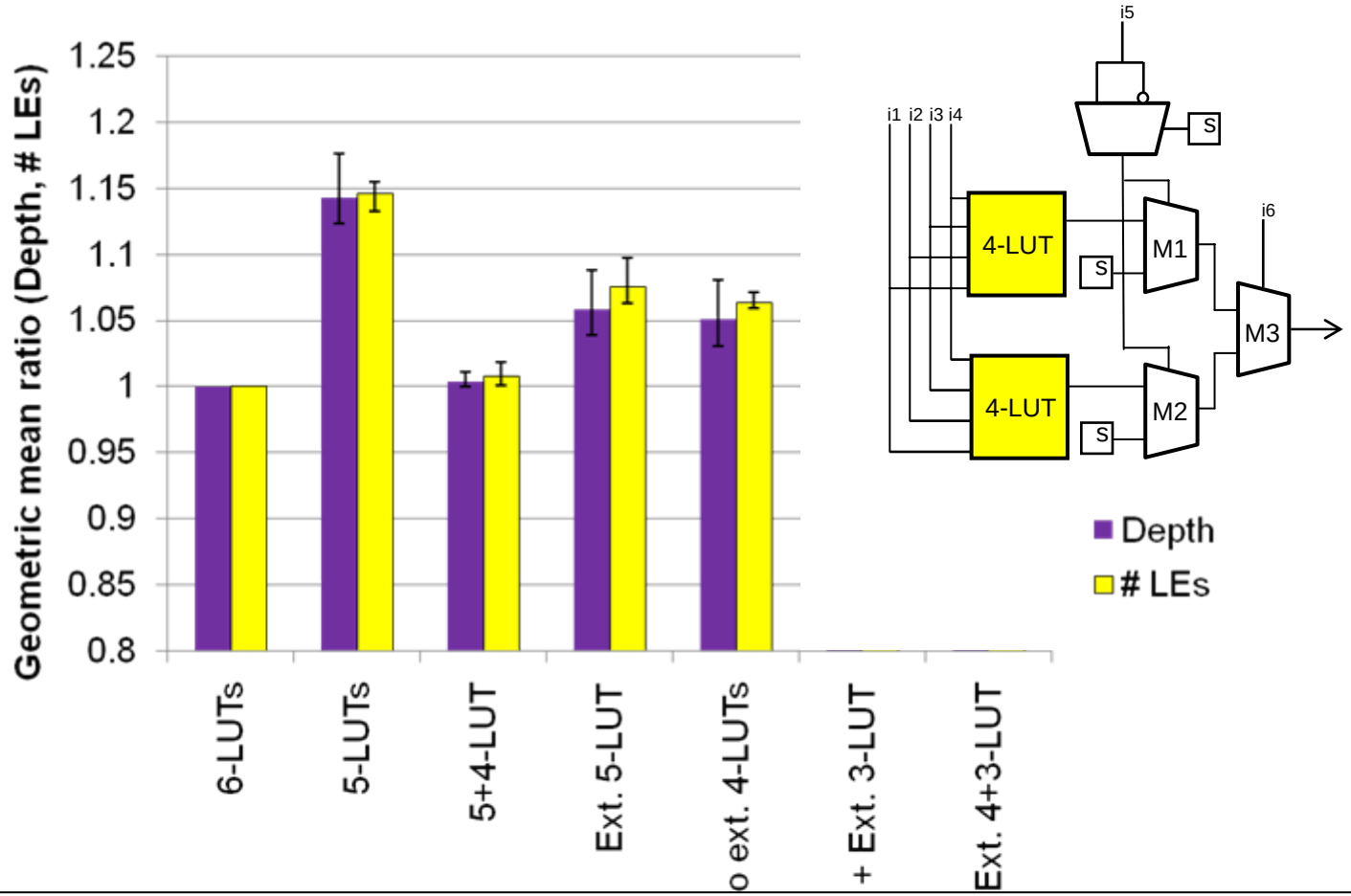
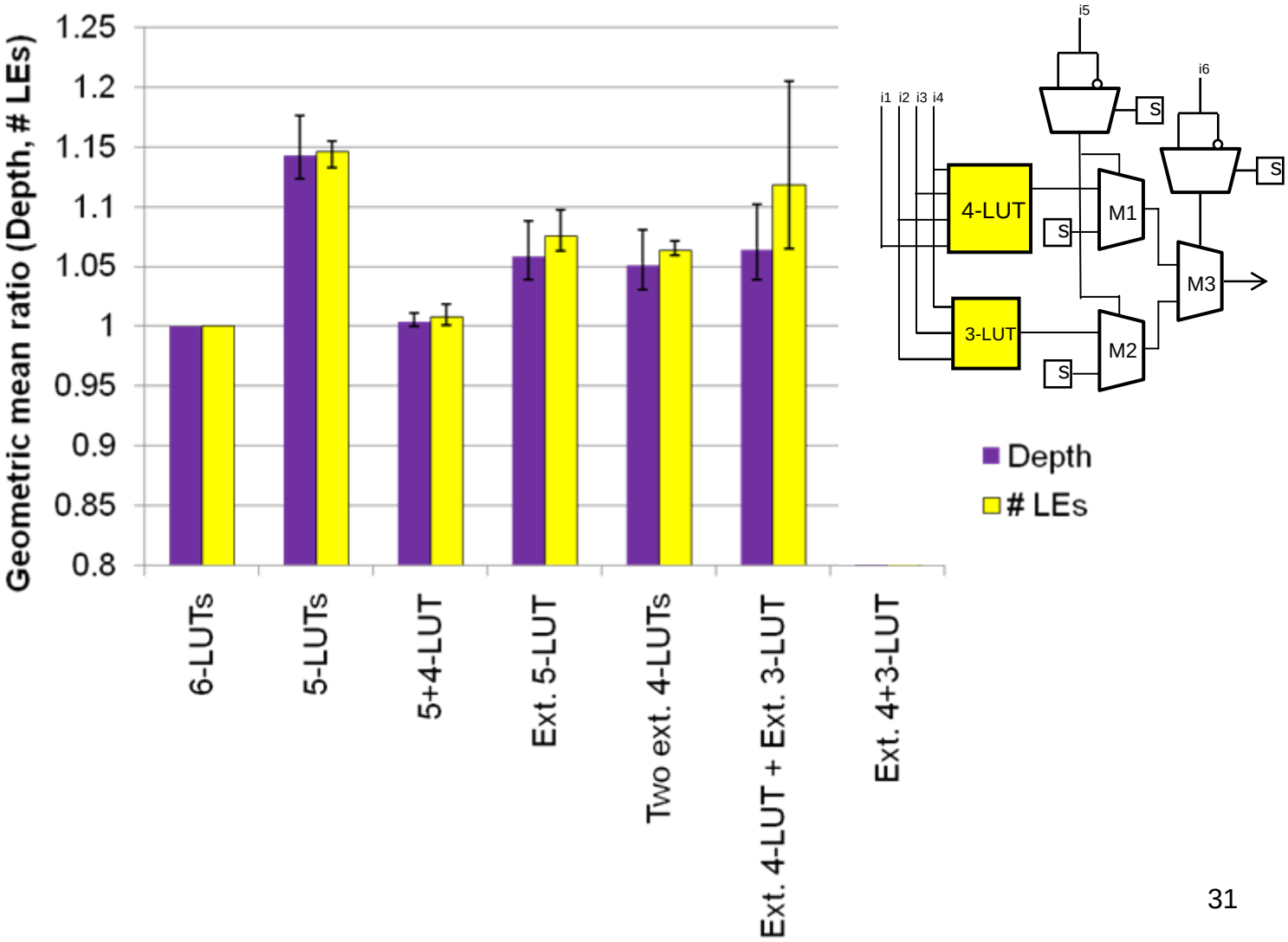
5+4-LUT
Ext. 5-LUT
Two ext. 4-LUTs
Ext. 4-LUT + Ext. 3-LUT
Ext. 4+3-LUT
Depth
LEs
i1 i2 i3 i4 i5
i6
5-LUT
S
S

Results



Better than extended 5-LUT for almost same silicon area.

Results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1.15
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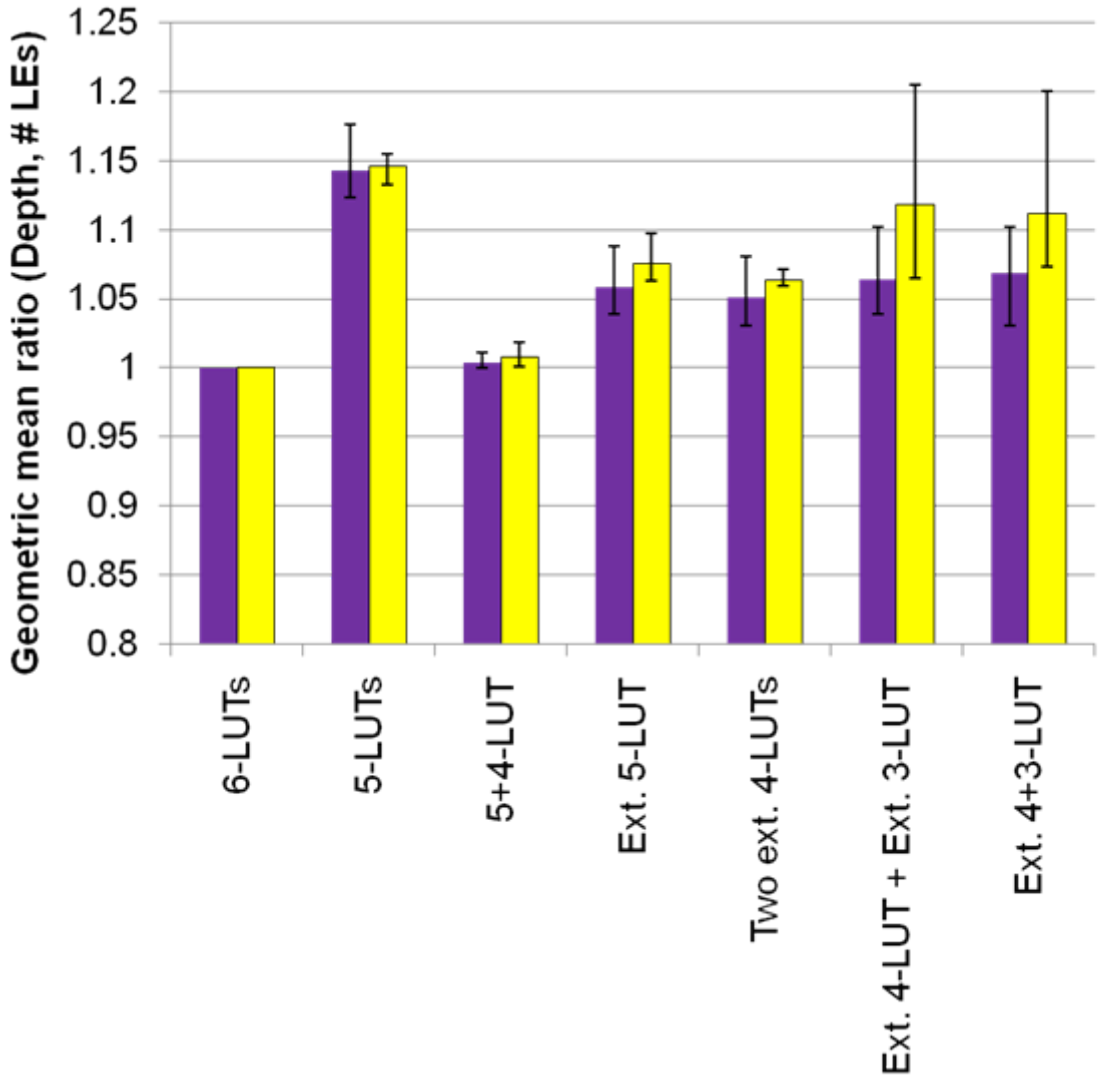
Depth
LEs
i1 i2 i3 i4
i5
i6
S
4-LUT
3-LUT
M1
M2
M3

Results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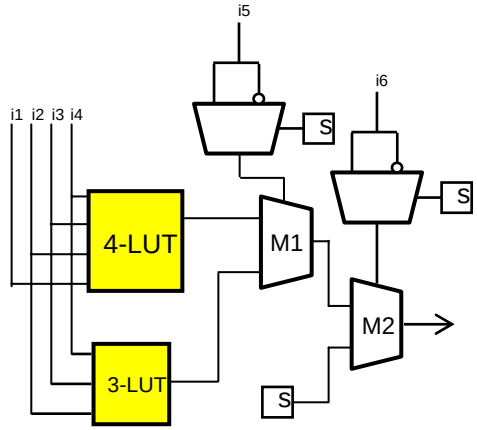
Depth
LEs


i5
i6
i1 i2 i3 i4
S
S
4-LUT
M1
M2
3-LUT
S

Overall Logic Density Estimate

- Assume baseline 6-LUT FPGA architecture with core tile silicon area breakdown:
  - 50% routing; 25% LUT; 25% other (FF, carry, etc).
- Assume LUT portion reduced in proportion to # SRAM cells in LE.

Architecture	SRAM cells	Ratio vs. 6-LUTs
6-LUT	64	1.00
5-LUT	32	0.50
5-LUT + 4-LUT	49	0.77
Extended 5-LUT	34	0.53
Two ext. 4-LUTs	35	0.55
Ext. 4-LUT + Ext. 3-LUT	28	0.44
Extended 4-LUT + 3-LUT	27	0.42

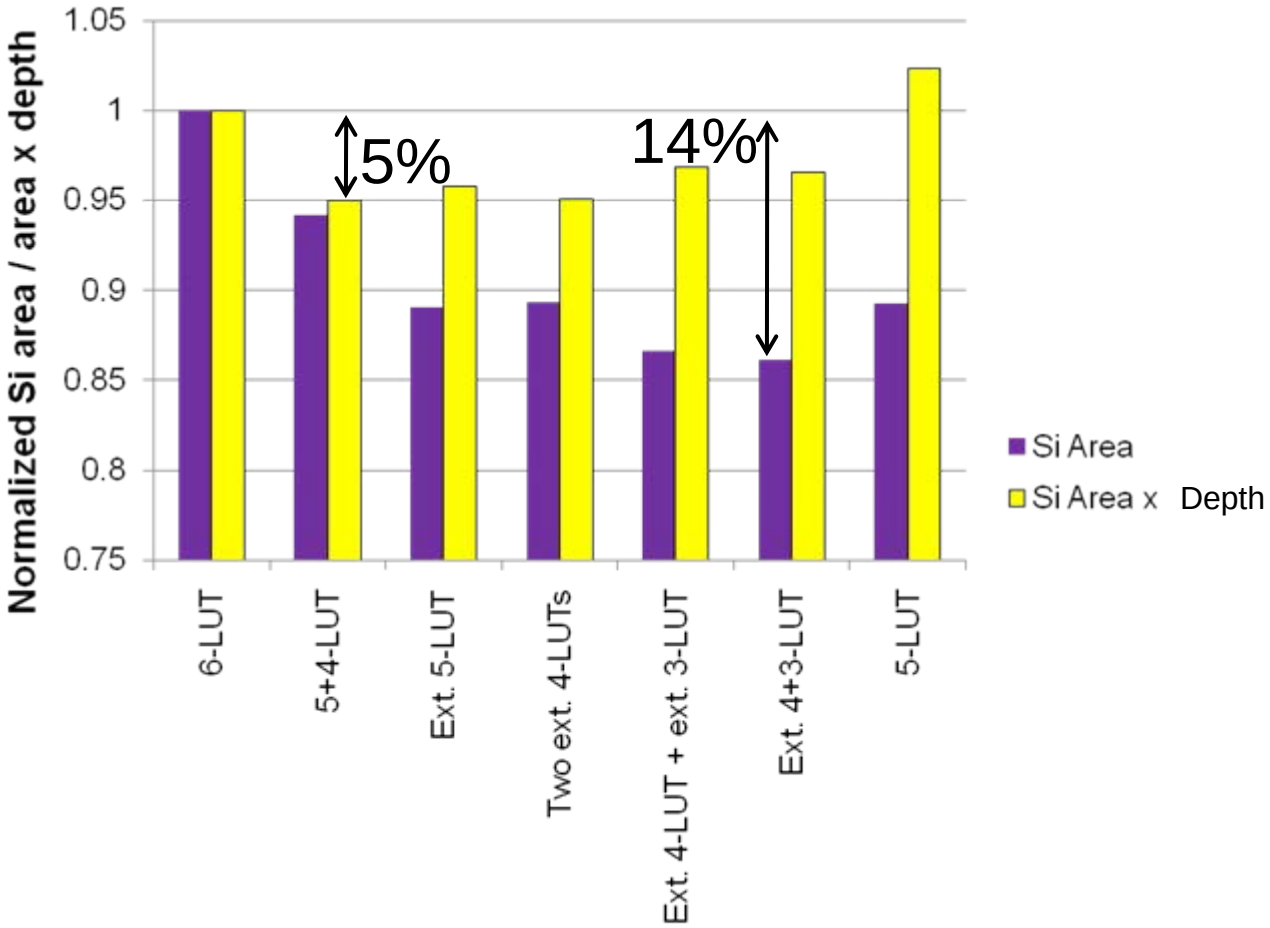
Si area relative to baseline arch = f X (75% + 25% X s)

Ratio of # of LEs needed (>=1)

Ratio of # SRAM cells (<=1)

Area & Area-Depth Product

- Average across **33** circuits:



Summary

- Logic functions very often have *trimming inputs*.
  - Inspire new logic element architectures.
- New elements can achieve estimated 14% improvement in logic density vs. 6-LUTs; 5% improvement in area-depth product.
  - May also offer power benefits.
- Results for 7-input elements in paper.
- Future work: don’t cares; fracturable LUTs.

Back-Up Slides

	6-LUTS		5+4-LUT		Ext. 5-LUT		Two ext. 4-LUTs		Ext. 4 + Ext. 3		Ext. 4+3-LUT		5-LUTs	
CIRCUIT	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**
alu4	5	774	5	774	6	751	6	760	6	734	6	751	6	866
apex2	6	868	6	868	6	906	6	906	6	901	6	906	7	990
apex4	5	752	5	752	5	766	5	769	5	762	5	766	6	840
bigkey	3	579	3	579	3	691	3	689	3	691	3	692	3	806
clma	10	2795	10	2767	10	3231	10	2917	10	3044	10	3237	12	3179
des	4	691	4	725	5	848	5	819	5	867	5	845	5	948
diffeq	8	636	8	643	9	722	9	723	9	733	9	730	9	757
dsip	3	689	3	691	3	691	3	691	3	694	3	692	3	692
elliptic	10	1797	10	1797	11	1828	11	1832	11	1843	11	1842	12	1873
ex1010	6	2452	6	2456	6	2505	6	2517	6	2500	6	2505	7	2755
ex5p	5	504	5	468	5	497	5	518	5	512	5	517	5	594
frisc	13	1735	13	1740	13	1832	13	1834	13	1835	13	1835	14	1842
misex3	5	723	5	723	5	745	5	746	5	741	5	751	6	811
pdc	7	1948	7	1980	7	2025	7	2071	7	2035	7	2025	7	2495
s298	8	641	8	641	8	665	8	648	8	663	8	666	9	731
s38417	7	2567	7	2551	7	2998	7	2917	7	3076	7	3024	8	3068
s38584.1	6	2287	6	2287	6	2553	6	2431	6	2509	6	2554	7	2688
seq	5	780	5	786	5	813	5	812	5	809	5	805	5	908
spla	6	1670	6	1698	7	1671	6	1804	7	1689	6	1800	7	1906
tseng	8	647	8	651	8	680	8	679	8	703	8	703	9	692
GEOMEAN (STD 20 CIRCUITS):	6.08	1075.16	6.08	1076.38	6.32	1143.29	6.27	1138.85	6.32	1144.99	6.27	1153.47	6.82	1241.43
RATIO VS 6-LUTS:			1.000	1.001	1.039	1.063	1.031	1.059	1.039	1.065	1.031	1.073	1.123	1.155

	6-LUTS		5+4-LUT		Ext. 5-LUT		Two ext. 4-LUTs		Ext. 4 + Ext. 3		Ext. 4+3-LUT		5-LUTs	
	DEPTH	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**	**DEPTH**	**AREA**
cf_cordic_v_18_18_18	9	3822	9	3866	10	4203	10	4114	10	4593	10	4585	11	4461
cf_fir_24_16_16	18	10929	18	10452	18	11843	18	11793	18	13605	18	13630	18	11668
des_perf	3	3264	3	4019	4	4314	4	4081	4	5044	4	4881	4	4959
mac1	17	1959	17	2019	18	2166	18	2108	18	2487	18	2481	21	2215
mac2	31	6906	31	7116	32	7396	32	7267	32	8406	32	8415	39	7491
oc54	22	2393	22	2385	22	2600	22	2523	22	2761	22	2780	24	2726
paj_boundtop_hierarchy_no_mem	4	1294	4	1294	4	1371	4	1327	4	1371	4	1371	6	1376
paj_raygentop_hierarchy_no_mem	16	6314	16	6193	17	6693	17	6518	17	7276	17	7281	17	6677
paj_top_hierarchy_no_mem	33	32967	33	31614	34	35196	34	33758	34	39470	34	39440	34	35016
rs_decoder_2	11	1649	12	1751	13	1919	12	1870	14	2043	14	1989	14	2265
sv_chip0_hierarchy_no_mem	5	12615	5	12684	6	12970	6	12909	6	13728	6	13727	6	12955
sv_chip1_hierarchy_no_mem	8	25473	8	24831	9	26984	9	26425	9	29564	9	29564	9	26882
sv_chip2_hierarchy_no_mem	18	46440	19	48099	19	50062	19	50070	21	55333	21	55443	19	50104
GEOMEAN (VPR 5.0 CIRCUITS):	11.88	6384.02	12.01	6505.71	12.93	7001.29	12.85	6837.28	13.10	7689.56	13.10	7658.75	13.98	7233.55
RATIO VS 6-LUTS:			1.011	1.019	1.088	1.097	1.081	1.071	1.102	1.205	1.102	1.200	1.176	1.133