Selectively Patterned Masks: Structured ASIC with Asymptotically ASIC Performance

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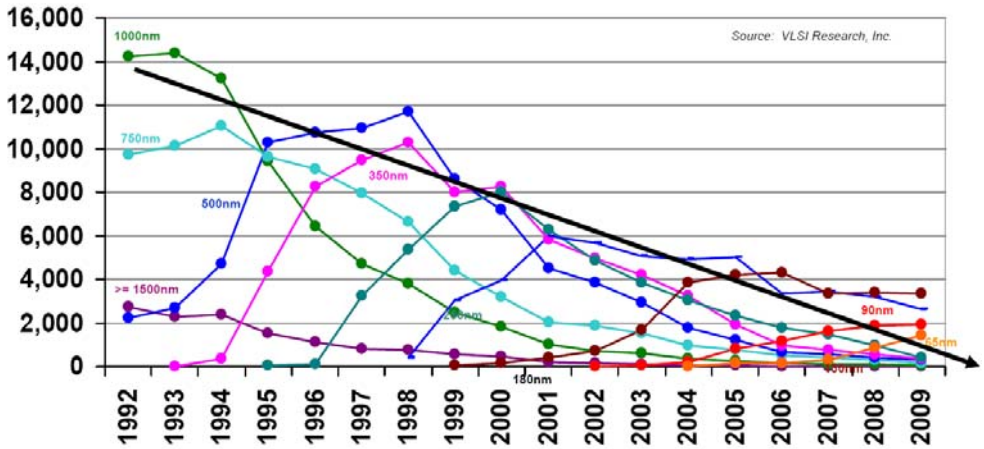
Outline

- Introduction
- Selectively patterned masks (SPM)
  - Concept
  - Pattern transfer process
  - Analysis: mask cost, throughput
- Structured ASIC using SPM
  - Tile design
  - Logic synthesis
  - Routing architecture
- Experimental results
- Conclusion

ASIC Has Been Slowed Down

- New design starts decrease
- Global alliance of foundries emerges

- **Increasing mask cost** is one of reasons



Process (μ)	2.0	0.8	0.6	0.35	0.25	0.18	0.13	0.10
Single Mask cost ($K)	1.5	1.5	2.5	4.5	7.5	12	40	60
# of Masks	12	12	12	16	20	26	30	34
Mask Set cost ($K)	18	18	30	72	150	312	1,000	2,000

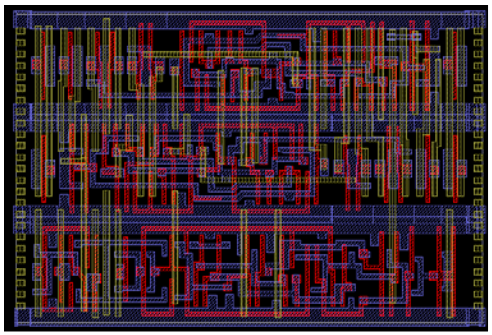
EETimes, 2002

Structured ASIC

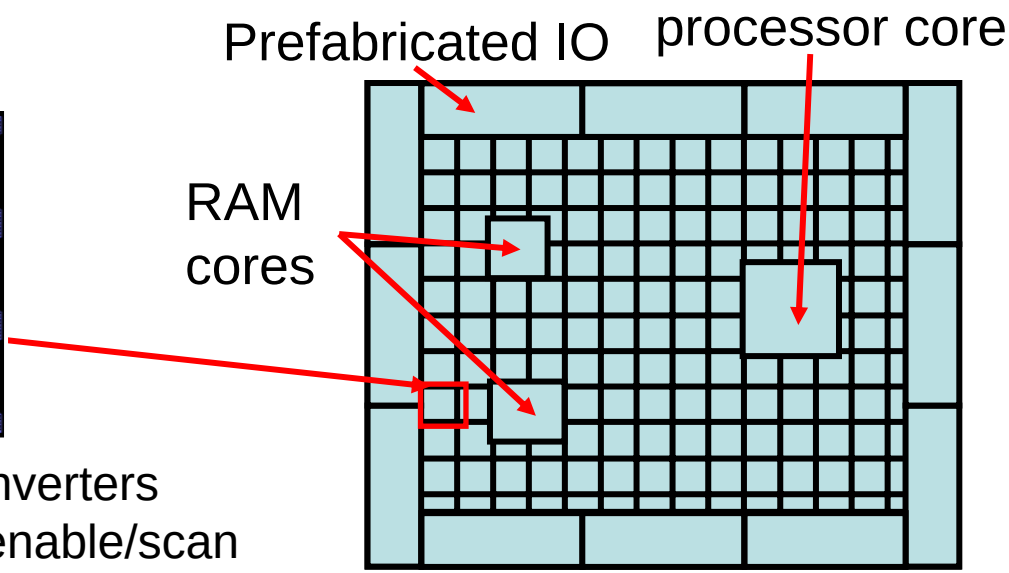
- Programmable device: a solution for mask cost

- Structured ASIC
  - Gate array has evolved into structured ASIC
  - Makes only contact/via masks for programming
    ←→ all metal and via masks in gate array

[N. Shenoy, DAC 2004]

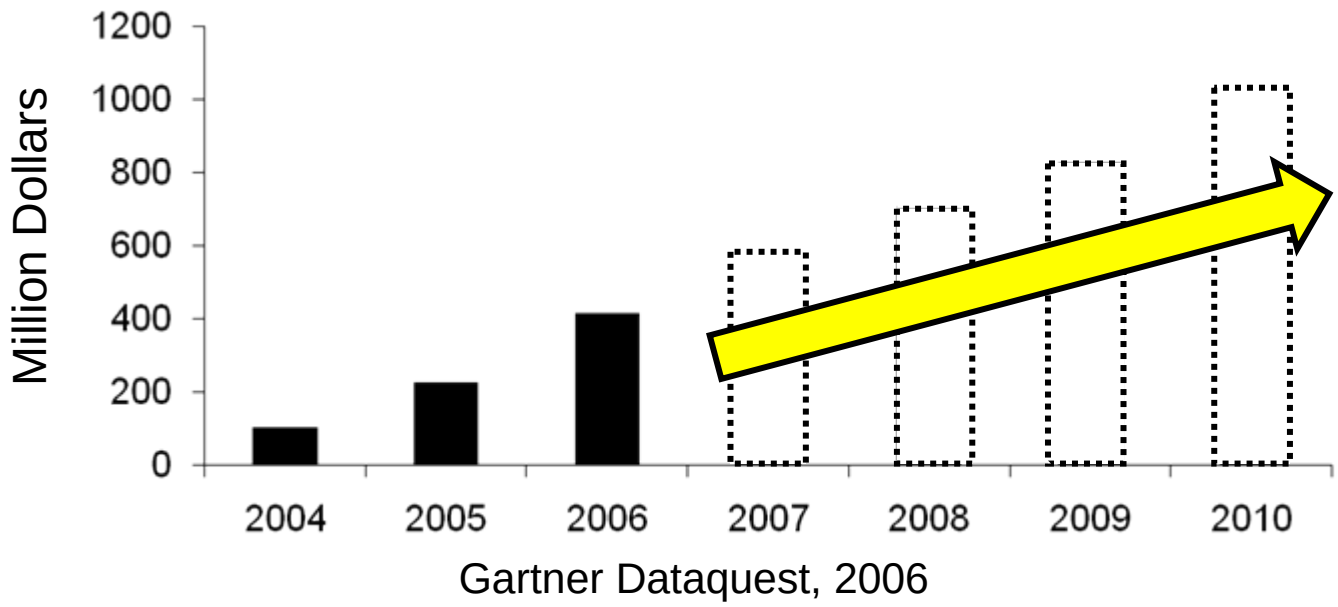


- 2 MUX tree, 2 local inverters
- A F/F with set/reset/enable/scan



Structured ASIC

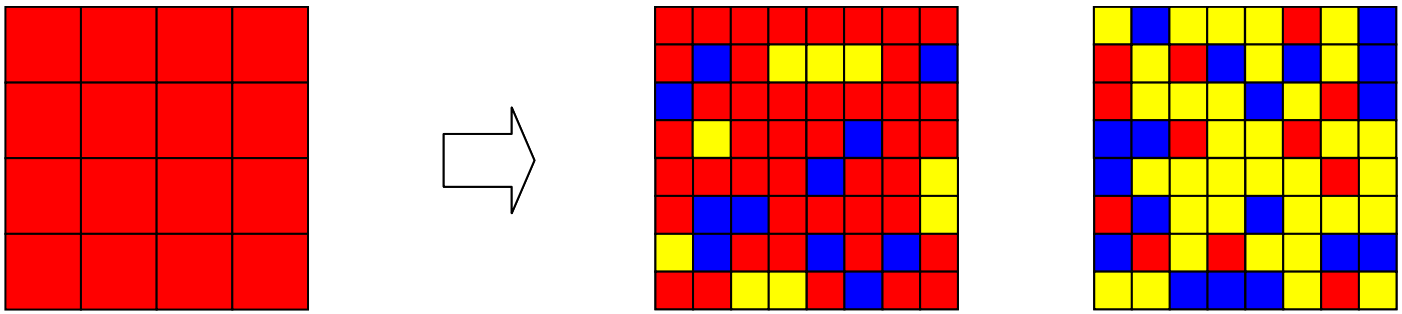
- Introduced in 1999
- Big success was expected
- Many companies jumped in the business in early 2000
- Not very successful
  - Not competitive to ASIC **(area: 3 ~ 7 times, delay: 2 ~ 6 times)**



Structured ASIC

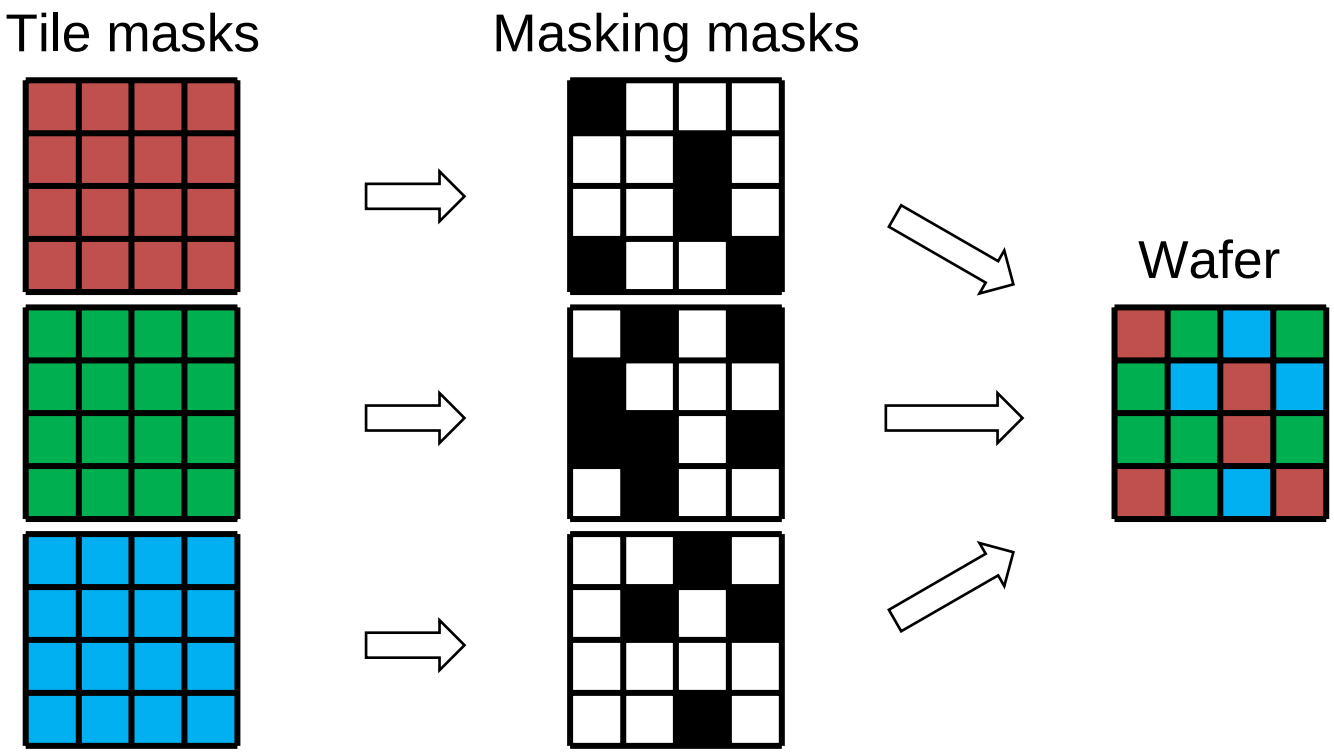
- Current SA: only one type of “tile”
  - Tile must be designed to implement any logic: too much redundancy
- **Is it possible to have multiple tiles?**
  - Different designs would need different mix of tiles

    → Have to make ALL masks!



Selectively Patterned Masks (SPM)

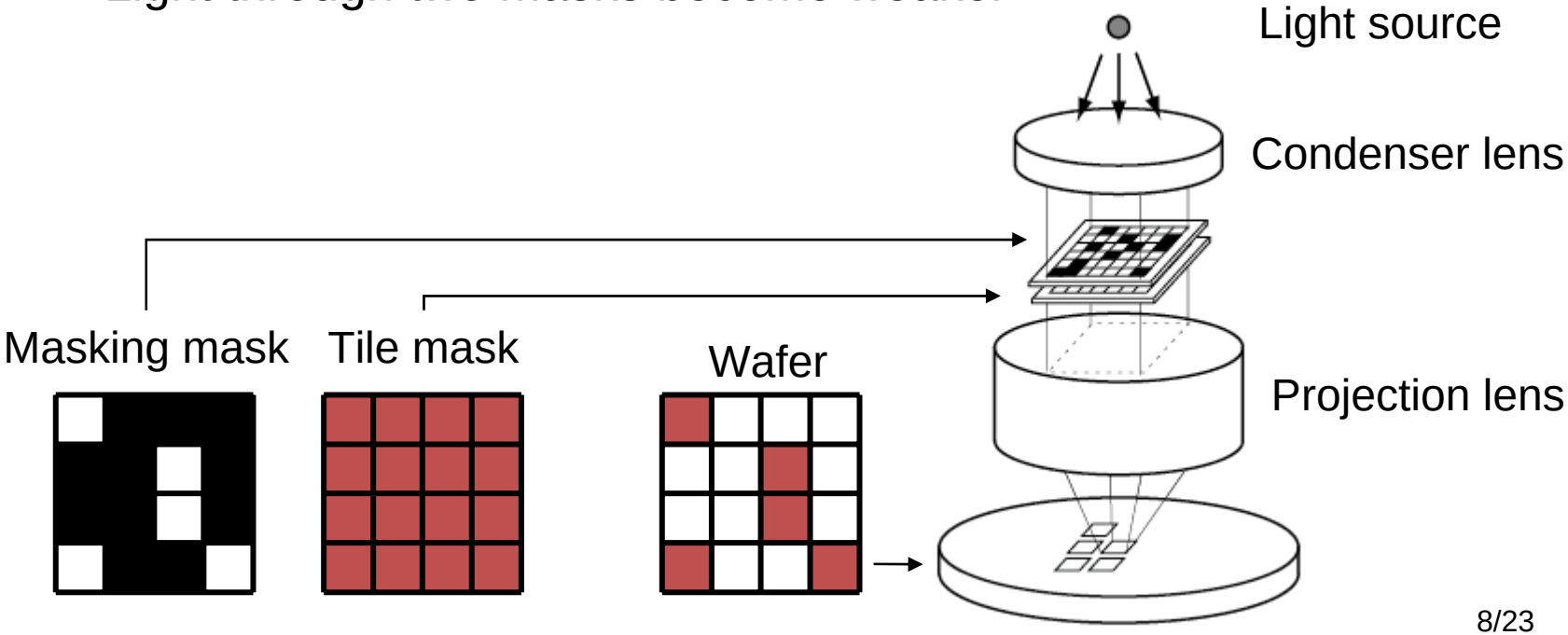
- Tile masks: homogeneous just like SA, but more than one tiles
- **Masking masks:** used to selectively pattern tiles



Selectively Patterned Masks (SPM)

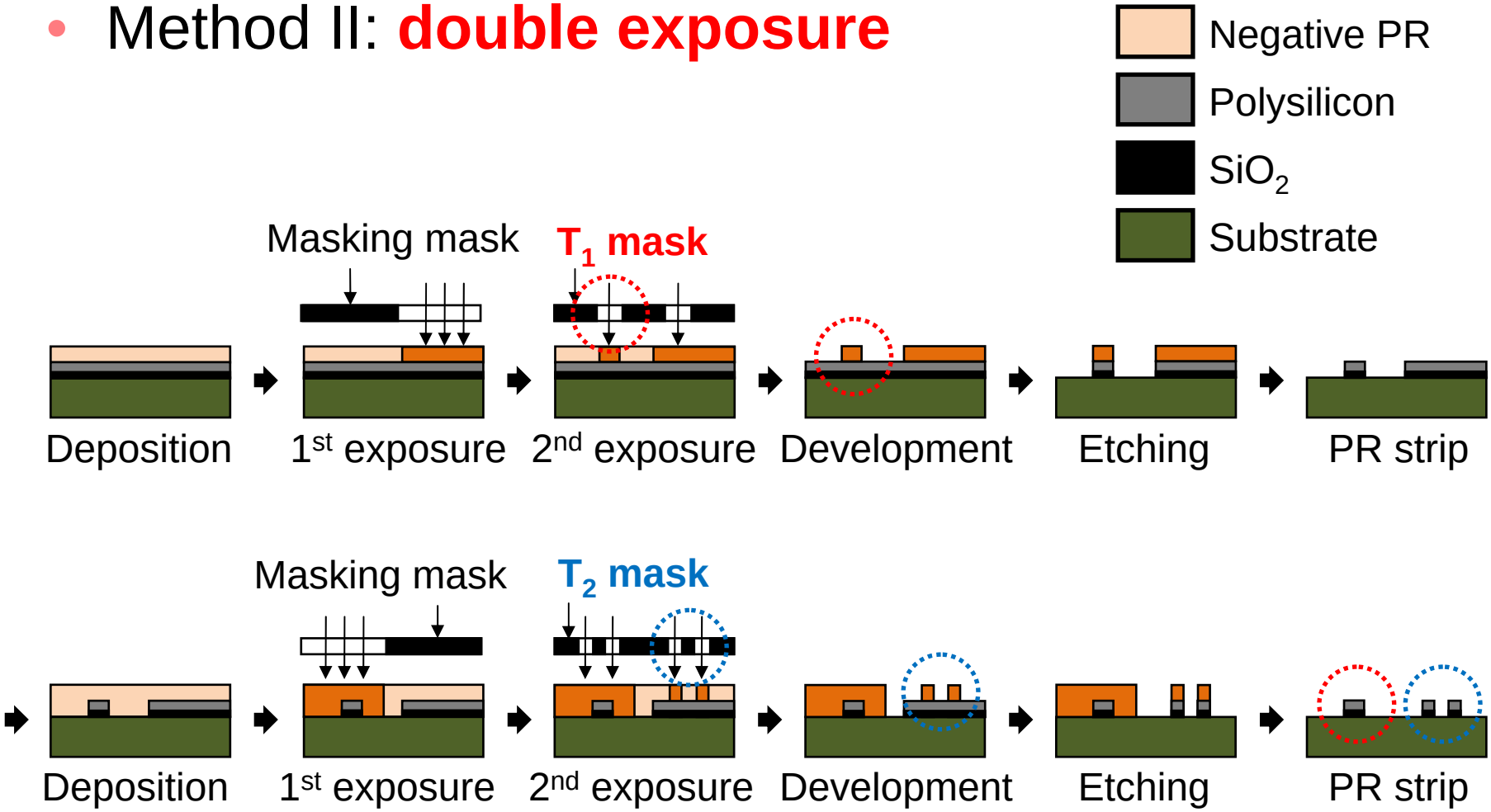
- How to selectively pattern? Method I: tile and masking masks together during lithography

- **But, practical limitation...**
  - Current lithography equipment does not support
  - Light through two masks become weaker



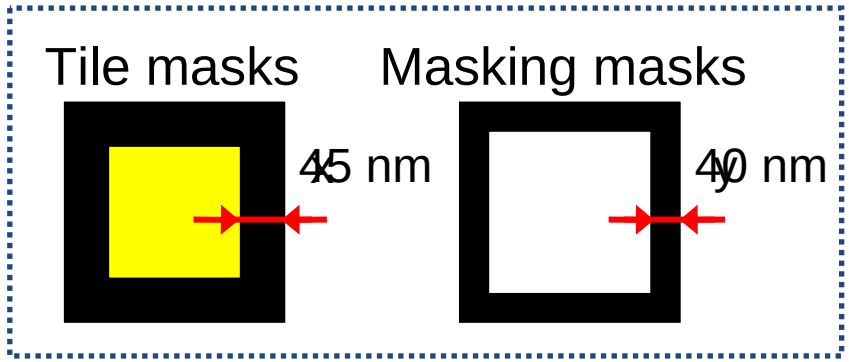
Selectively Patterned Masks (SPM)

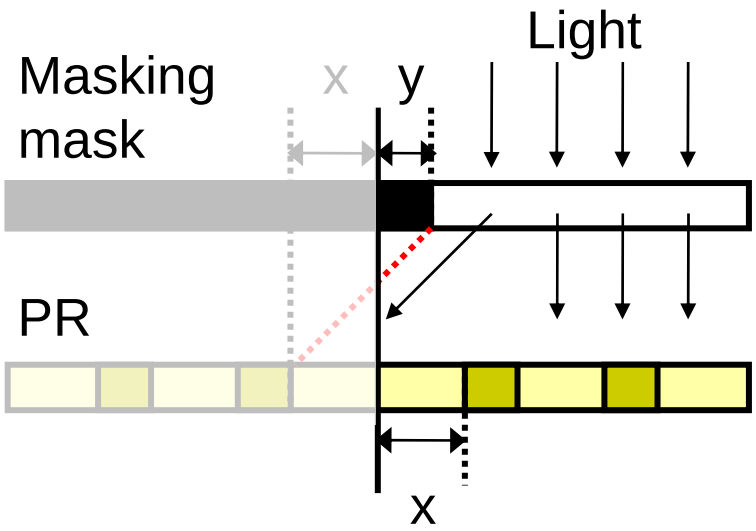
- Method II: **double exposure**



Mask Design in Double Exposure

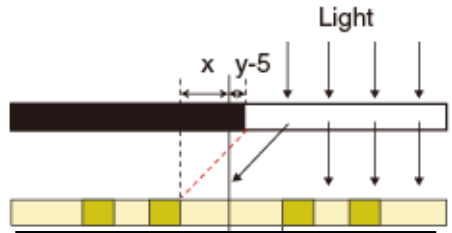
- **Boundary margin** to accommodate
  - Light diffraction
  - Mask misalignment





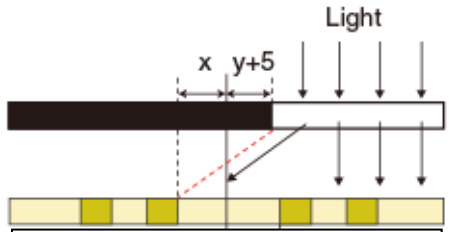
$x \geq y,\ x + y \geq 80$

Misalignment to the left



$x \geq y - 5,\ x + y - 5 \geq 80$

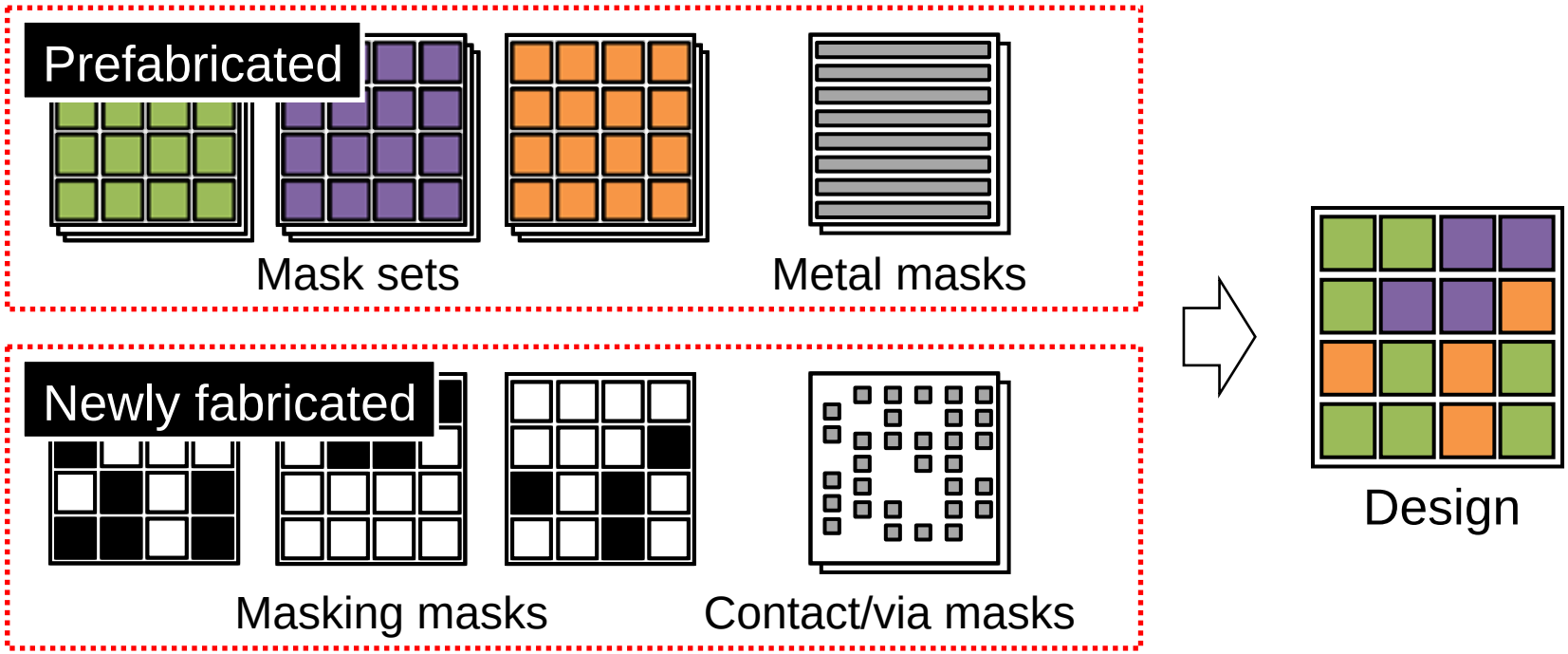
Misalignment to the right



$x \geq y + 5,\ x + y + 5 \geq 80$

Structured ASIC Using SPM

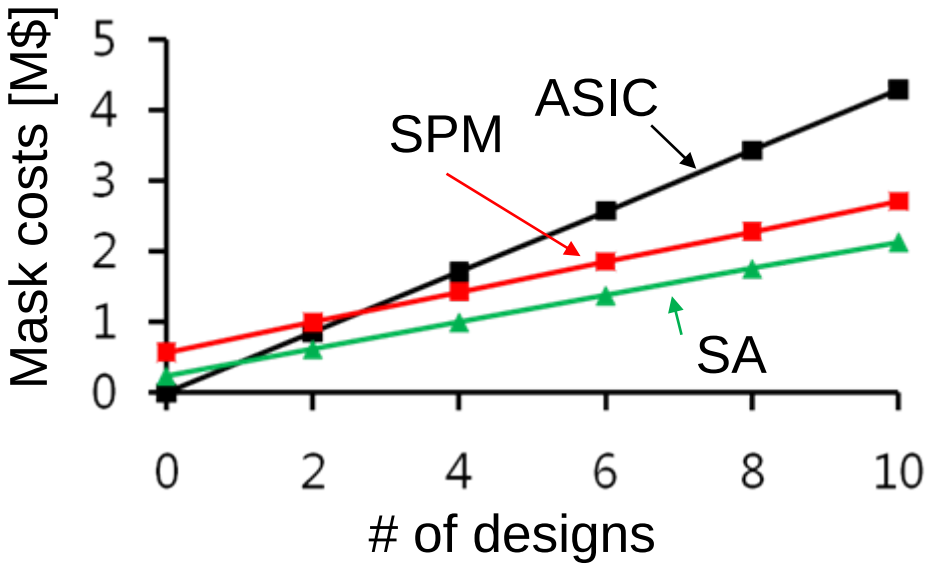
- **Mask sets, metal masks**: pre-fabricated
- **Contact/via masks**: fabricated for each design, used to program tiles & make connection
- **Masking masks**: fabricated for each design, but cheap



Analysis of Mask Cost

- Cost model is similar to that of standard SA

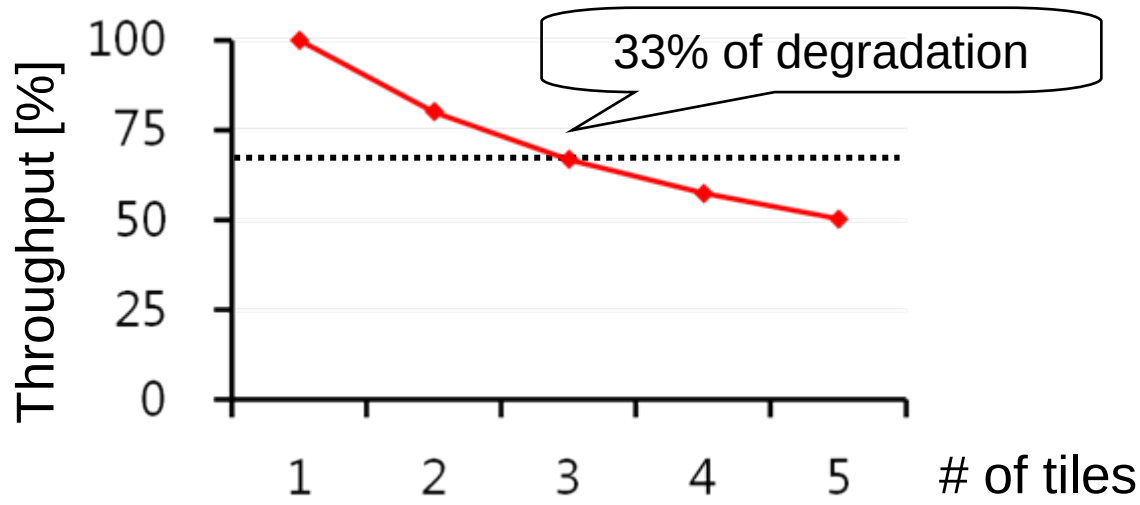
	Pre-fabricated	Newly fabricated
ASIC		All masks
Standard SA	One tile mask set	Contact & via masks
SA with SPM	Multiple tile mask sets	Contact & via masks + Masking masks



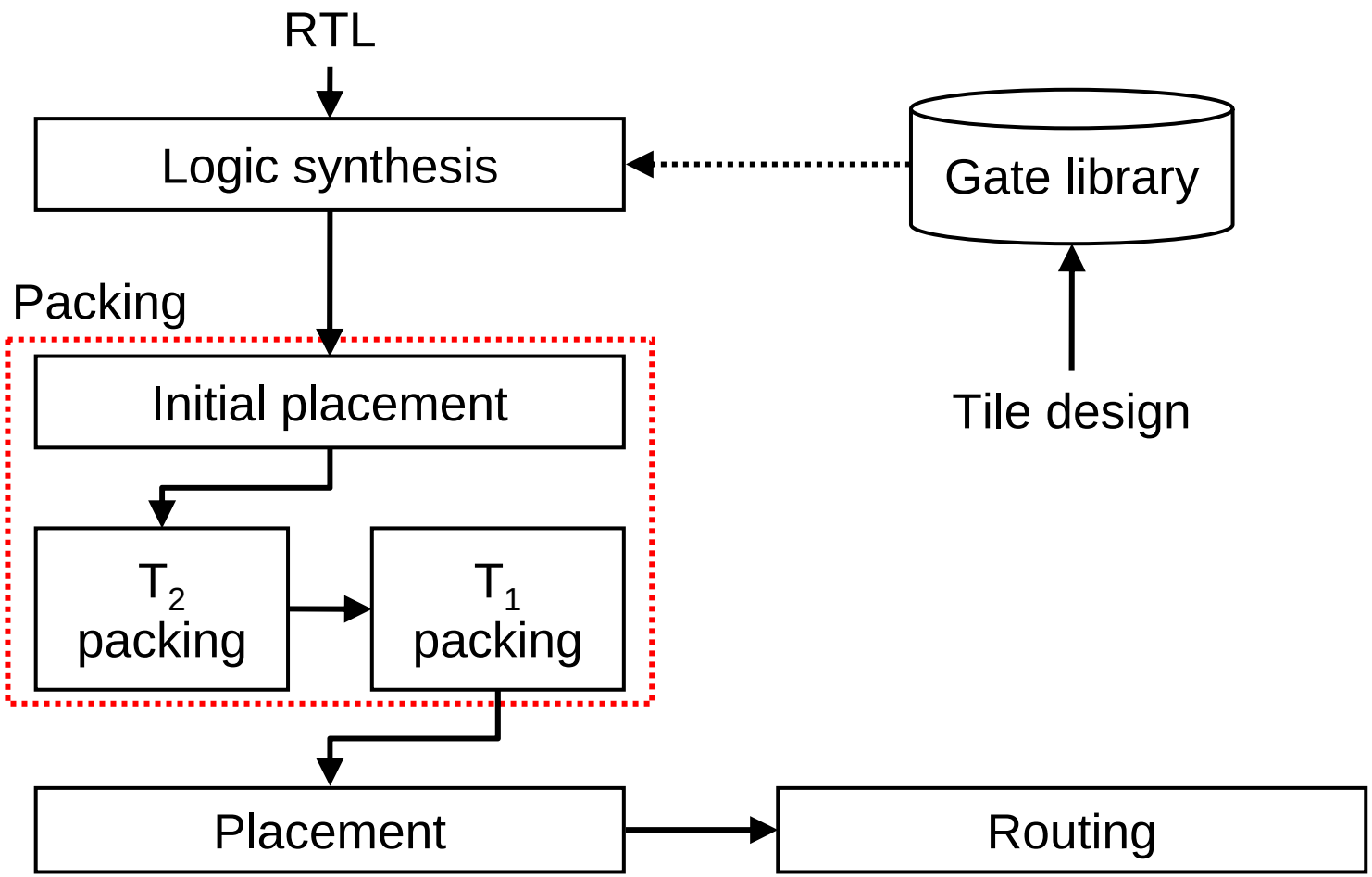
Analysis of Manufacturing Throughput

- Use of masking masks and multiple tiles increase manufacturing time

	Exposure	Etching
Standard patterning	One time	One time
Selective patterning	# of tiles × 2	# of tiles

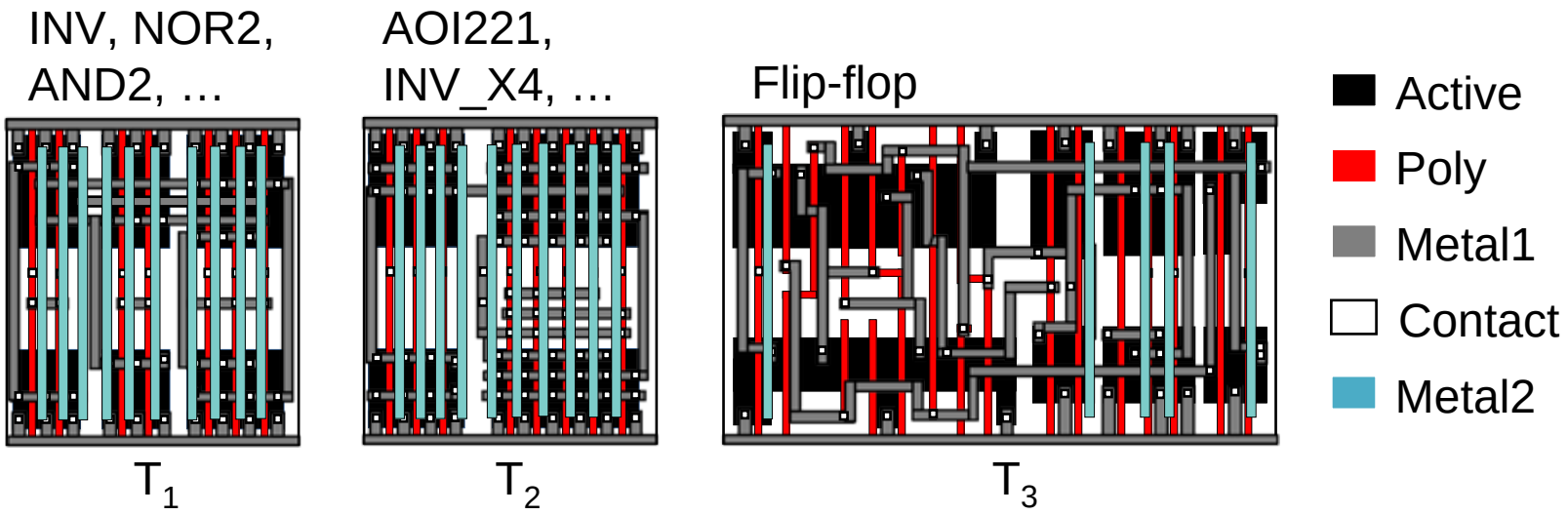


Structured ASIC Using SPM



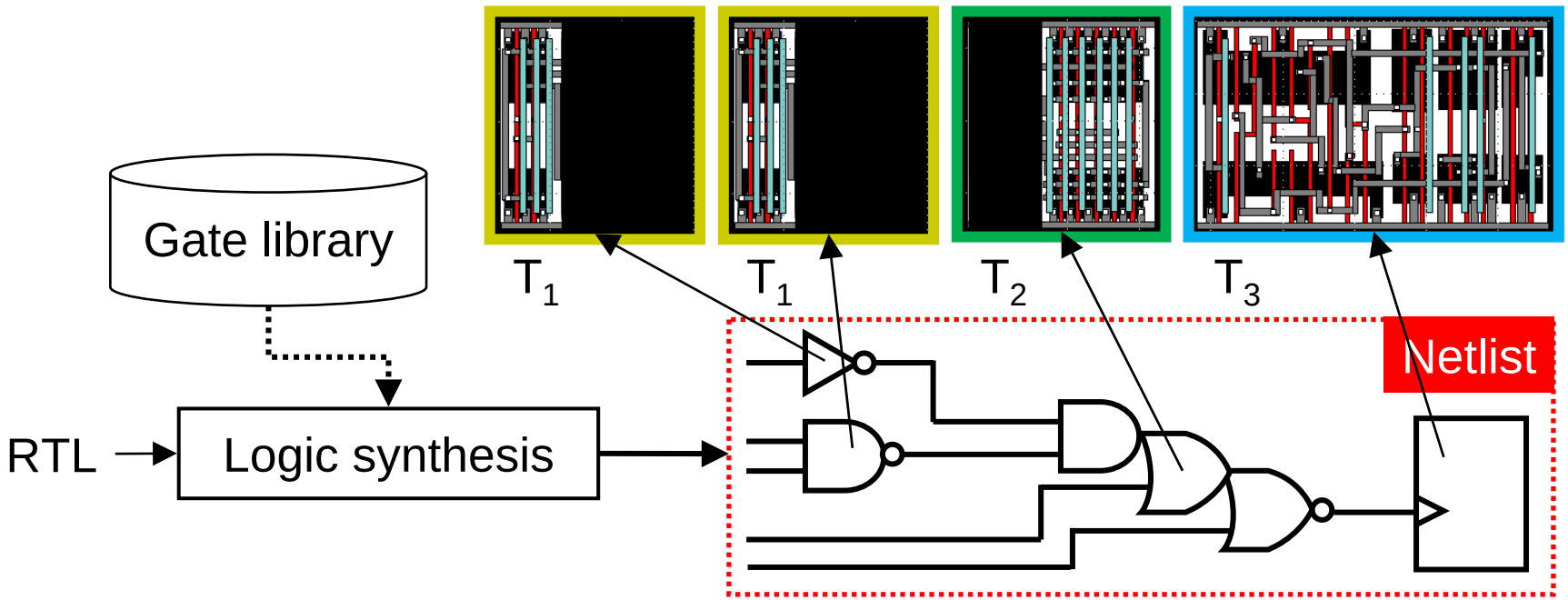
Tile Design

- Three tile architectures
  - T_1: three basic logic gates
  - T_2: two complex gates
  - T_3: F/F (with set/reset)



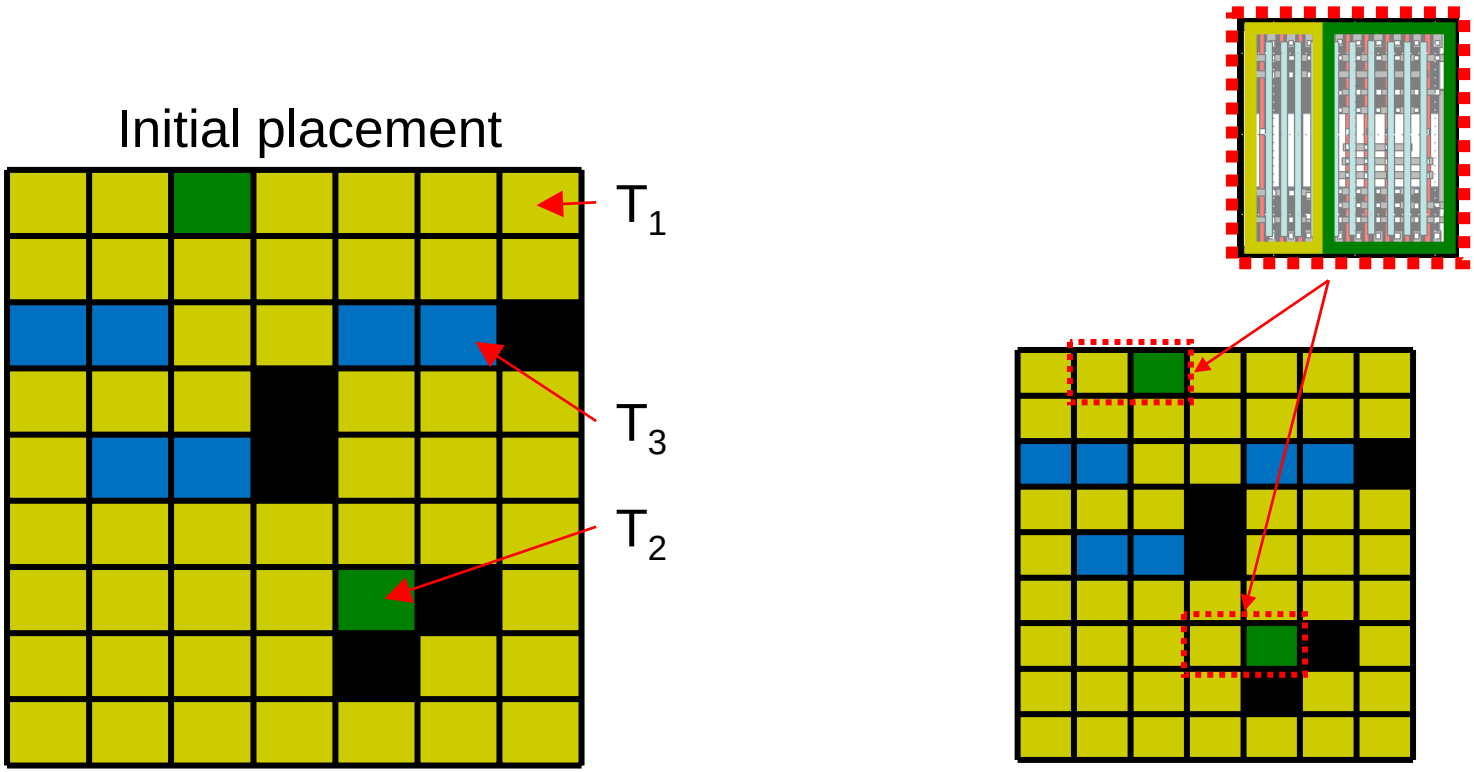
Logic Synthesis

- **Gate library**: models each “gate” (NOT tile)
- **Logic synthesis**
  1. Initial netlist is made such that each gate occupies one tile



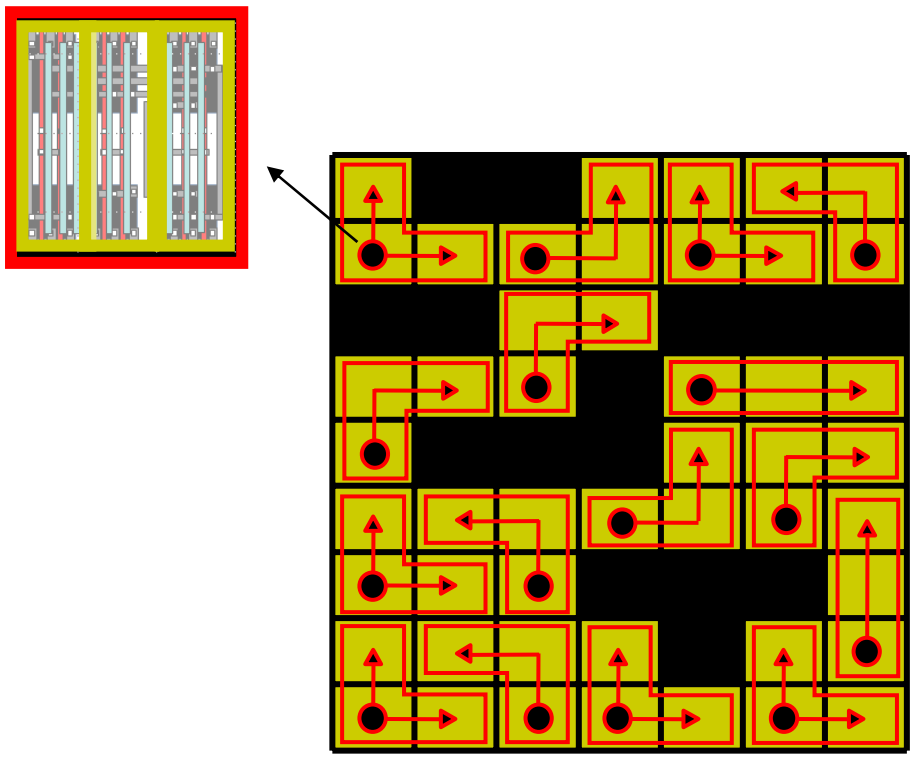
Logic Synthesis

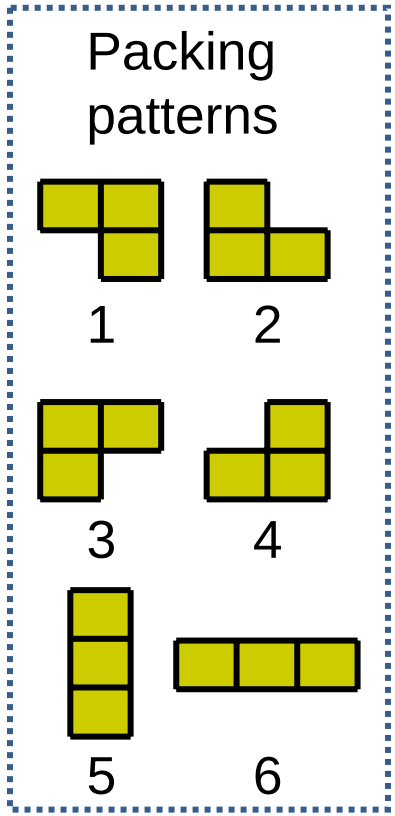
2. Initial placement
3. Locate T2 → merge with nearest T1



Logic Synthesis

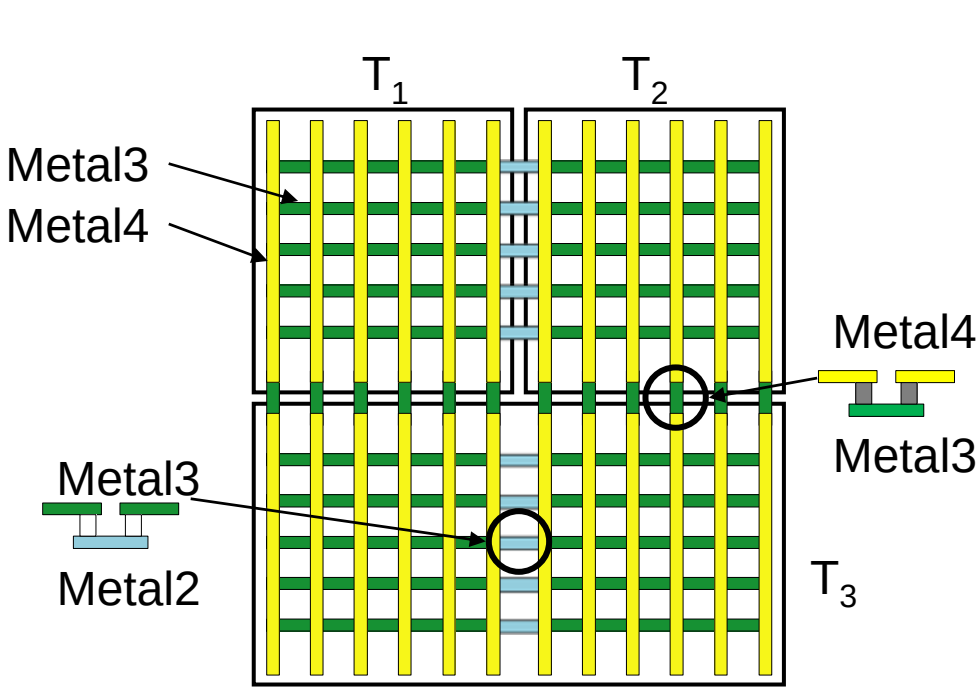
4. Merge adjacent “three” T_1s ← scan tiles from bottom-left to upper-right of placement

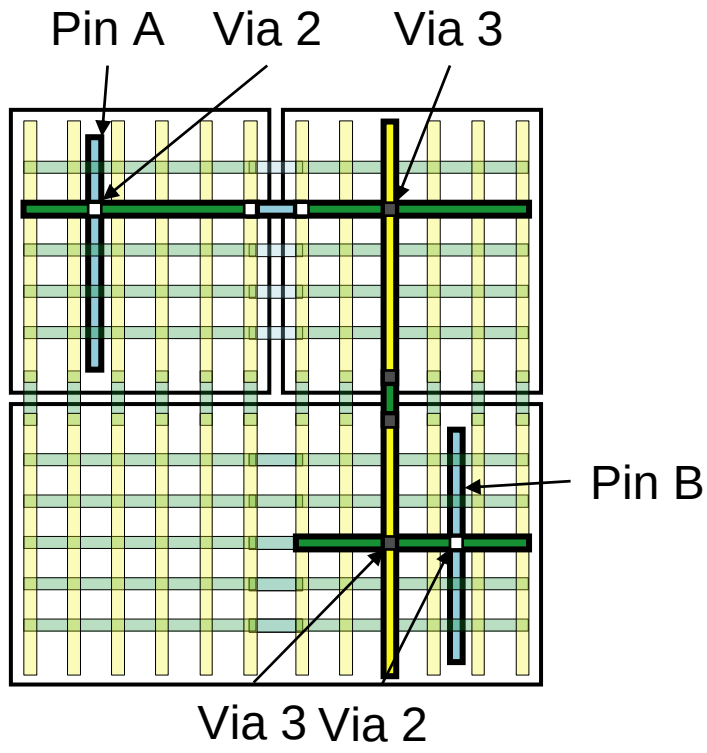




Routing Architecture

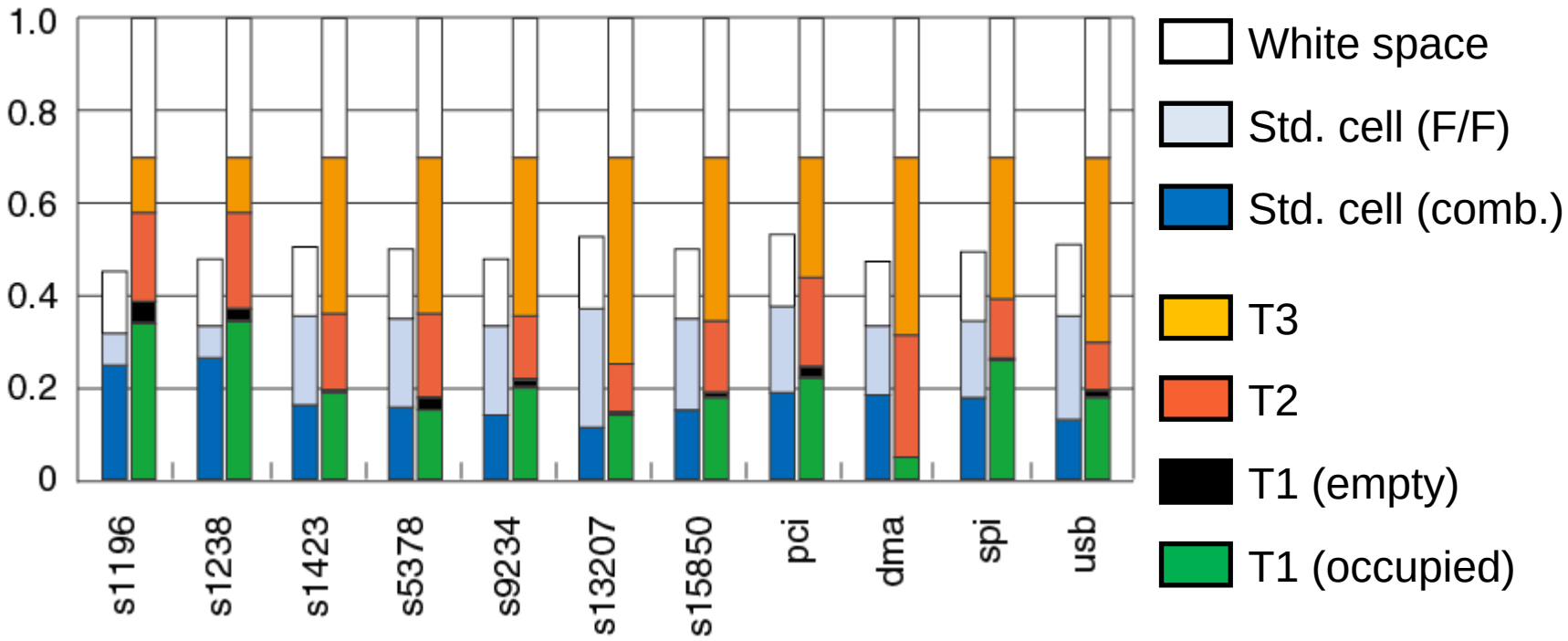
- **A grid** (made of M3+M4) is placed on top of each tile (two grids for T3)
- Programmable via is used for inter-tile connection





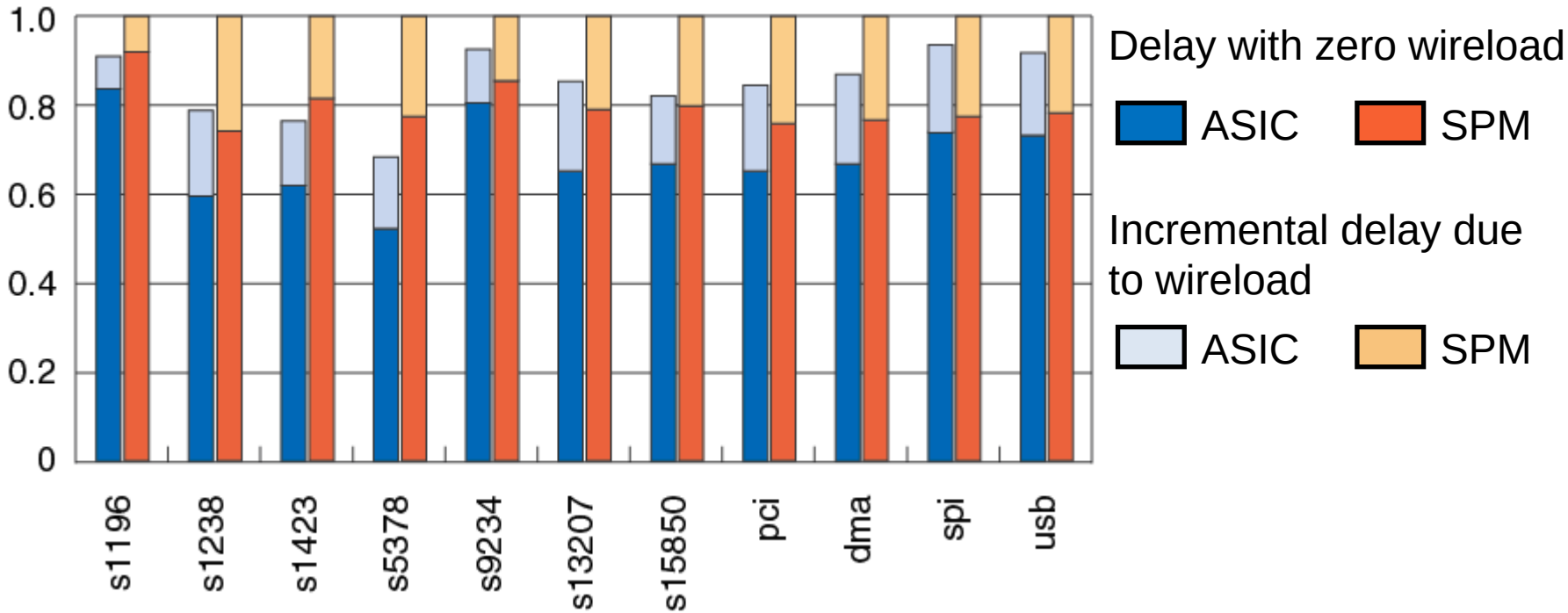
Experimental Results

- Area-optimized design
  - SPM/ASIC = 2 ↔ 3 ~ 7 in conventional SA
  - Why area increases? → tile height & tile utilization



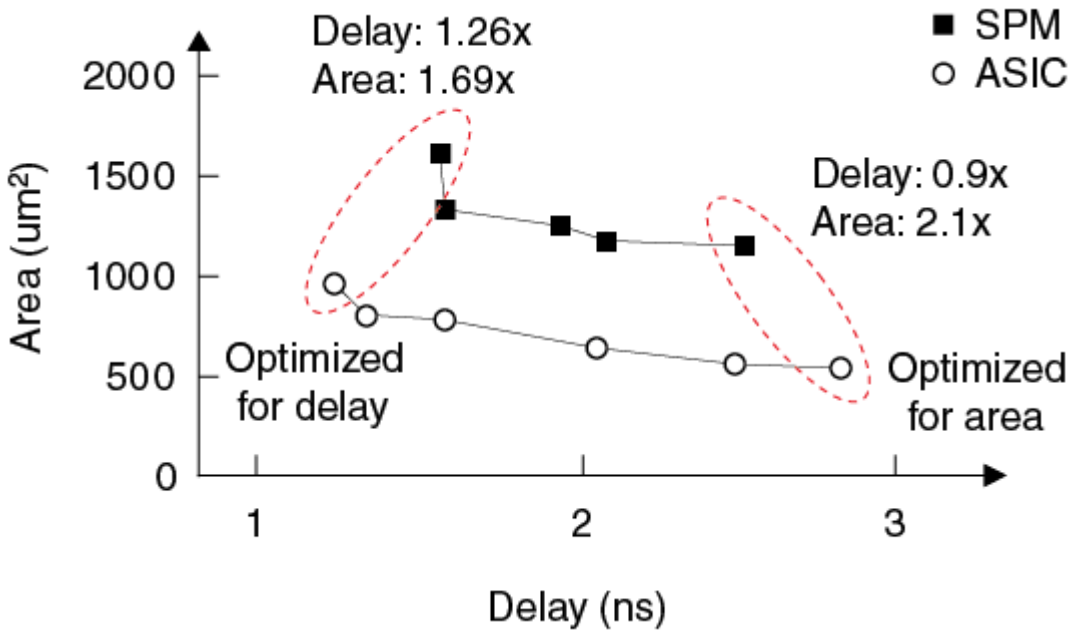
Experimental Results

- Delay-optimized design
  - SPM/ASIC = 1.2 ↔ 2 ~ 4 in conventional SA
  - Why delay increases? → lack of gates & routing arch.



Experimental Results

- Design space (area vs. delay curve)
  - Delay opt. → SPM/ASIC = 1.26 (delay), 1.69 (area)
  - Area opt. → SPM/ASIC = 0.9 (delay), 2.1 (area)
  - Why large gap occur? → lack of gates & tile regularity



Conclusion

- Current structured ASIC (SA)
  - Performance limited due to “regularity”
- SPM
  - Allows “irregular” structured ASIC with similar mask cost as SA
  - Prototype SA using SPM was demonstrated
- Future works
  - Logic synthesis
  - Routing algorithm