



A Resilient Router Design Through Data Path Salvaging

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Outline

- Background
- Motivation
- Resilient NoC Design
- Experiments

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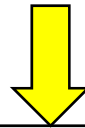
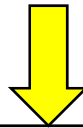
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Reliability Challenge

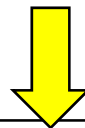
Technique keeps
on scaling down.

The chip is
getting larger.

Applications requires
more powerful chip.



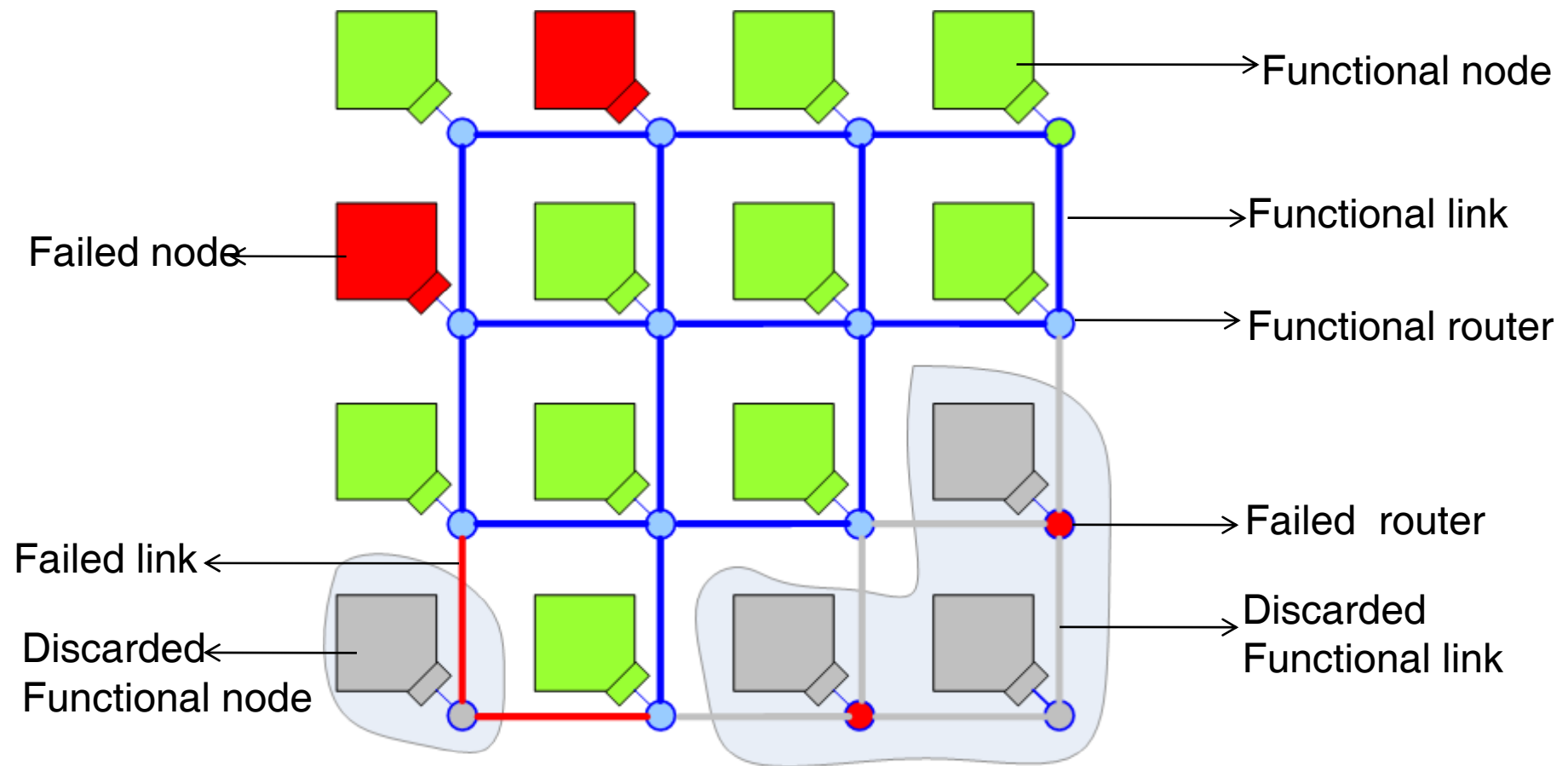
There are more transistors on a single chip.



Manufacture defect increases.
Wear-out appears frequently.



NoC Reliability Influence on a SoC



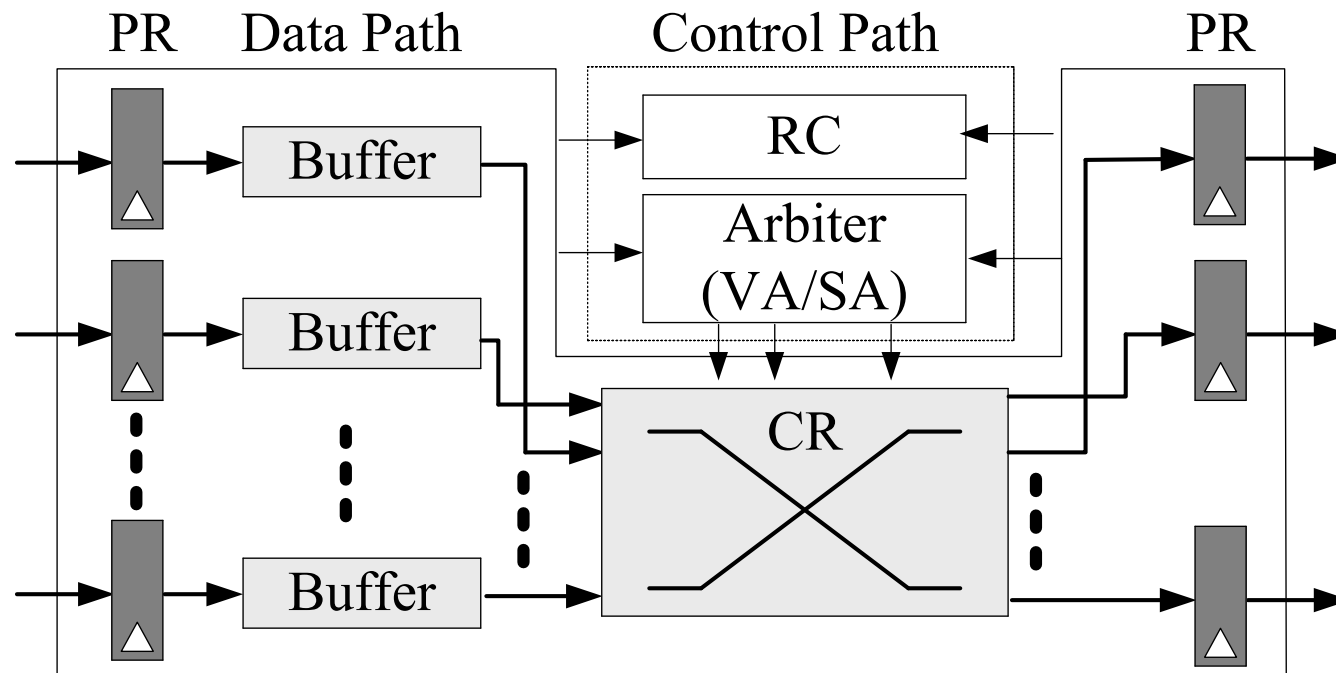
Related work

- Vicis: A Reliable Network for Unreliable Silicon [Fick09]
 - Port swapping, ECC, fault tolerance routing algorithm
- A Lightweight Fault-Tolerant Mechanism for Network-on-Chip [Koibuchi 08]
 - Default bypass backup
- Bulletproof: A defect-tolerant CMP switch architecture [Constantinides 06]
 - Redundancy and share

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Conventional Router Architecture



NoC Area Breakdown

Fault rate p , Component area A

$$A \rightarrow p$$

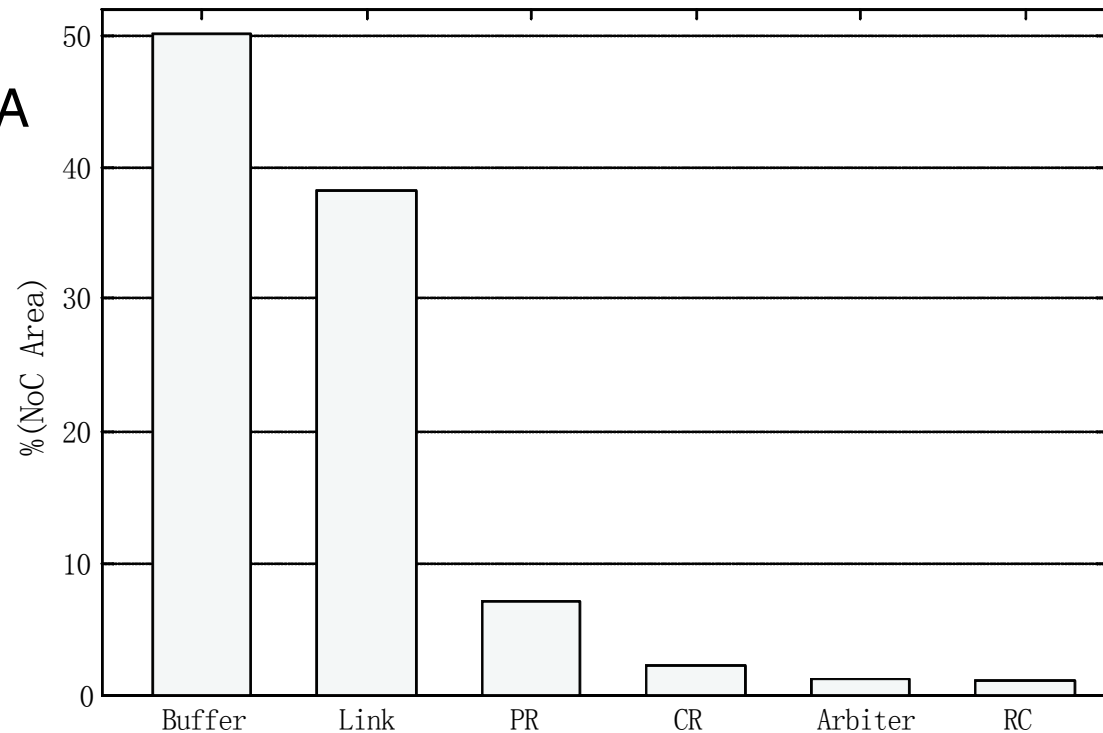
$$2A \rightarrow 1-(1-p)^2 \approx 1-(1-2p)=2p$$

.

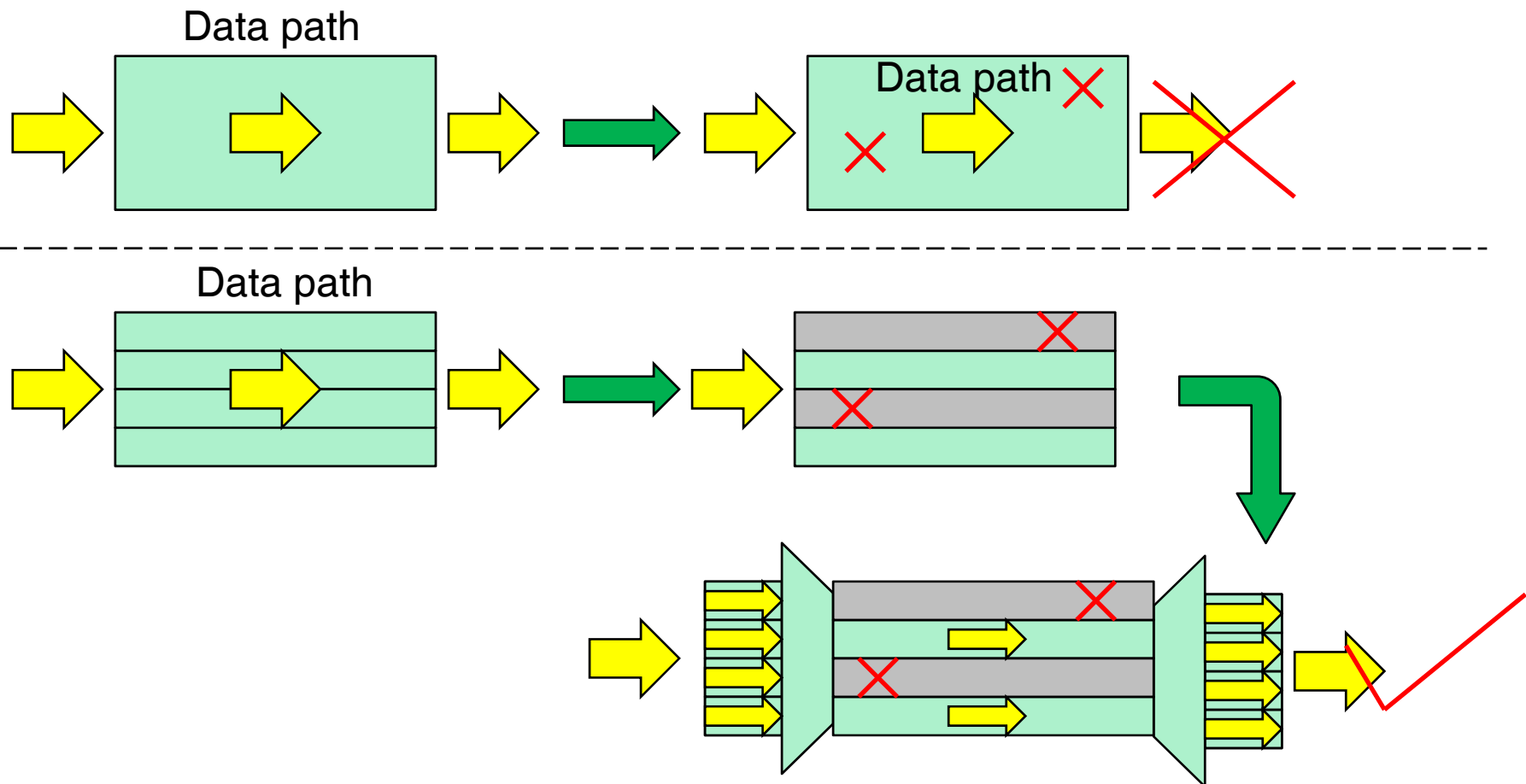
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$$nA \rightarrow 1-(1-p)^n \approx 1-(1-np)=np$$



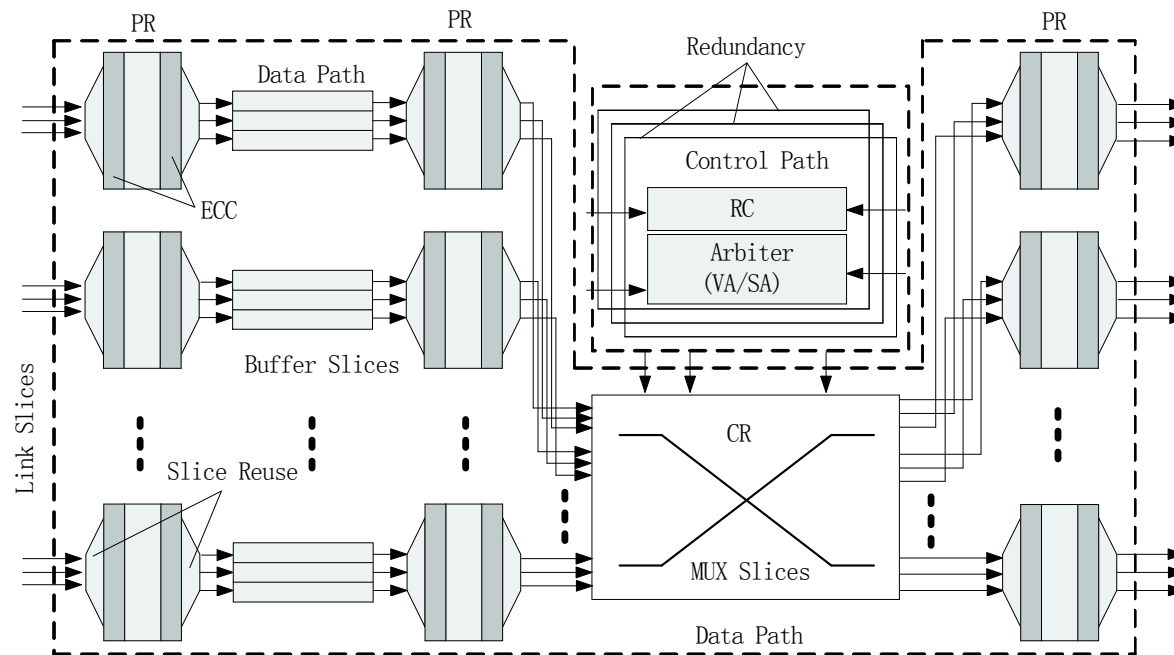
Data Path Slice Reuse



Outline

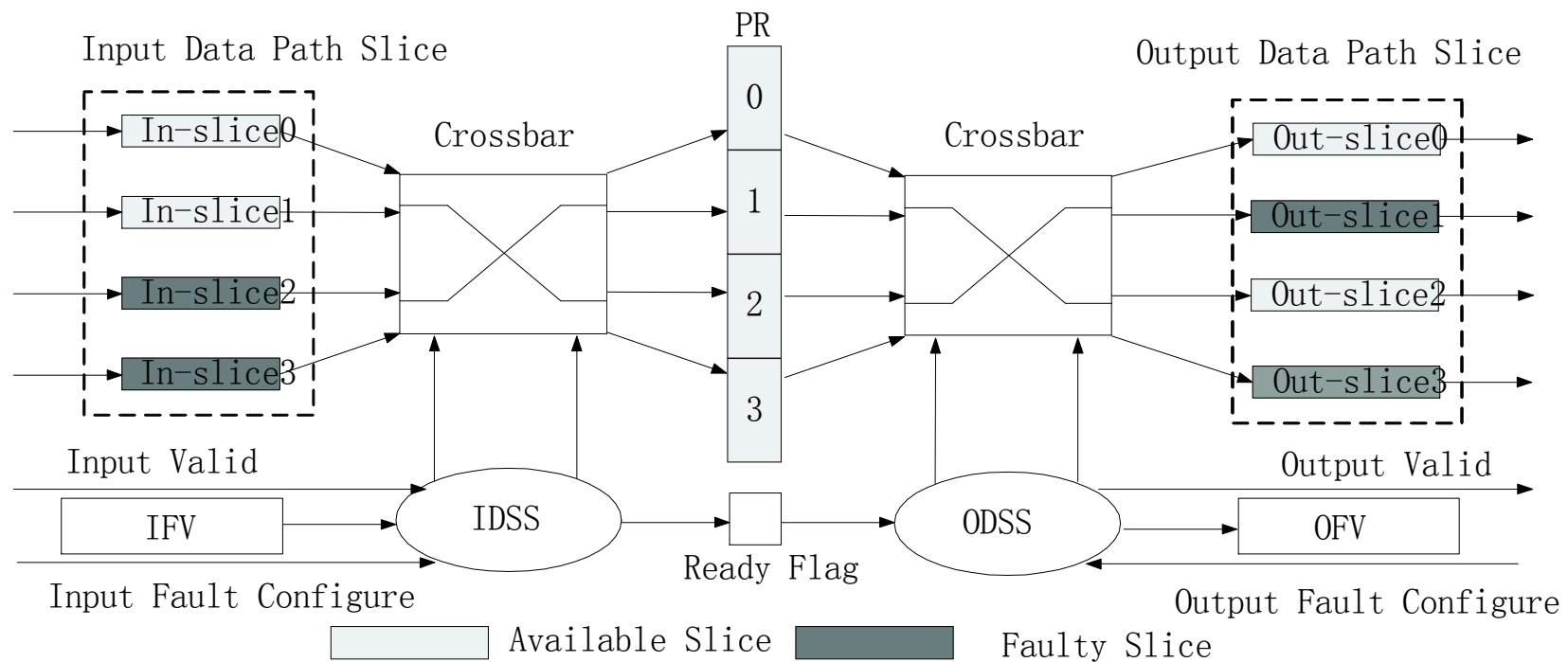
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Resilient NoC Design Scheme

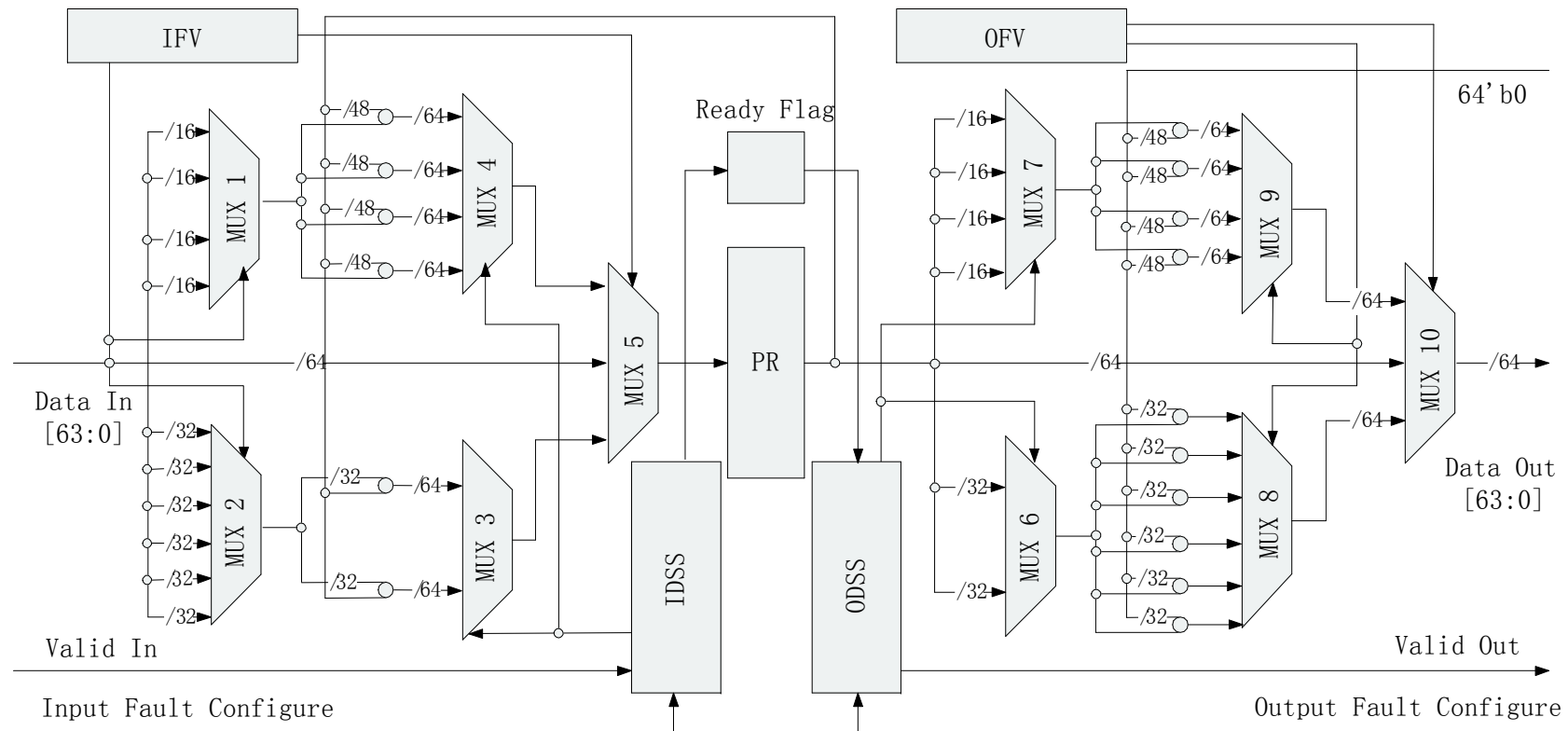


Module	RC	PR	Arbiter	CR	Buffer	Link
Area	Small	Medium	Small	Medium	Large	Large
Method	Redundancy	ECC	Redundancy	Slice Reuse	Slice Reuse	Slice Reuse

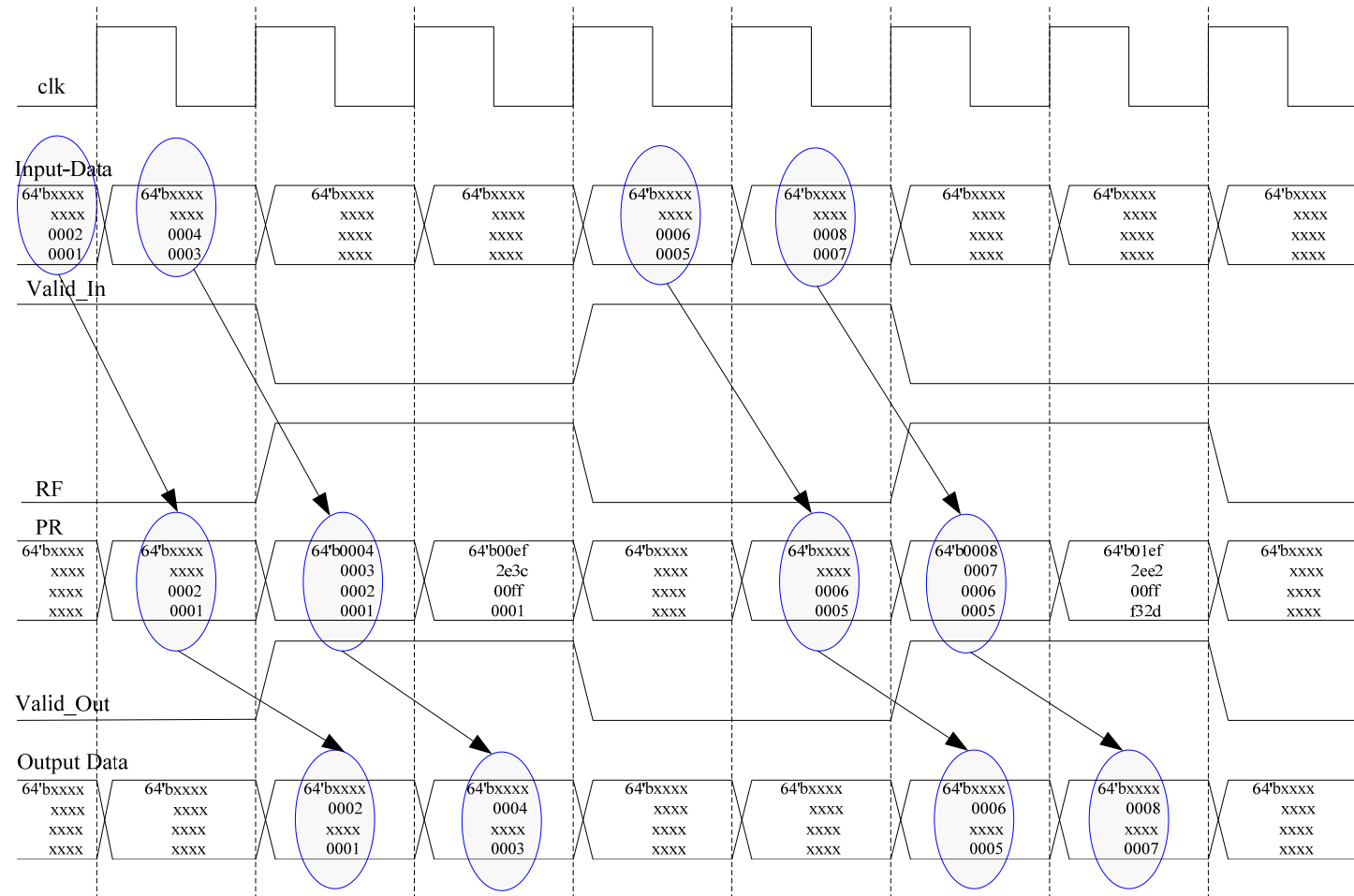
Slice Reuse Principle



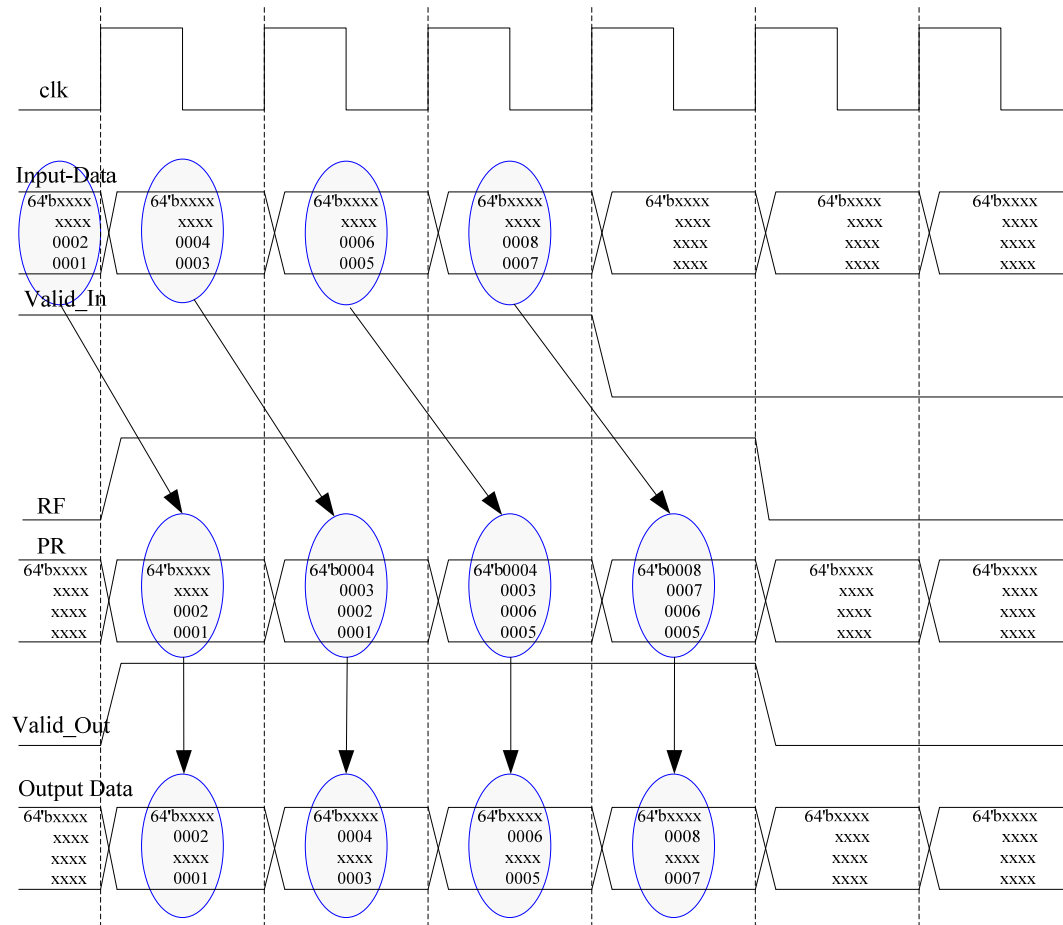
Slice Reuse Structure



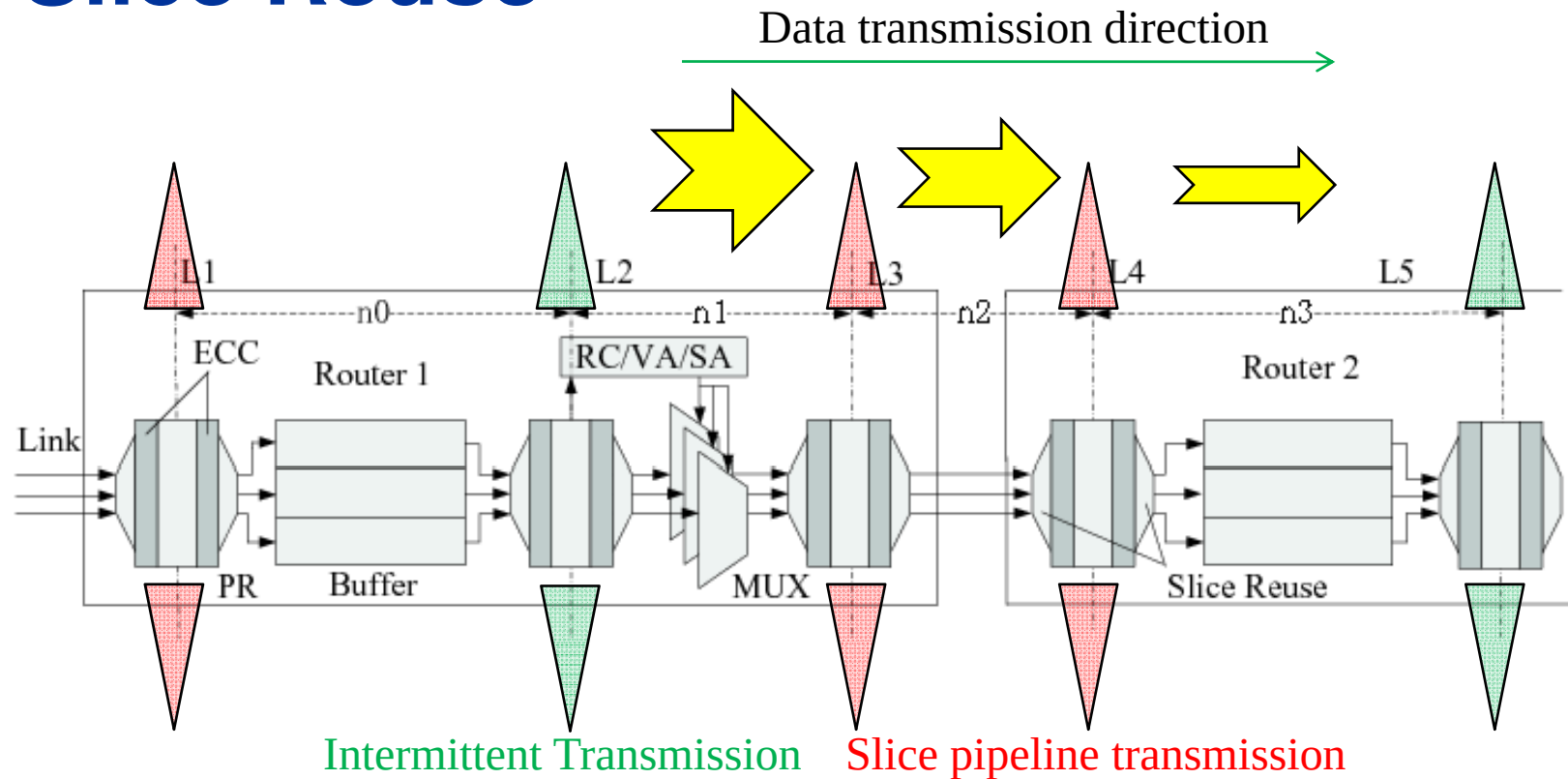
Intermittent Transmission



Slice Pipeline Transmission



Slice Reuse

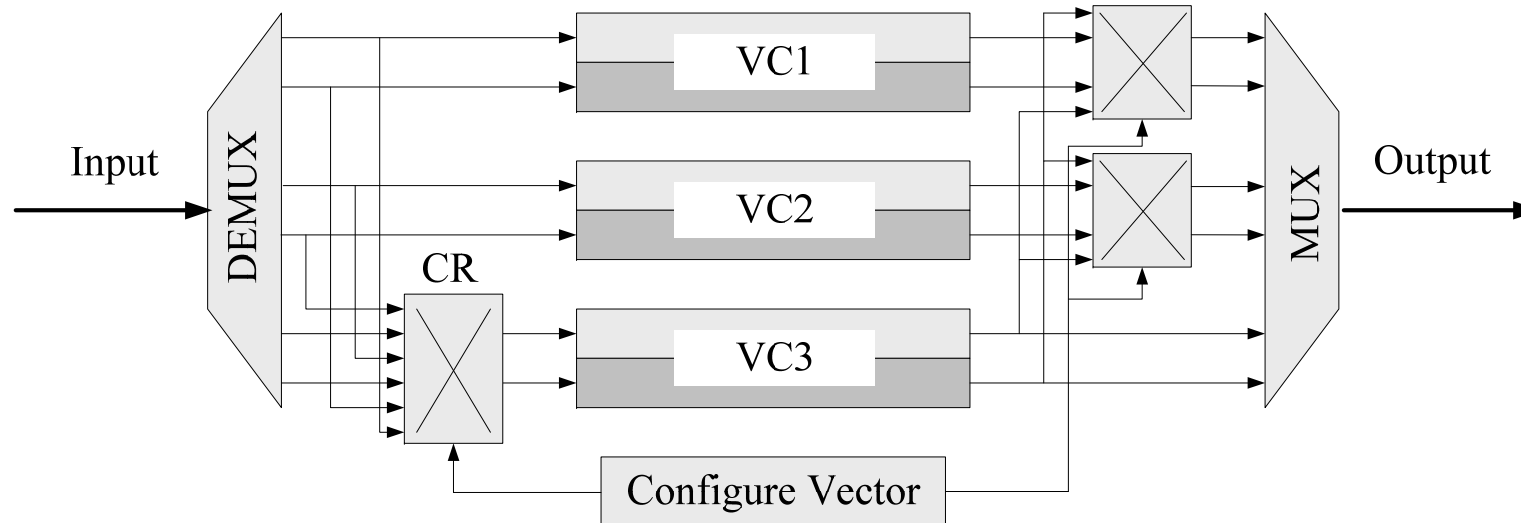


Pipeline slices are correlated: $n1 \geq n2 \geq n3$

The correlations are limited: $n0 > n1$, $n0 = n1$, $n0 < n1$

The correlations are dynamic regarding to different pipelines

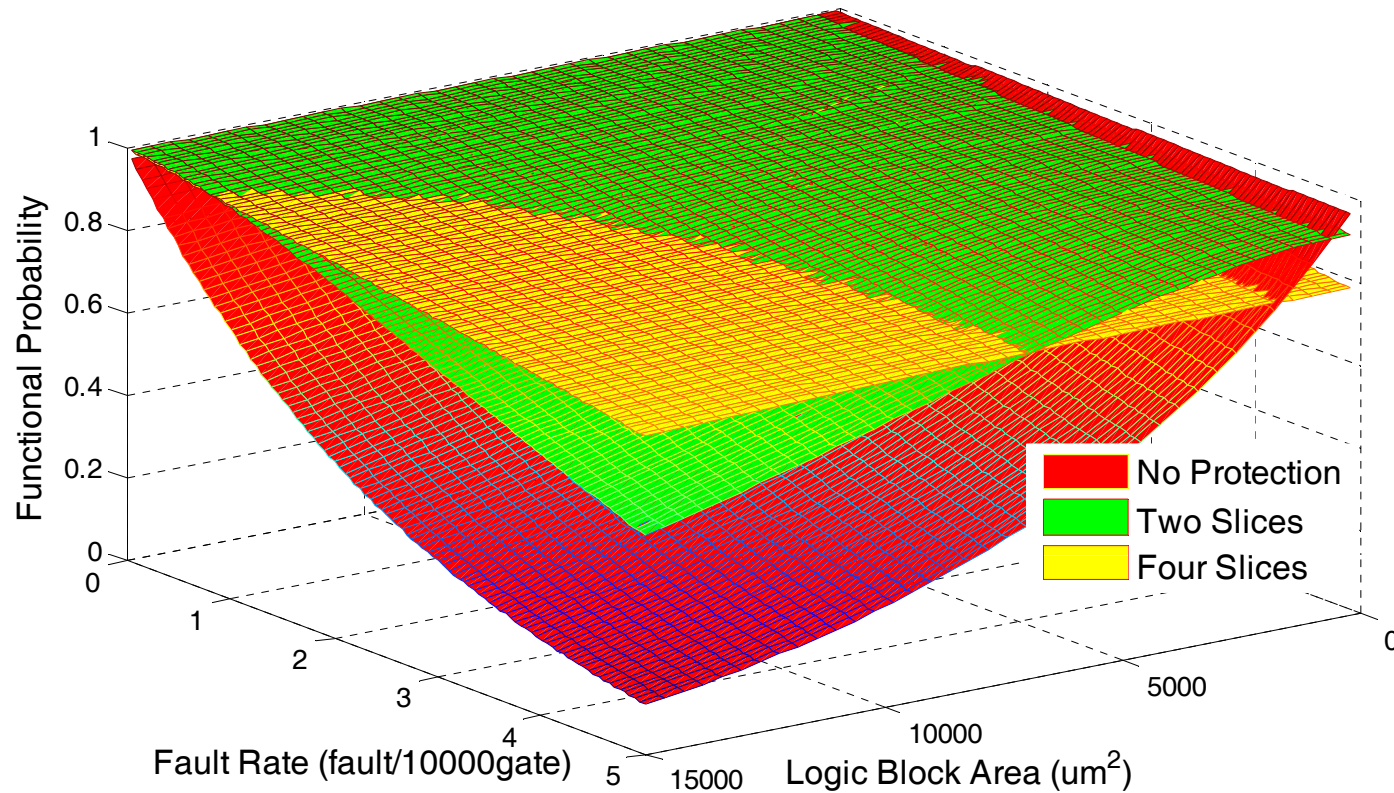
Extension to Virtual Channel Router



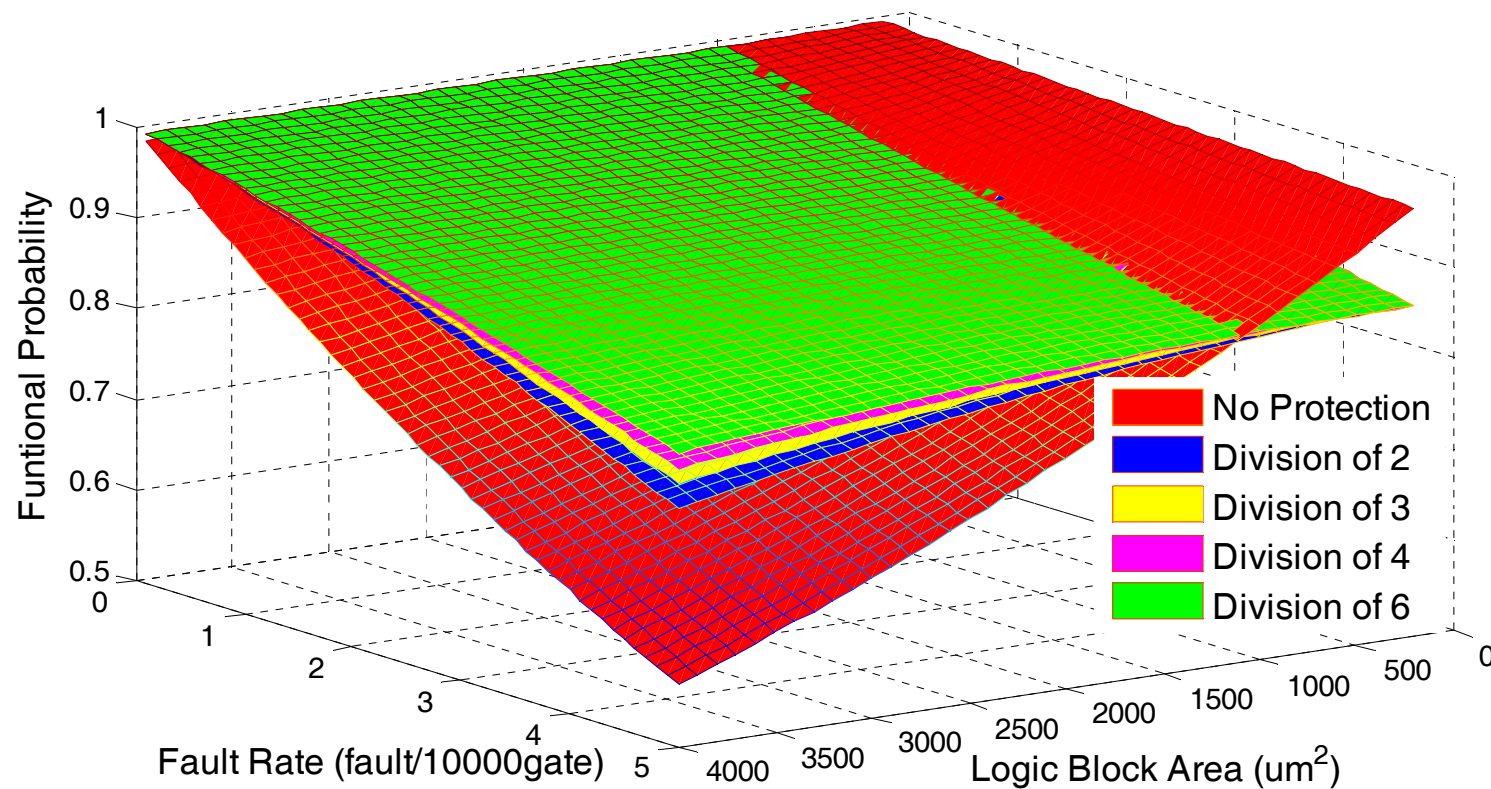
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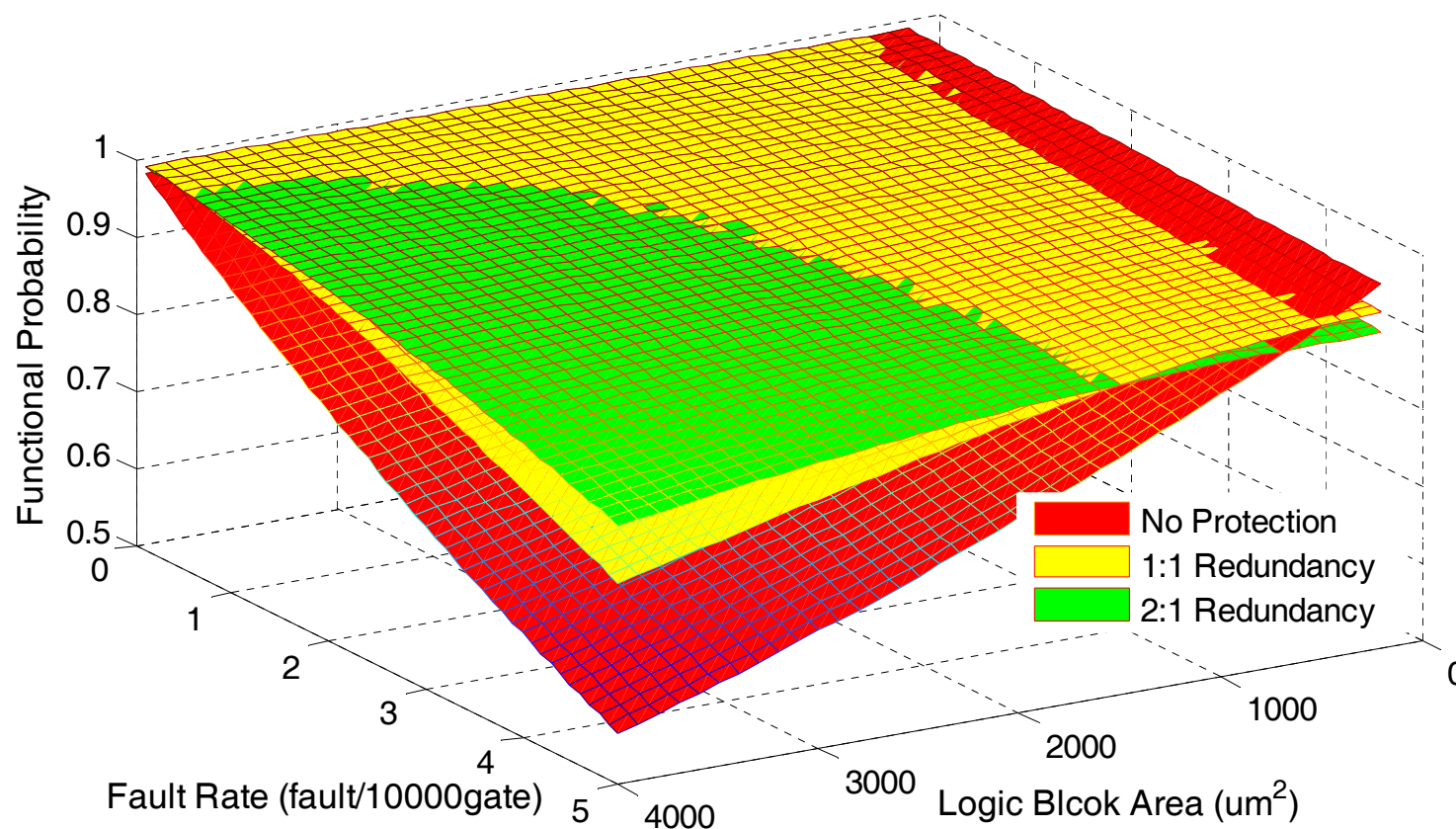
Design Choice (slice granularity)



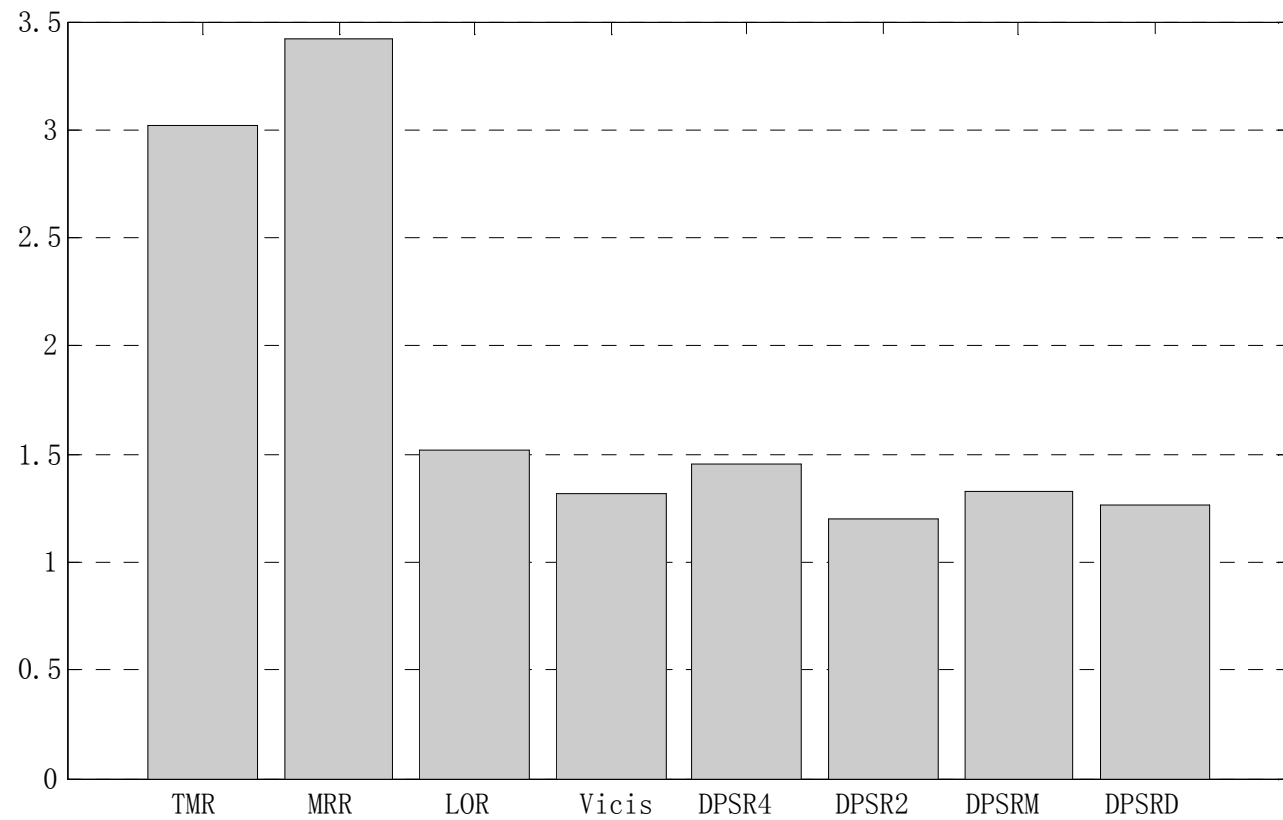
Design Choice (redundancy granularity)



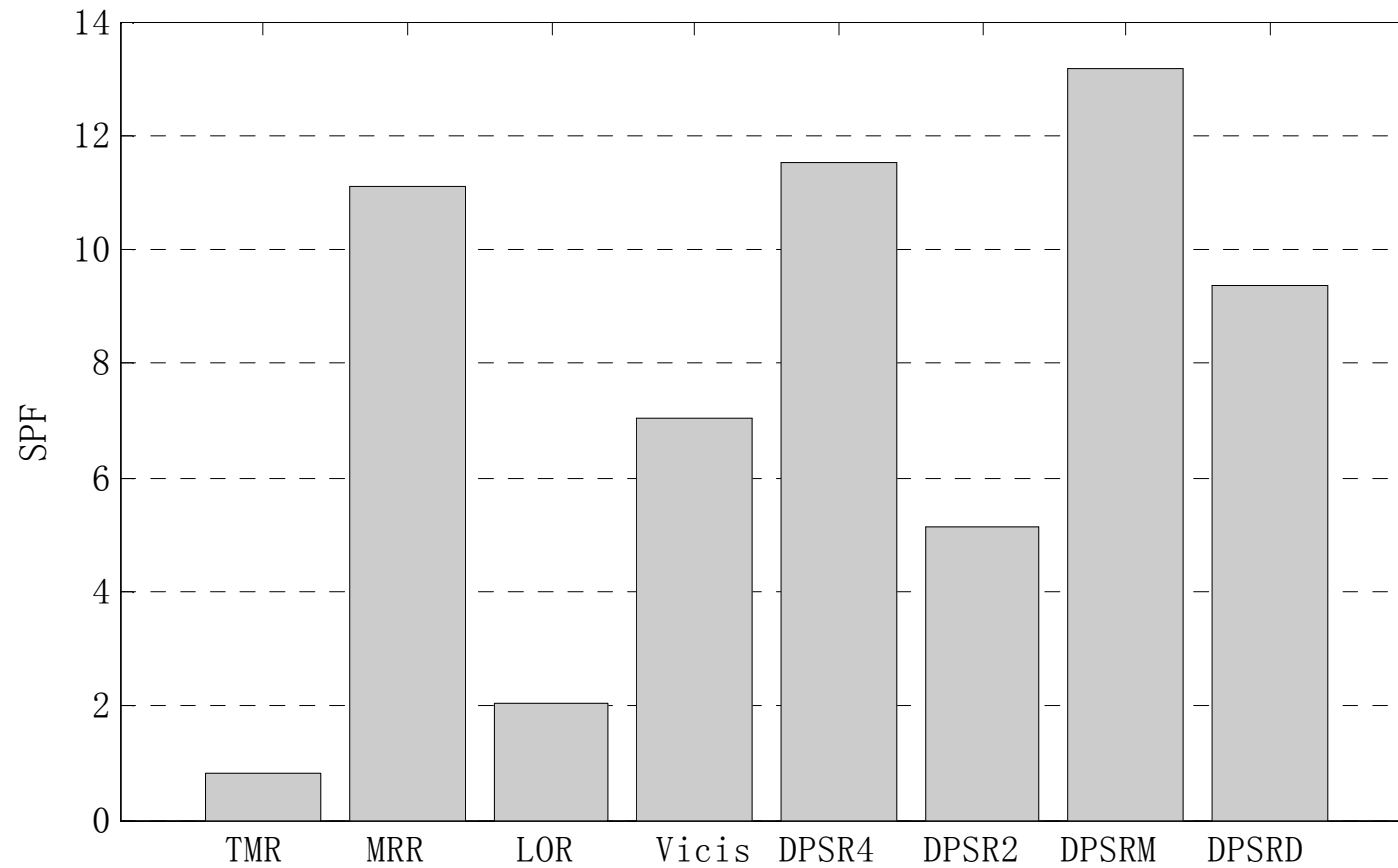
Design Choice (redundancy scale)



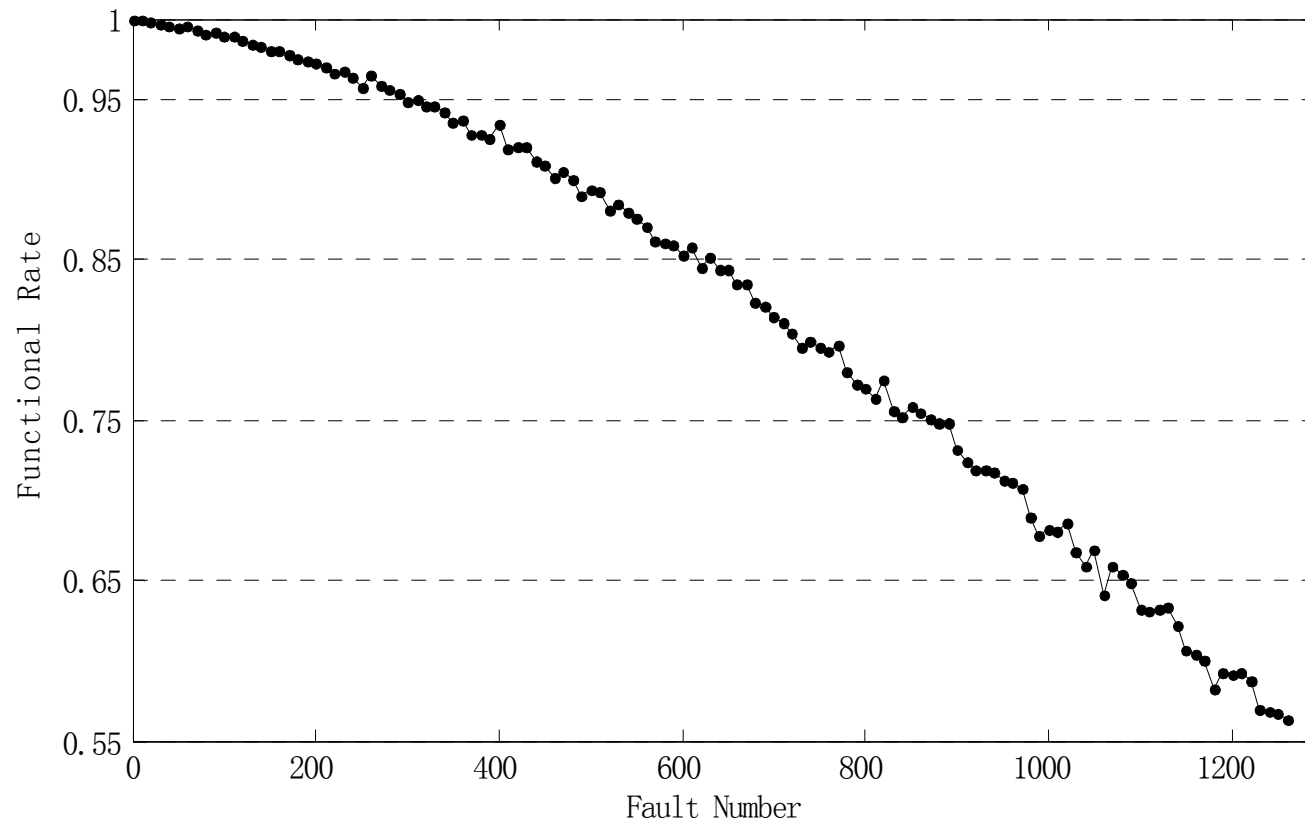
Area Overhead

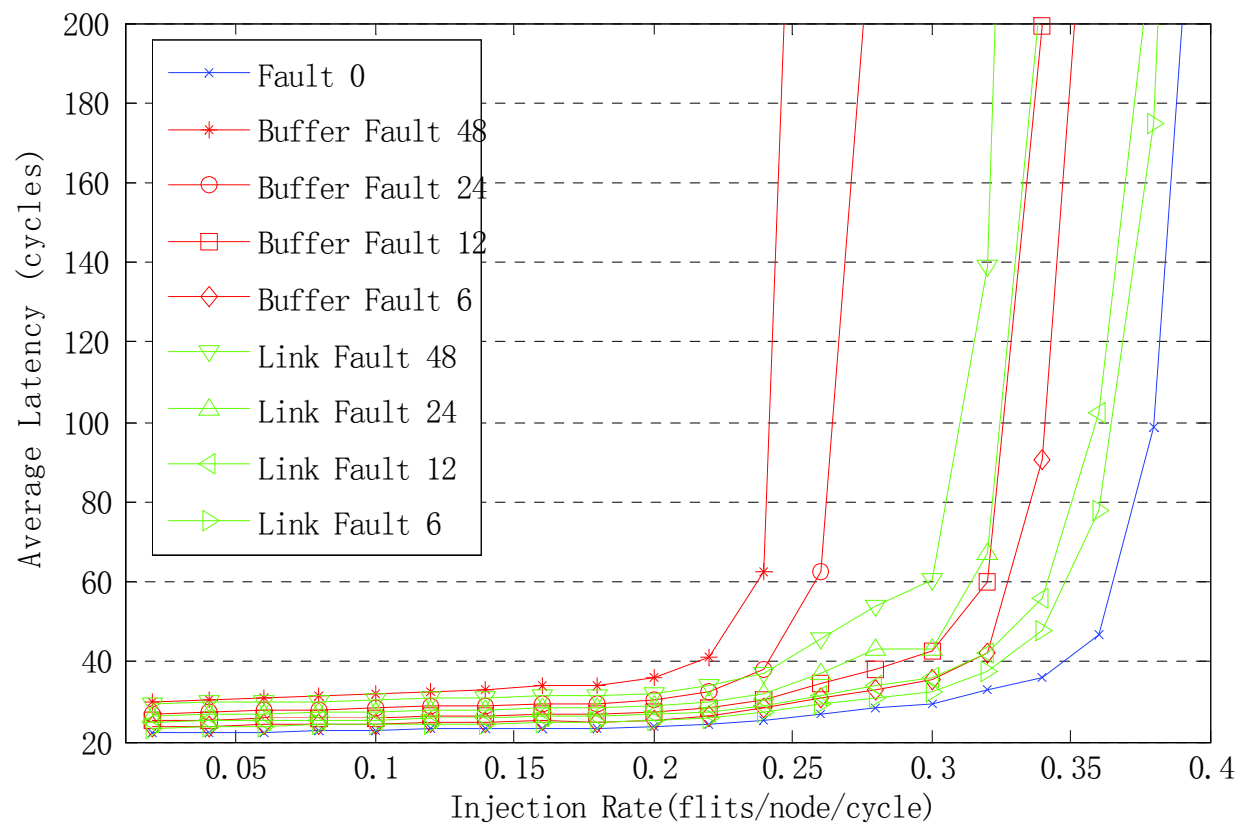


Reliability



Reliability

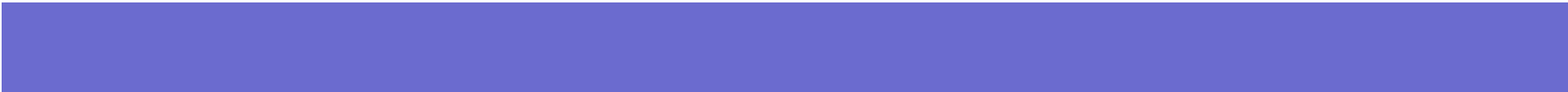






Questions?





Thanks!

