Chip-Package-Board Co-Design / Co-Verification Technology for DDR3 1.6G in Consumer Products

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Apache Design Solutions

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Apache DESIGN SOLUTIONS

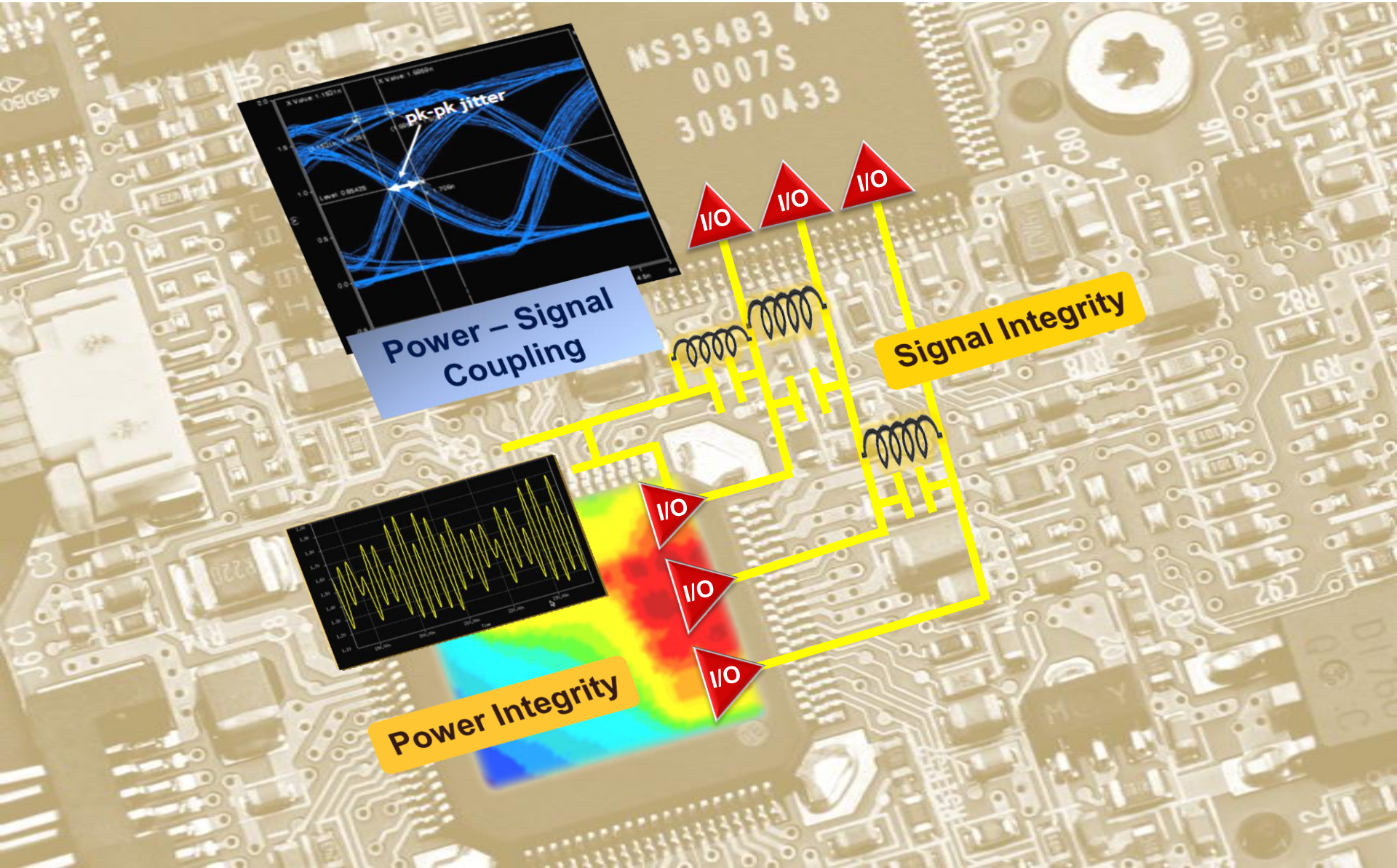
Agenda

- Challenges in DDR3 (consumer product)
- Key aspects of DDR3 C-P-B Co-verification
- View points of EDA tool provider

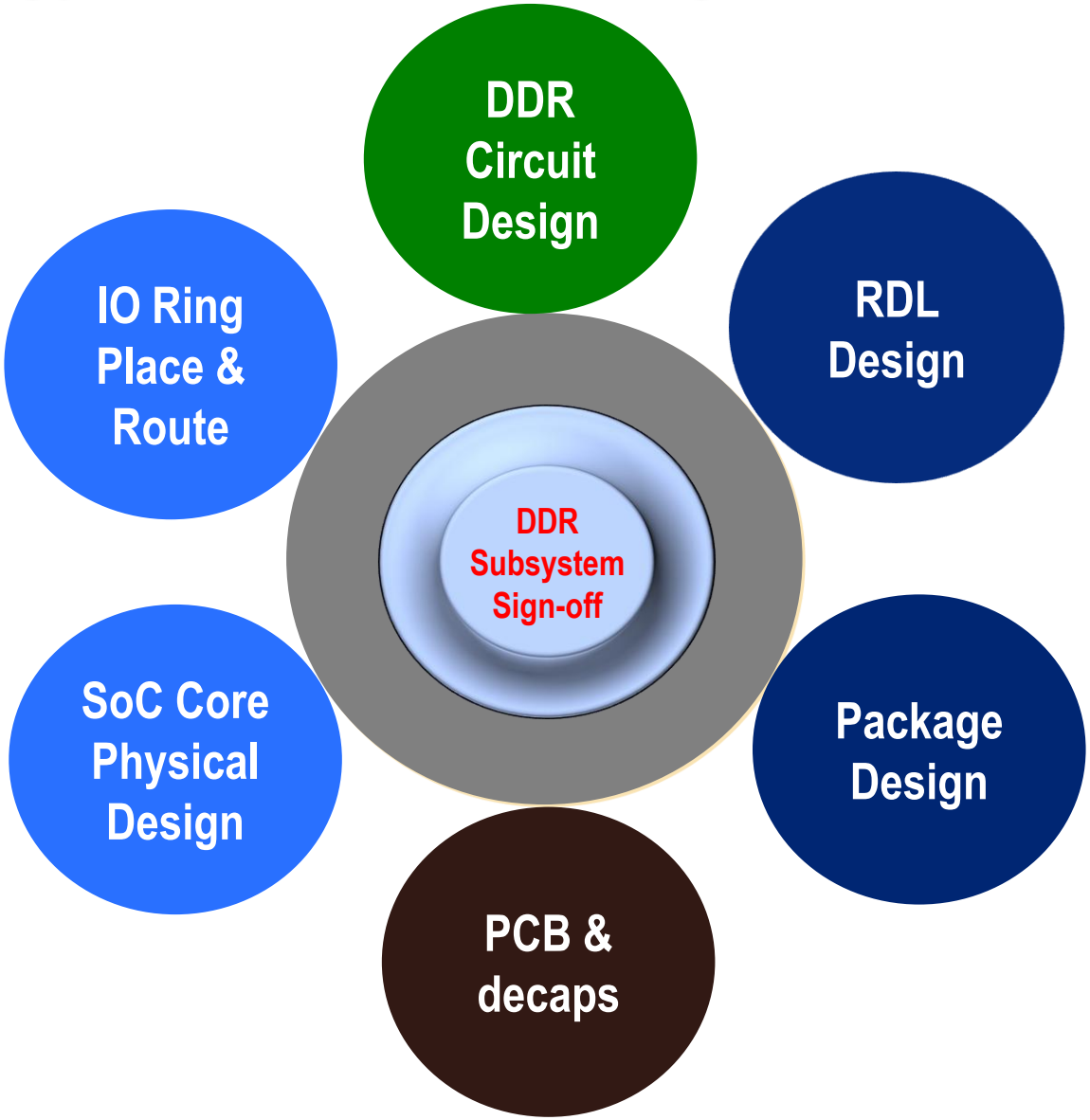
DDR3 1.6G Challenges

- Increased clock frequency and reduced voltage supply
- Tighter timing and noise budget
- Cost sensitivity (consumer products)
- Shortened time window for sign-off
- Debugging failure is more difficult

Chip-Package-Board View of DDR System



Ecology of DDR3 Co-Design / Co-Verification

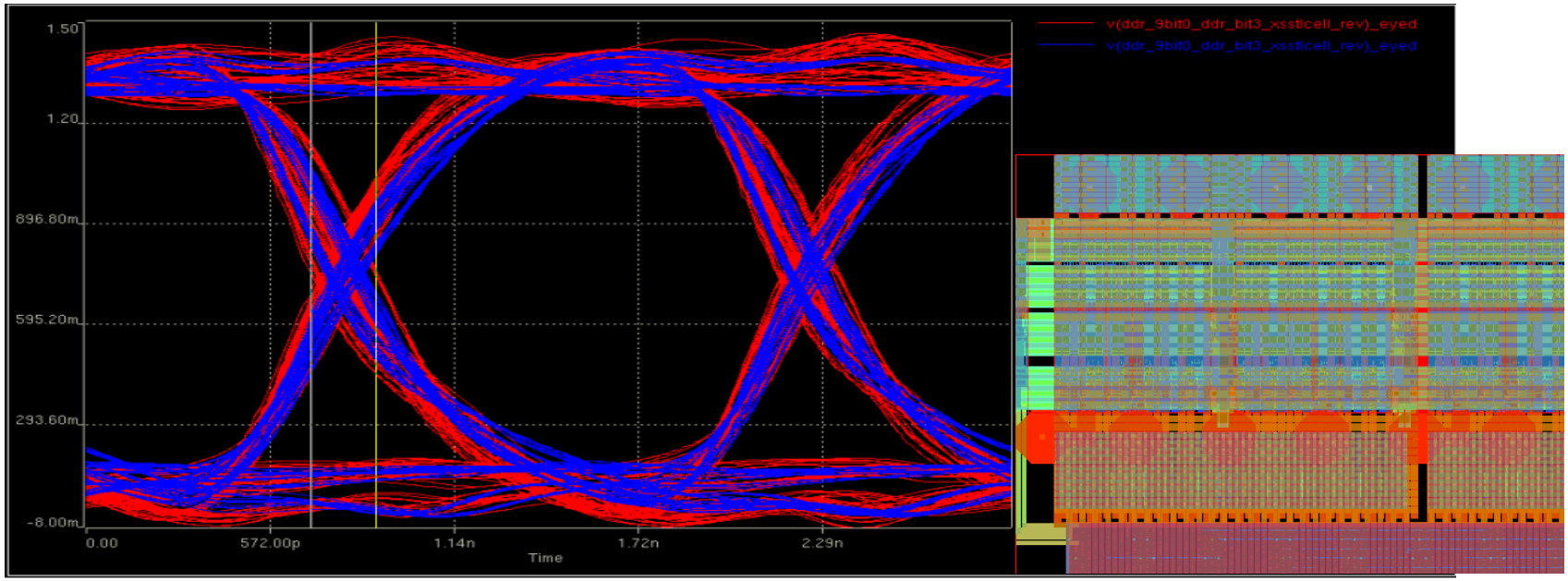


Key Aspects of Co-Verification

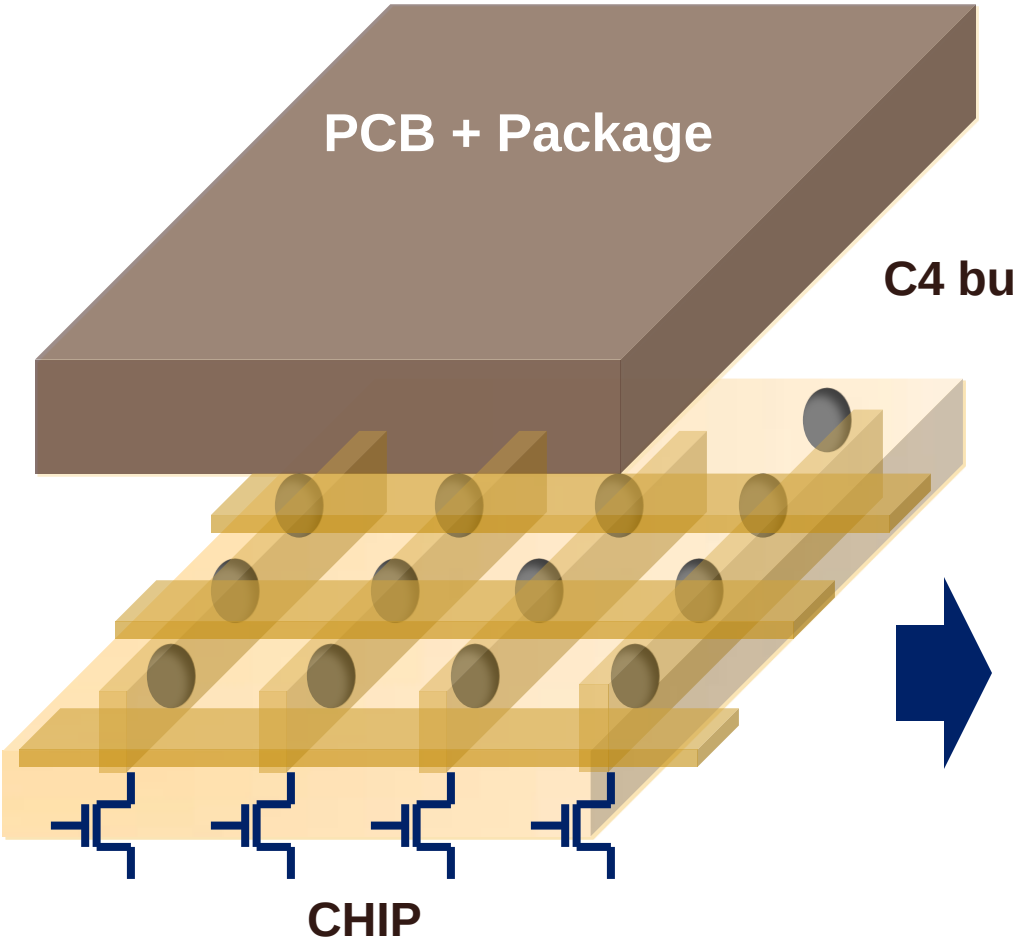
- Handling of multiple banks of DDR interface for realistic debugging
- Early stage co-design / co-verification
- IO ring parasitics and decaps
- Impact of core switching noise
- Accurate channel models from DC to 15GHz

On-Die PG Effect on Jitter

- Red – Jitter simulation without on-die PG grid: 202ps
- Blue – Jitter simulation with on-die PG grid: 150ps

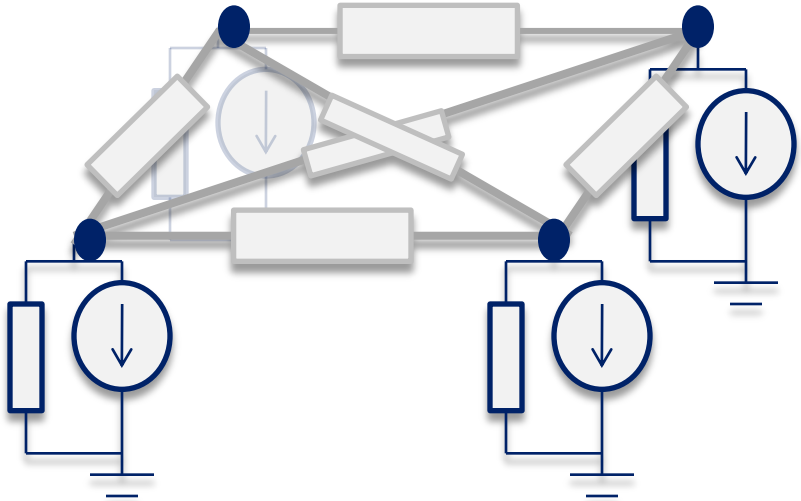


Chip Power Model for C-P-B Analysis

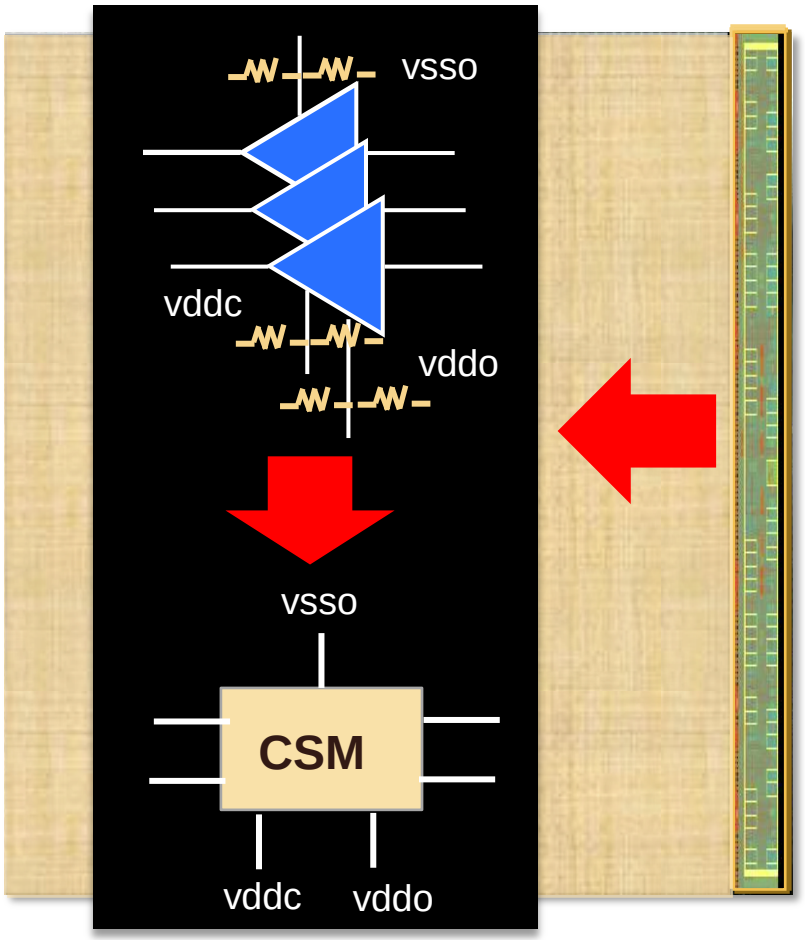


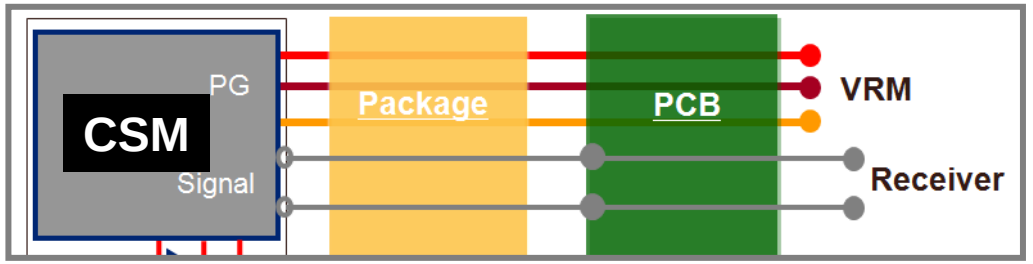
- Chip on-die Power Grid RLC
- Transistor current /Cap/Esr
- Open SPICE netlist format

Chip Power Model

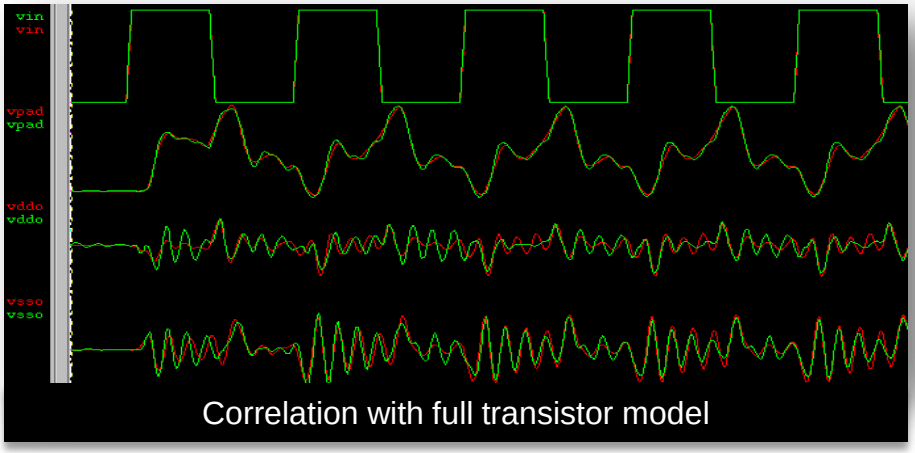


Expanding CPM for DDR - Chip Signal Model



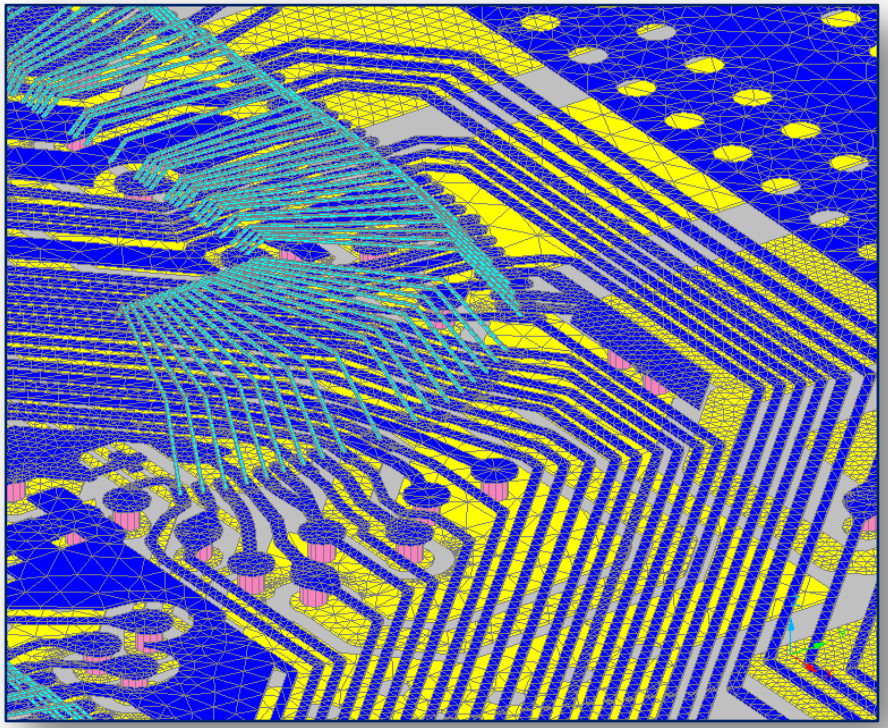


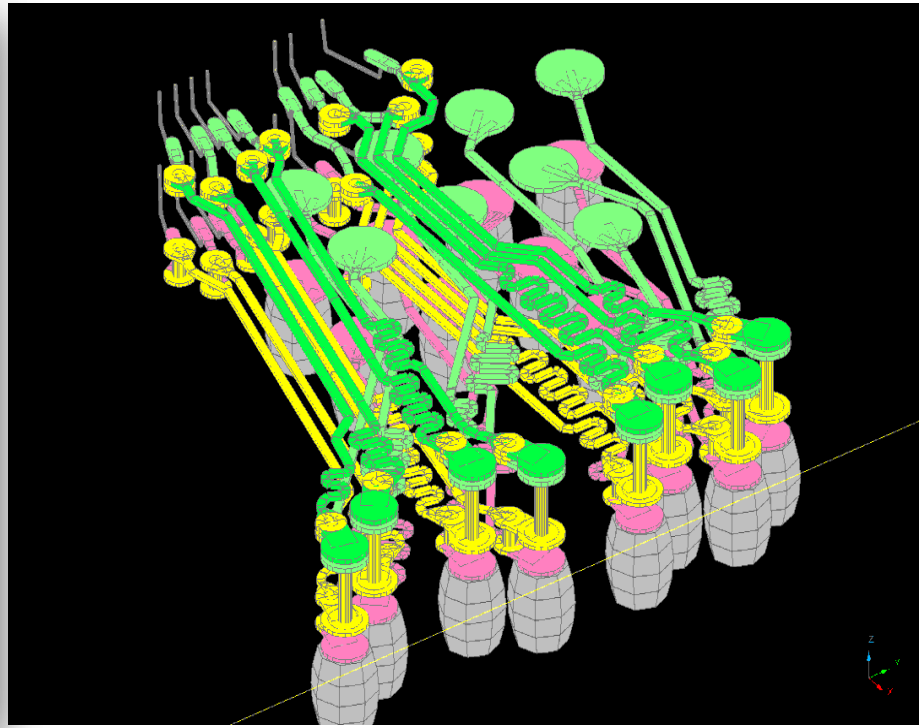
Models non-linear IO behavior & PG parasitics
Speed-up for DDR system simulation
Enables C-P-B co-verification of DDR



Correlation with full transistor model

Need Accurate Channel Models





Conclusion

- DDR3 C-P-B co-verification needs a platform that integrates and models all the components in the DDR system
- Early co-analysis is the key to the success through model exchange among chip, package and board design teams
- New design methodologies suitable for co-verification are needed to overcome challenges from DDR3 1.6G

Your Best SOC Design Foundry

ASP DAC 2011
Yokohama, Japan

DDR3 1600mbps

Global Unichip Corporation
Jen Tai Hsu
Senior Director, IP Division

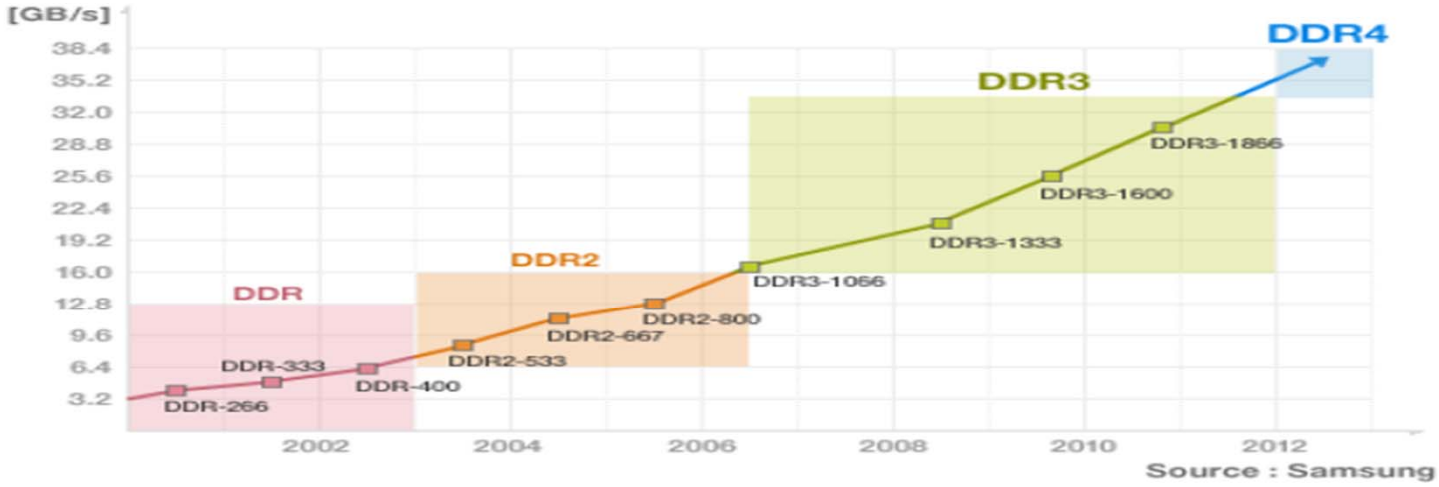
創意電子
GLOBAL UNICHIP CORP.

Outlines

- DDR memory and trend
- DDR3 new feature introduction
- DDR3 high speed PHY design
- PI/SI analysis
- Wire bond solution
- 1866/2133mbps higher speed of DDR3
- Conclusion

DDR Generation

- DDR3 : transition happening but not complete yet
- DDR4: 2011 specification finalized



High-bandwidth Samsung DDR3 SDRAM will provide a performance growth path for tomorrow's desktops, notebooks and servers. For example, a dual-channel, 128-bit, 1.6Gb/second DDR3 memory subsystem offers bandwidth beyond 25.6GB/second.

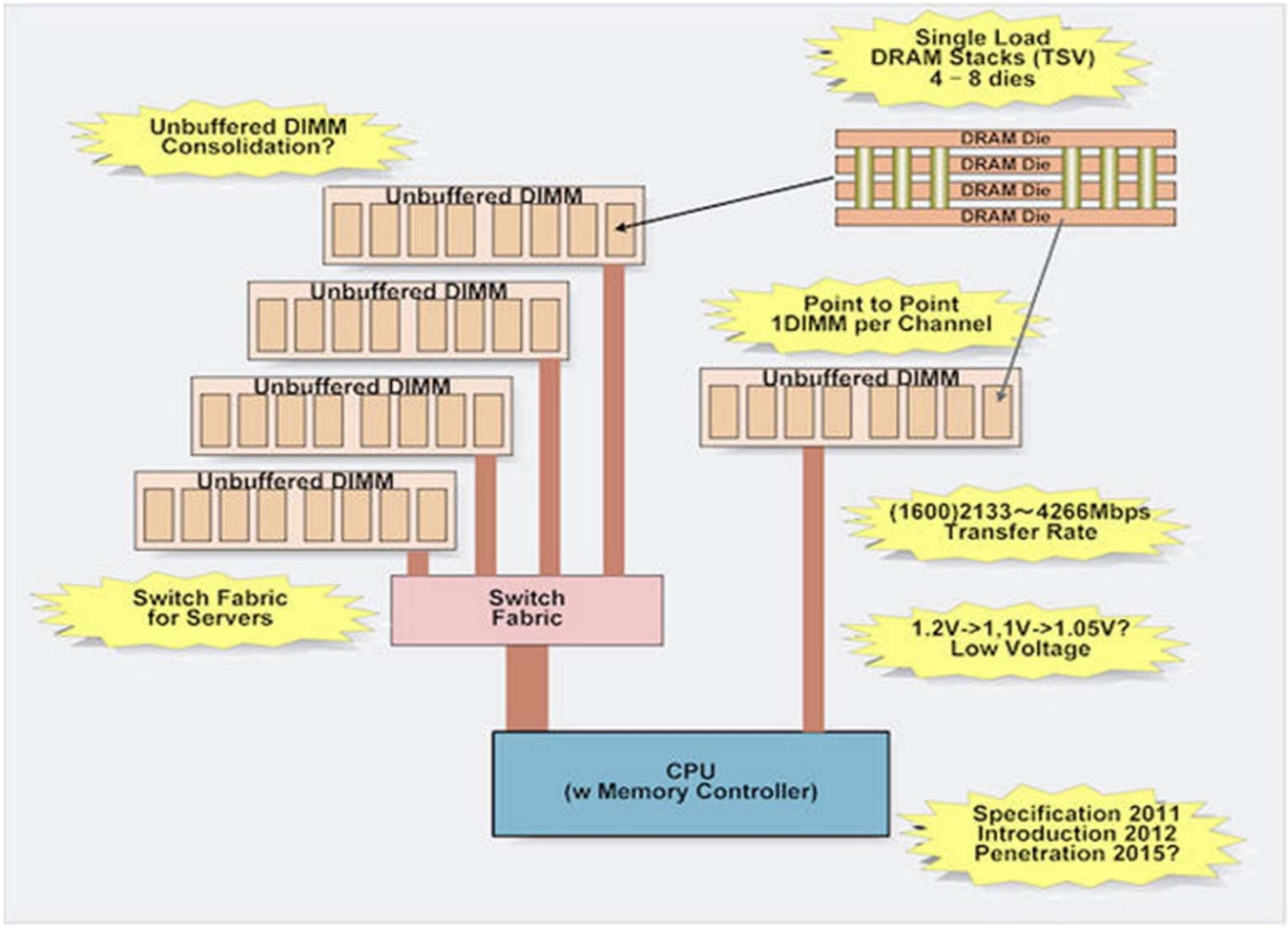
DDR memory comparison

- DDR feature comparison

Memory	DDR2	DDR3	DDR4
Data rate (mbps)	400~1066	800~2133	2133~4266
System assumption	2 DIMM per channel	2 DIMM per channel	single DIMM per channel
Vdd/Vddq	1.8v±0.1v	1.5v±0.075v	1.2v/1.1v *
Interface	SSTL18	SSTL15	
Package	TSOP/BGA	BGA	BGA/TSV (Through-silicon Via)
System buses	parallel	parallel	point to point

* not finalize yet

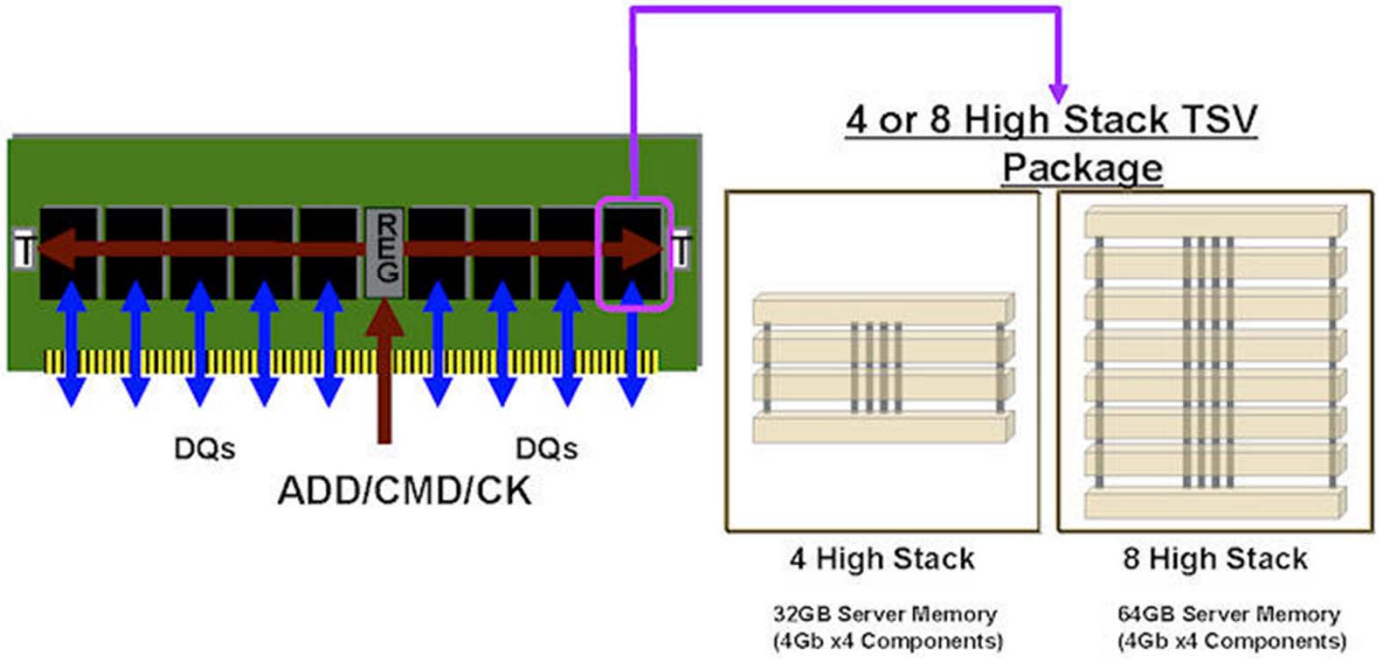
DDR4 system



Source: PCWatch 後藤弘茂

TSV in DDR4

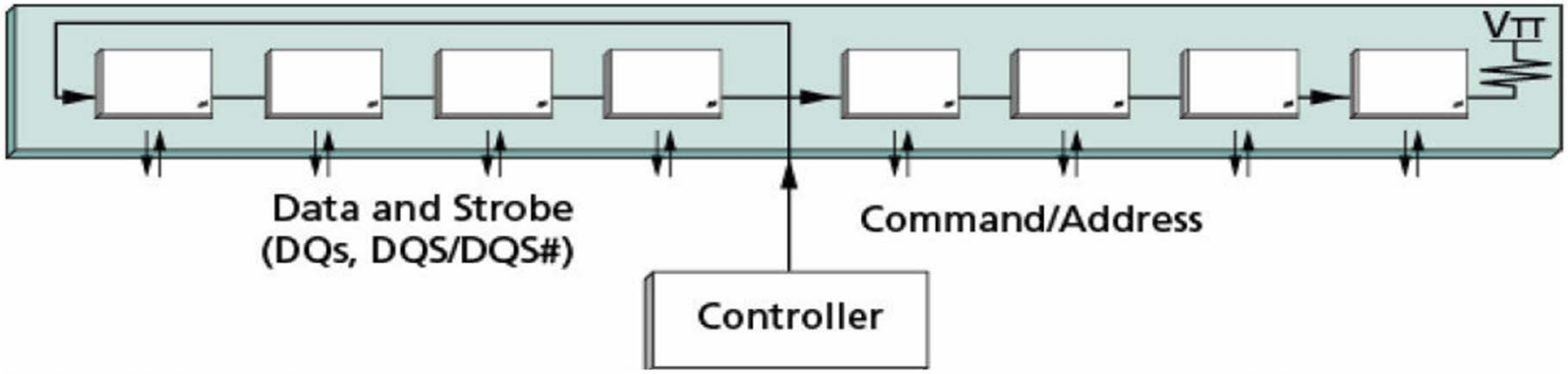
TSV Example in Server

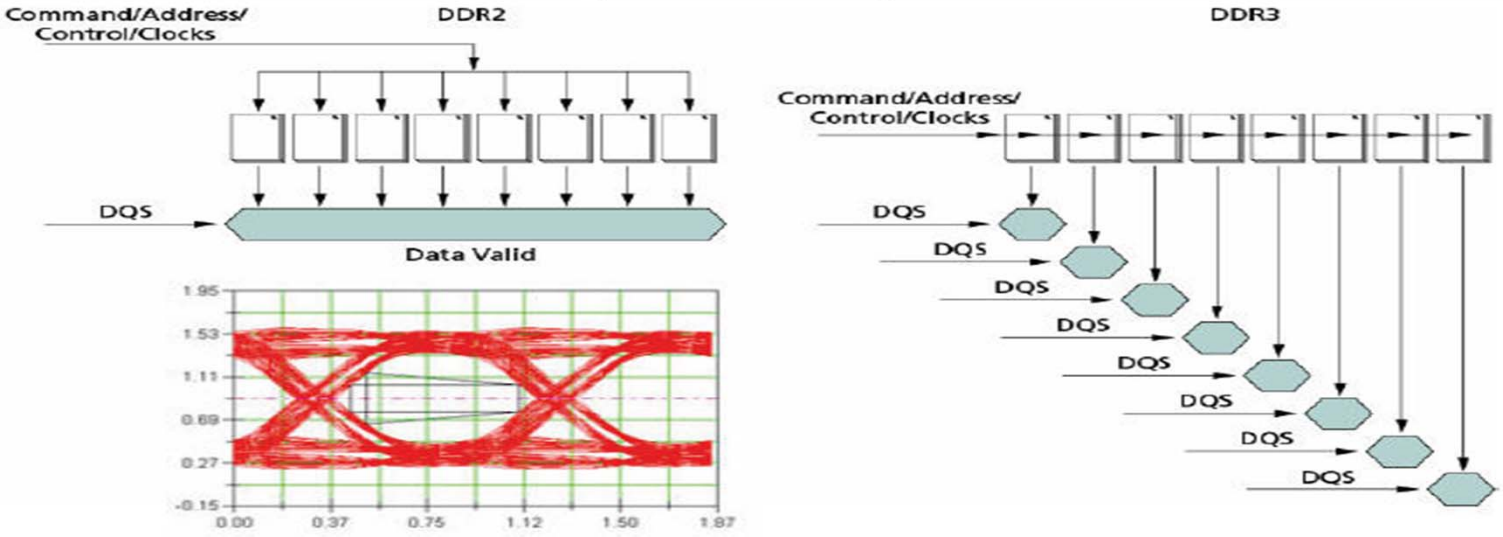


Source: Denali MEMCON10

DDR3 new feature (1)

- Write/ Read leveling





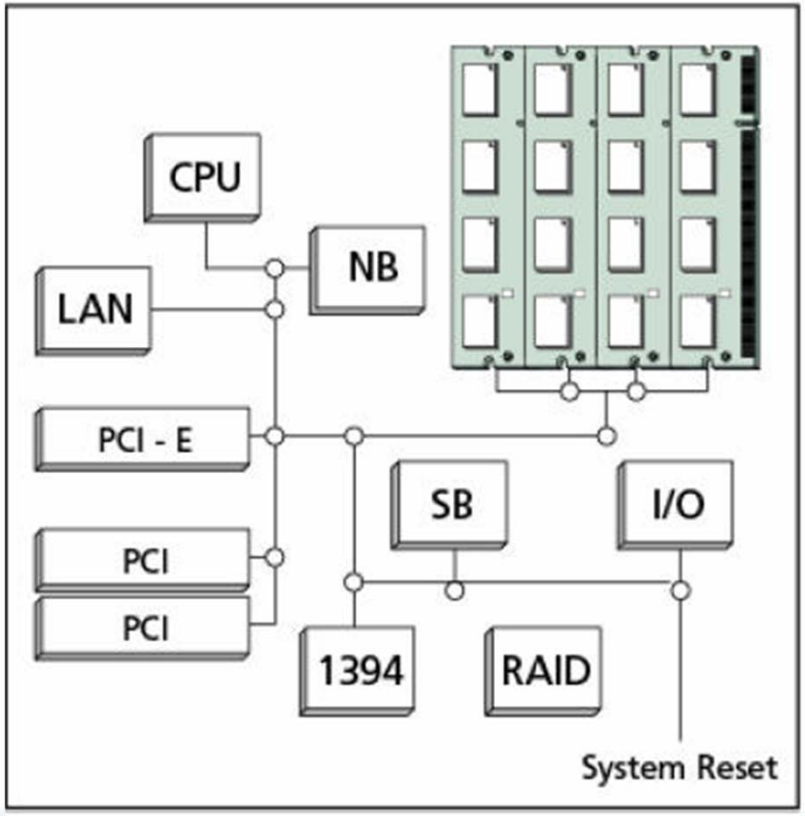
Source: Micron

DDR3 new feature (2)

- Dynamic ODT (On Die Terminator)
  - ODT advantage
    - Dynamically turn on and off parallel terminator
    - Save power
      - Extra components cause leakage
    - Save cost
      - No extra components
  - ODT can change value on the fly without idle time in DDR3
    - It is applied in 2 DIMM module system
      - For the non-active device during write, with low-impedance terminator value
      - For the active device during write, with high-impedance terminator value

DDR3 new feature (3)

- Master Reset
  - Improve system stability
  - Reduce controller burden to ensure no illegal command



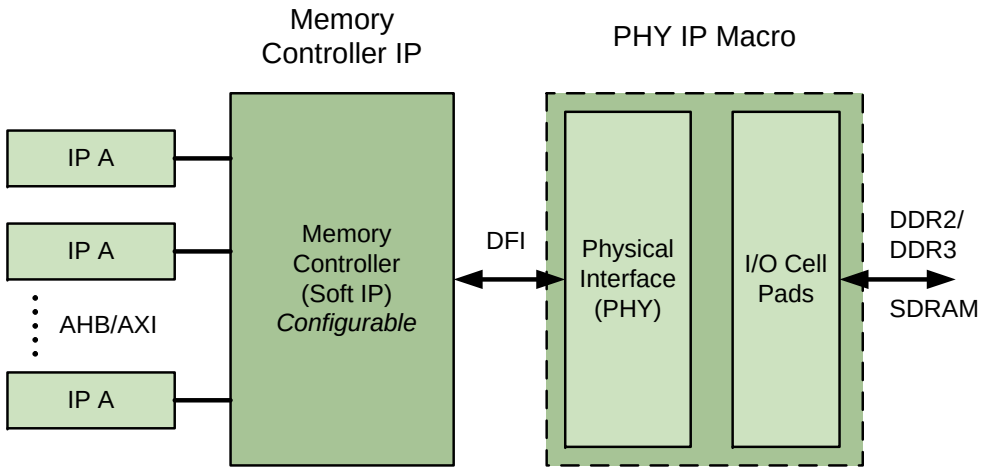
Source: Micron

DDR3 new feature (4)

- Self calibration
  - Through a ZQ pin to calibrate the accurate ODT (on die terminator) and OCD (off chip driver)
- In DDR2, most of DDR chip use trimming to adjust OCD value

DDR3 high speed PHY design (1)

- Block diagram in system



DDR3 high speed PHY design (2)

- DDRPHY
  - IO (so called SSTL-15)
  - PLL/DLL(source synchronous DQS/DQ)
  - Logic (Ser/De-Ser, DFT…)
  - PVT (calibration)

DDR3 high speed PHY design (3)

- Timing budget
  - System designer need to break timing budget into individual parts in DDRPHY

tREF clock	1250			
	unit: ps	jitter/skew	setup time (ps)	hold time (ps)
Transmitter Components	DFF	skew		
	BUFFER	skew		
	MUX	skew		
	local clock tree	skew		
	local clock tree	jitter		
	dll	jitter		
	DQ IO duty	skew		
	DQ IO C2C	jitter		
	SSO push out	jitter		
Total transmitter uncertainty				
Inter-connection	PCB cross talk			
	ISI			
	Package and substrate	skew		
	PCB	skew		
Receiver components (DRAM)	tDS/tDH (1600mpbs) base AC150			
	tDS/tDH (1600mpbs) delta			
	tDS/tDH (1600mpbs) total			
	Total Worst Case Jitter + Skews			
	Data UI			
	Margin Under Absolute WC			
	Margin Under typical case			
	Margin Under guard banded			

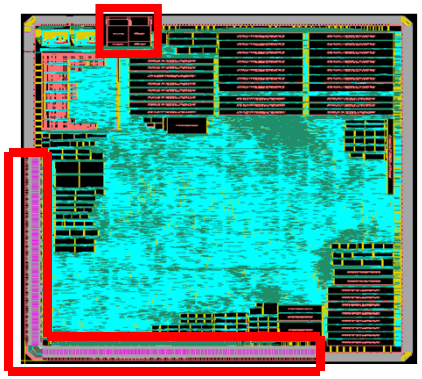
DDR3 high speed PHY design (4)

- To accommodate low cost and provide high performance DDR IP, per-bit de-skewing technology need to be used to eliminate the following skew and limit the total skew to 30ps
  - Internal Clock Skew
  - Internal Circuit Routing Skew
  - Package Skew
  - PCB Skew

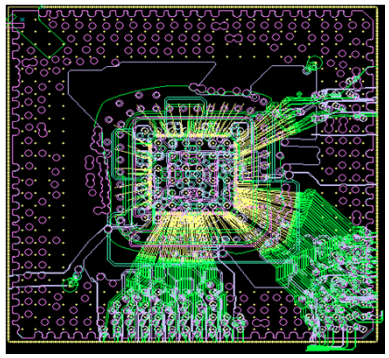
PI/SI (1)

- Power integrity and Signal integrity analysis is the must be items for DDR system design
- A DDRPHY claims it could run up to 1.6Gbps does not mean anything
- Package and PCB design impact the timing budget seriously

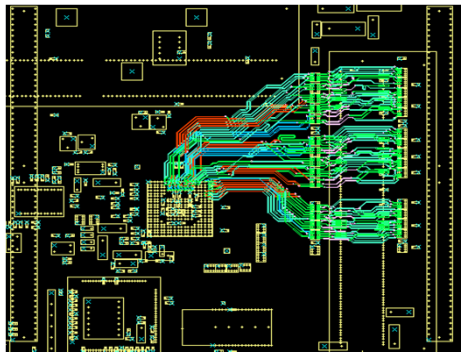
Chip model

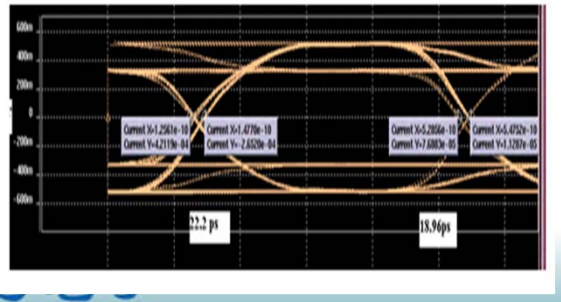


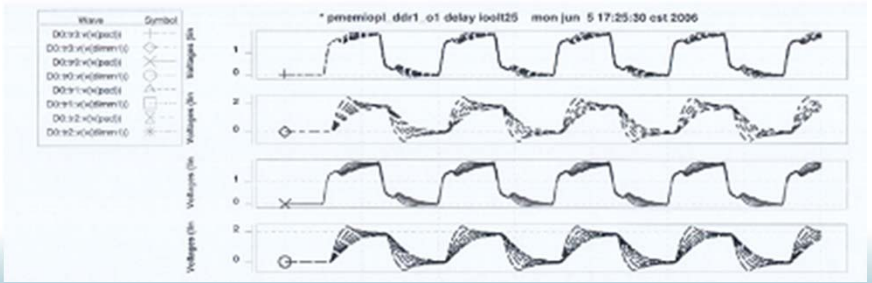
Package model



Board model







PI/SI (2)

- PI (power integrity)
  - Decoupling capacitor adding could lower the impedance in PI simulation
    - Decoupling capacitor need to be put as close to circuit as possible
    - On package decap
      - Capacitance size larger but with substrate inductance from die
    - On die decap
      - Capacitance size smaller but with very small inductance
  - How to optimize the usage of two kinds of decap
    - With flexible decap added on DDRPHY IP could optimize the package design flow in adding decap

PI/SI (3)

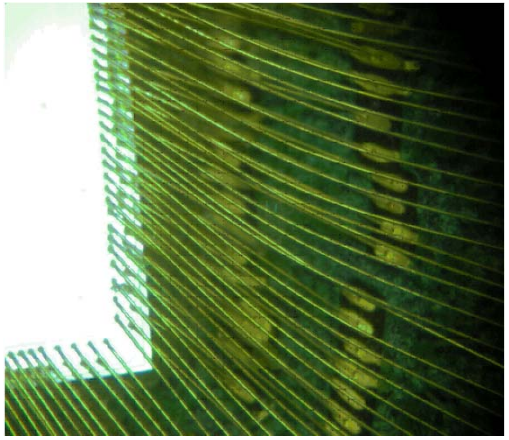
- SI simulation Eye diagram
  - The final sign-off of the DDRPHY system will be eye-diagram, which contains the following information
    - SSO
    - Cross-talk
    - ISI
    - IO duty
    - reflection

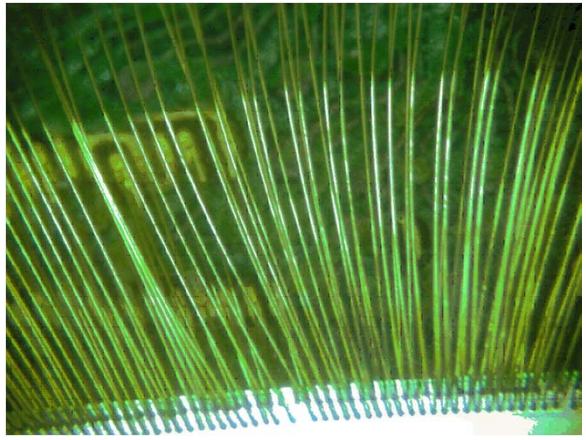
PI/SI (4)

- SI simulation Eye diagram
  - Model correctness will decide the accuracy of simulation result
    - PCB
    - Package
    - IO
  - Iteration on the correlation of simulation result and measurement takes a long cycle and timing consuming

Wire bond solution (1)

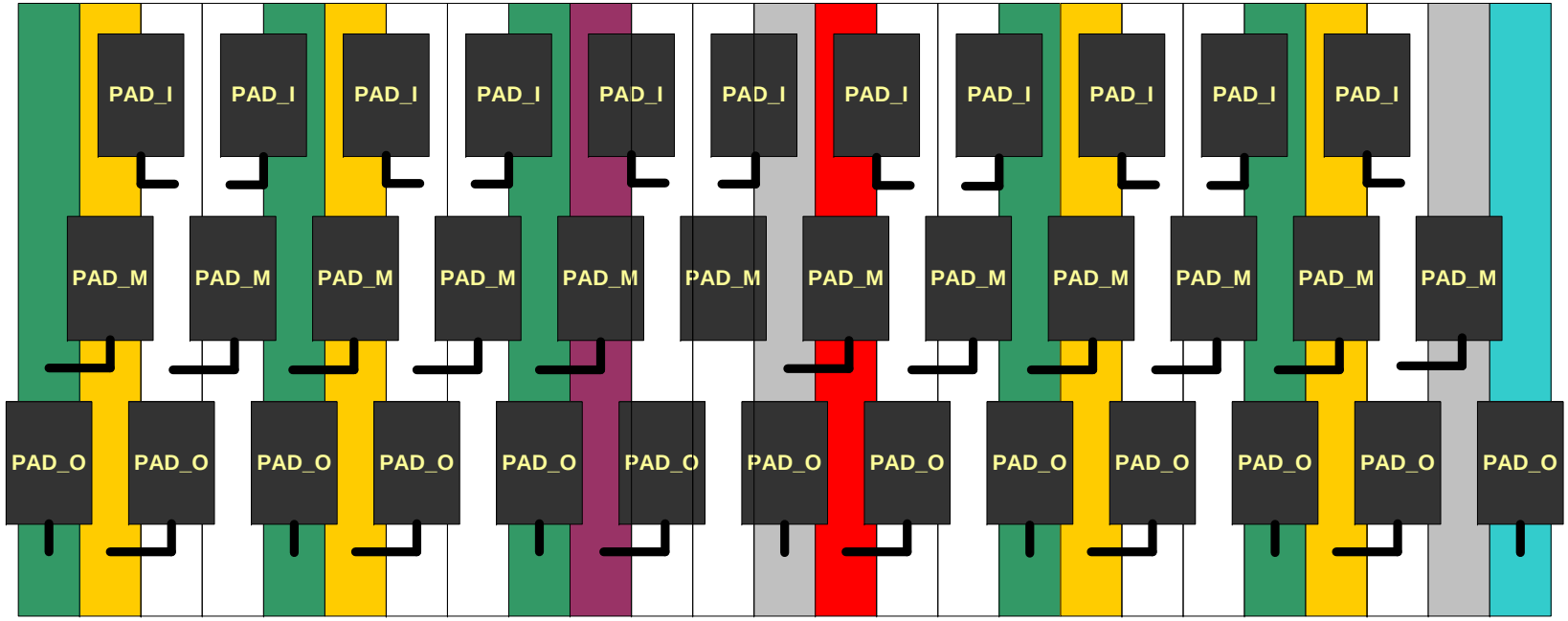
- Wire bond package needs more careful package substrate design
- Increase power/ground to IO ratio could lower the inductance of substrate
- General speaking, power/ground to IO ratio = 1:2 is a good starting
- However, high power/ground to IO ratio will increase the DDRPHY area





Wire bond solution (2)

- Proper arrangement on DDRPHY IO layout can increase power/ground to IO ratio without increase the size of PHY
- Tri-tier bond pad arrangement could decrease 40% of wire inductance



Higher speed in DDR3 (1)

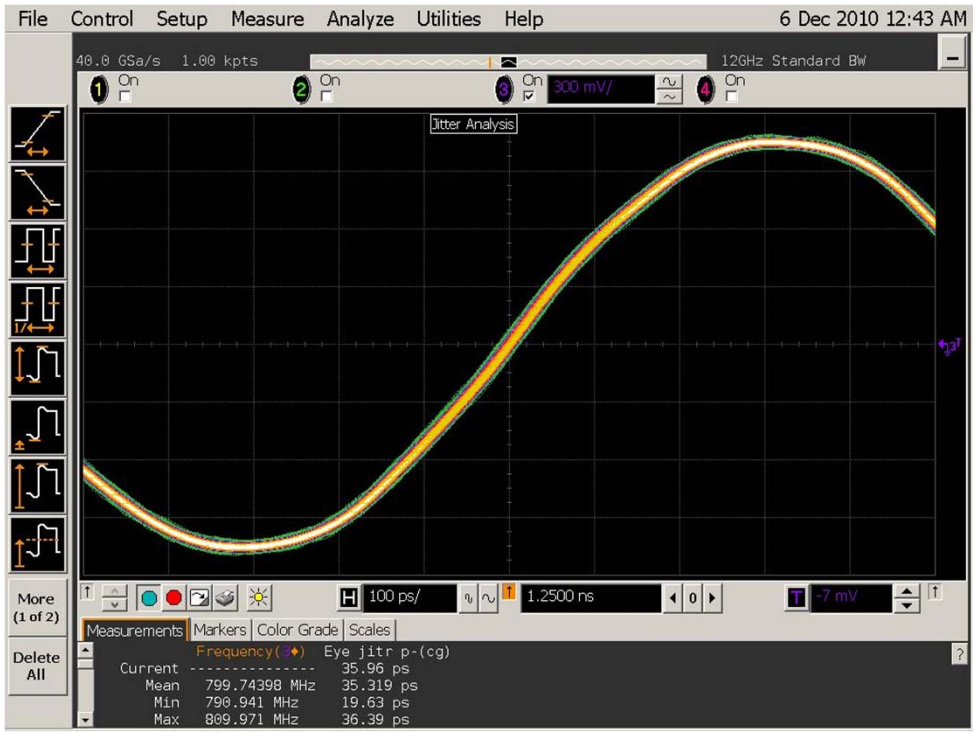
- DDR3 maximum speed is 2133mbps
  - UI = 468.8ps compared with UI =625ps when operating in 1600mbps. Difference = 156.2ps
- There is no design margin in such high speed operation
- How to “squeeze” the source synchronous system for the extra 156ps margin, that is a big challenge

Higher speed in DDR3 (2)

- DDR3 2133mbps
  - From the data eye simulation of 1600mbps, the setup time + hold time = 418ps, which means the following items take UI(625ps) - 418ps-25ps (dqs skew + jitter) = 182ps
    - SSO
    - Cross-talk
    - ISI
    - IO duty
    - reflection
  - DDRPHY designer need to squeeze 100ps from 182ps and another 50ps from the other skew and jitter inside the PHY

Higher speed in DDR3 (3)

- DDR3 2133mbps
  - Every components in the system need to be designed very carefully
    - PCB
    - Package
    - IO
    - Impedance matching
    - Clock skew
    - PLL/DLL jitter



Conclusion

- High speed DDR performance will strongly depends on
  - DDRPHY design and need DDR controller to provide logic function control of PHY
  - Package design
    - PI/SI simulation is to make sure the quality of package substrate
  - PCB design
    - PCB layer and layout will impact the performance of DDRPHY a lot

C-P-B Co-design/Co-verification for DDR3 1.6G in consumer products

CT Chiu, ASE

January 27, 2011

Packaging Trend for Consumer Product

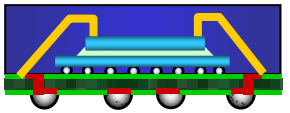
0.18 μm/FSG | 0.13 μm/FSG | 90 nm/Low-K | 65 nm/Low-K | 45 nm/Low-K

- High Density and Supply Chain Integration
- Emerging Advanced Packages Solutions
- High Electrical & Thermal Performance
- Fast Time-to-market & Quality
- Small, Light & Soft
- Low Cost
- Green

Ultra thin PKG

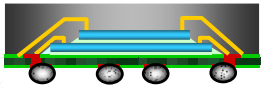
WLCSP

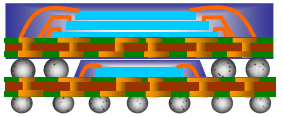
Hybrid PKG



Stacked / MCM / SiP PKG

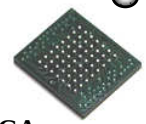
PiP





PoP

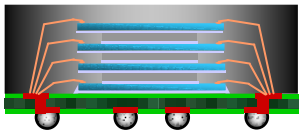
Ball Array PKG



FBGA
(mini BGA)

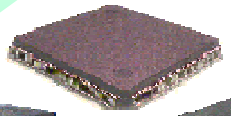
SiP BGA

BGA
family

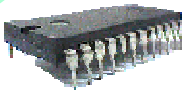


Stacked-die
BGA

Surface Mount Lead-frame PKG

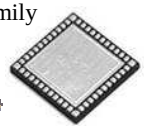


QFP
family



P-DIP

SOP
family

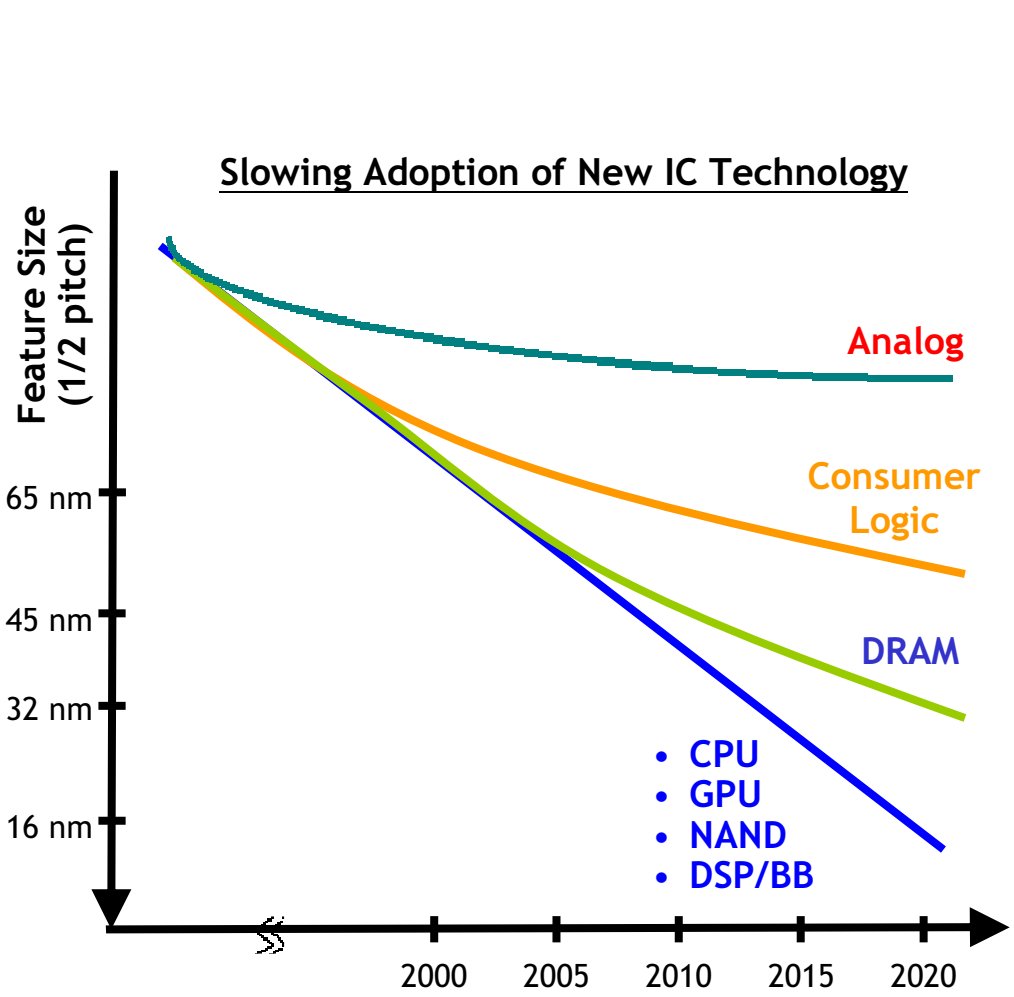


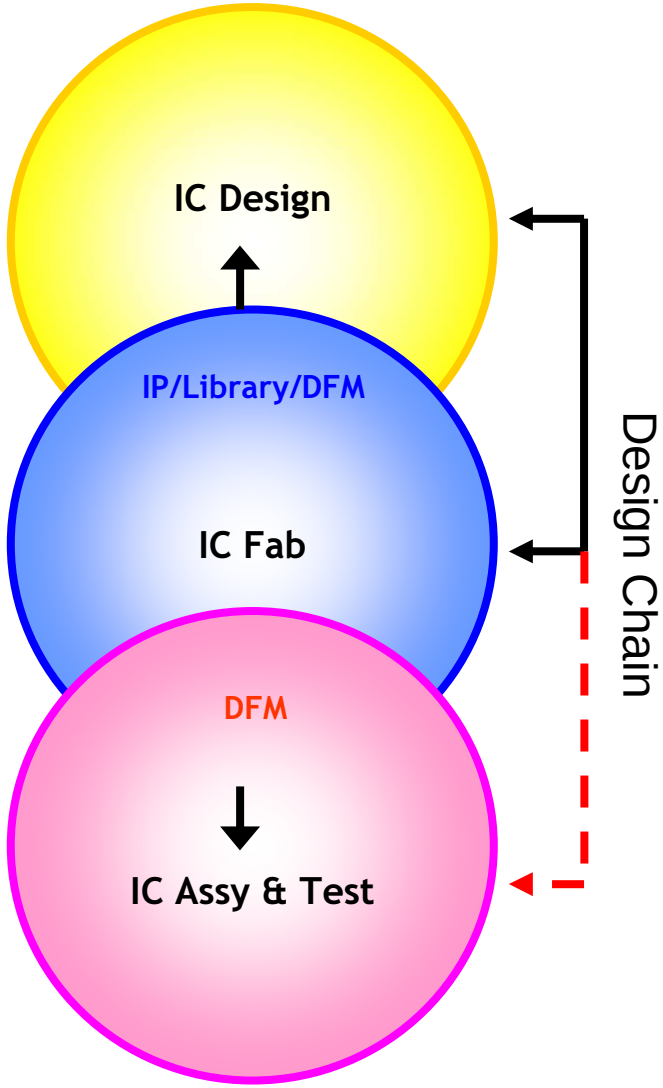
BCC

QFN
family

1990 | 1995 | 2000 | 2005 | 2010

Design Span Expanding for Total Performance

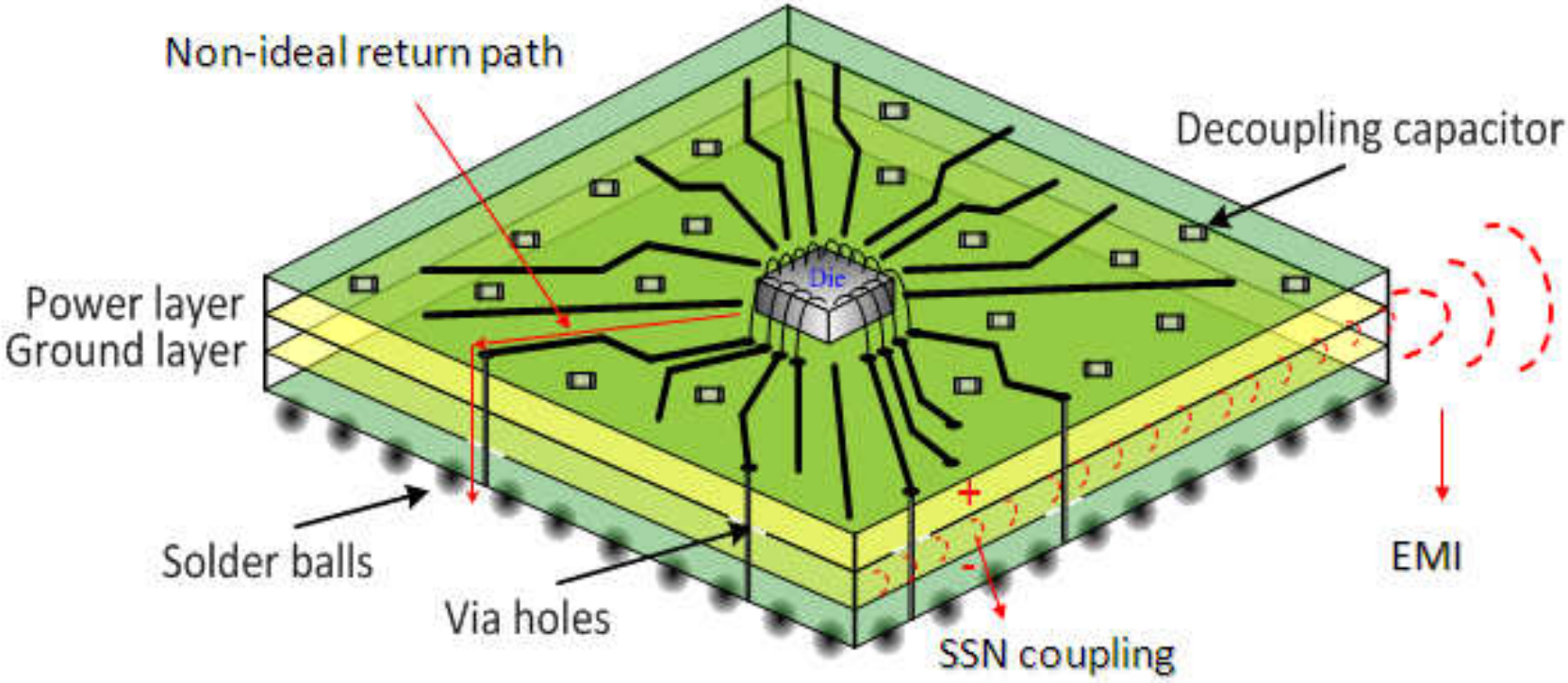




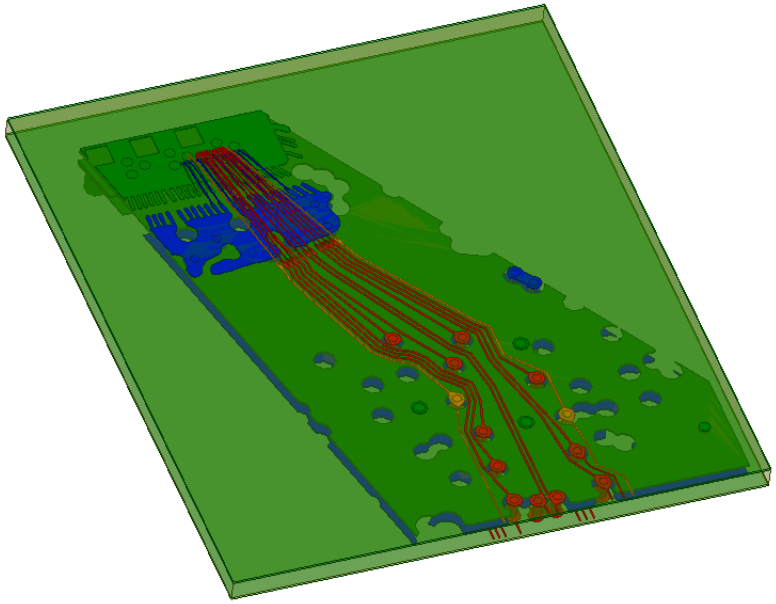
Ref.: GSA, SIA, ITRS (2007) & ASE Data

Package Performance Index for High Speed Signal

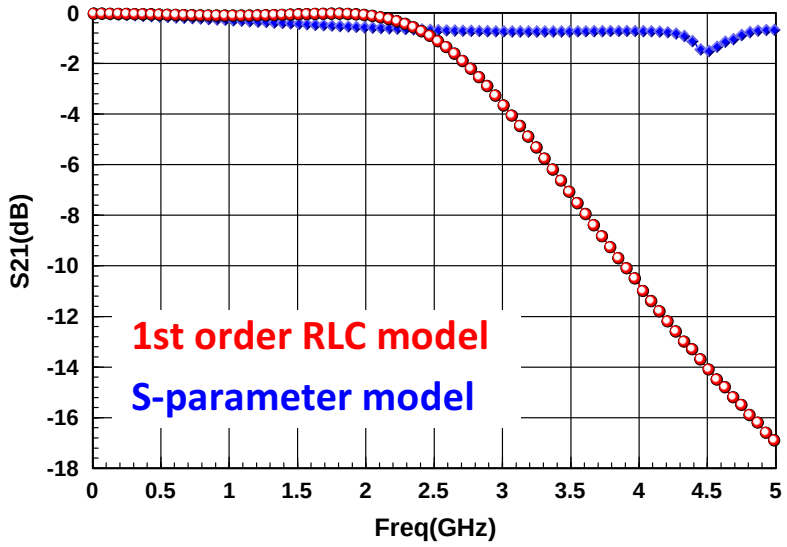
- **Signal Integrity (SI)**
  - **- Timing Skew, Impedance, X-talk, Jitter**
- **Power Integrity (PI)**
  - **- PSN impedance, SSN, SSO**
- **Eletromagnetic Interference (EMI)**
  - **- Near-field radiation, Shielding**

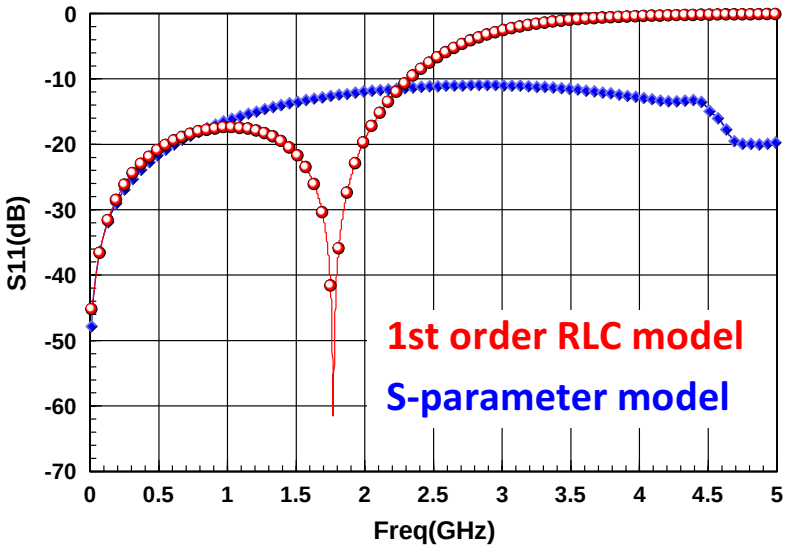


Package Modeling Transition

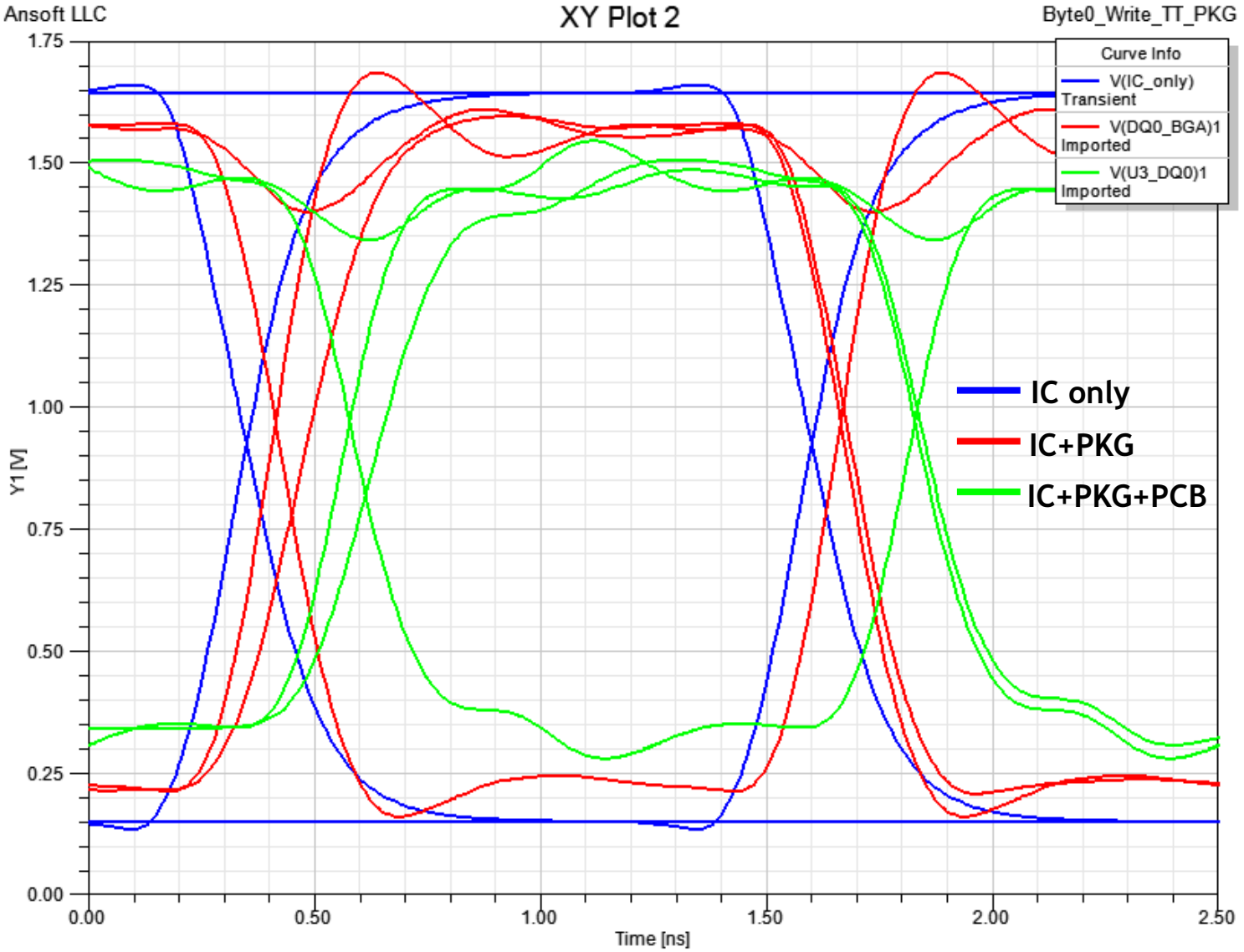


- ✓ Bonding wire
- ✓ Transmission line
- ✓ Via transient
- ✓ Plating bar
- ✓ PWR/GND effect

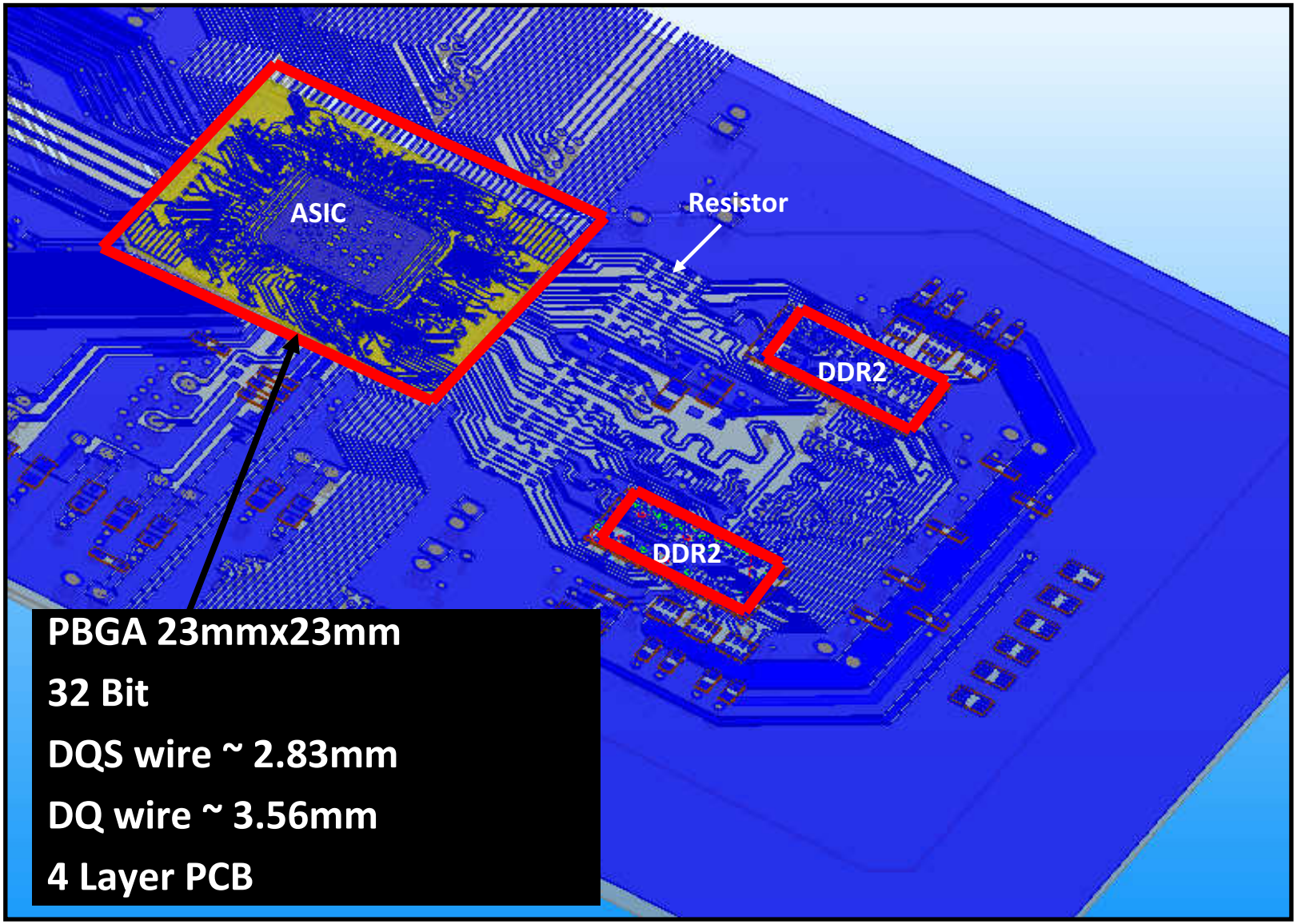




IC-Package-Board Co-Verification

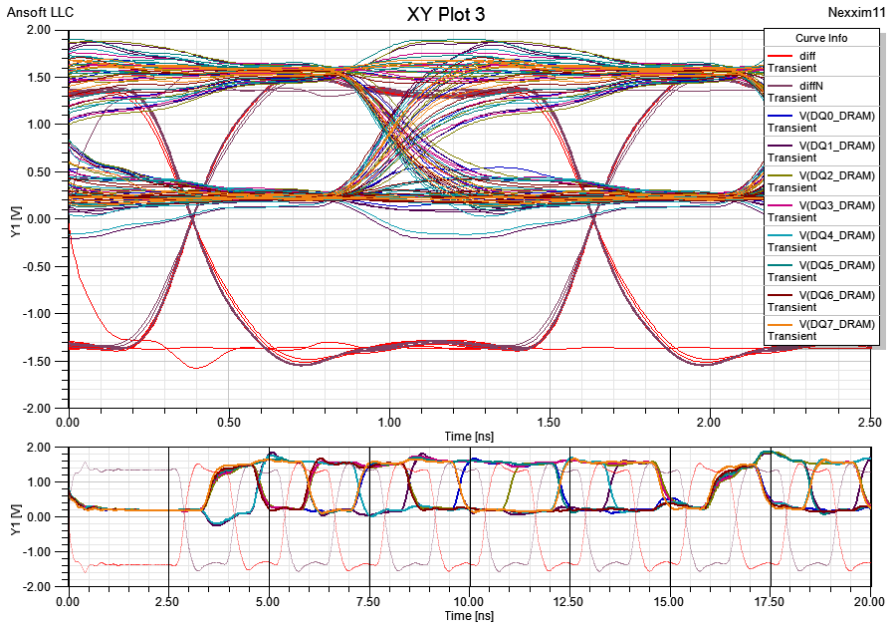


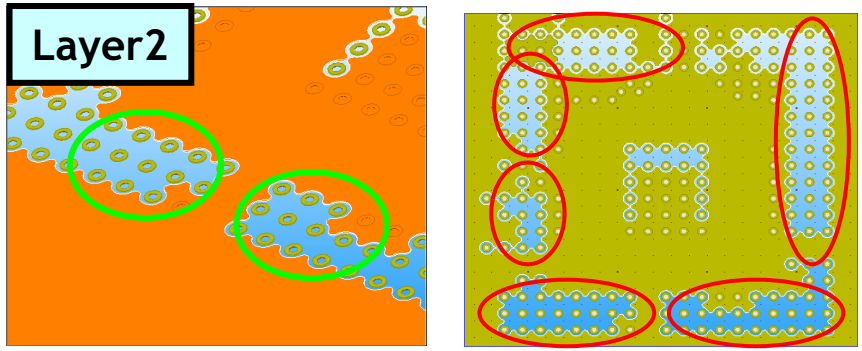
DDR2 - 800Mbps : Wire Bond BGA Package



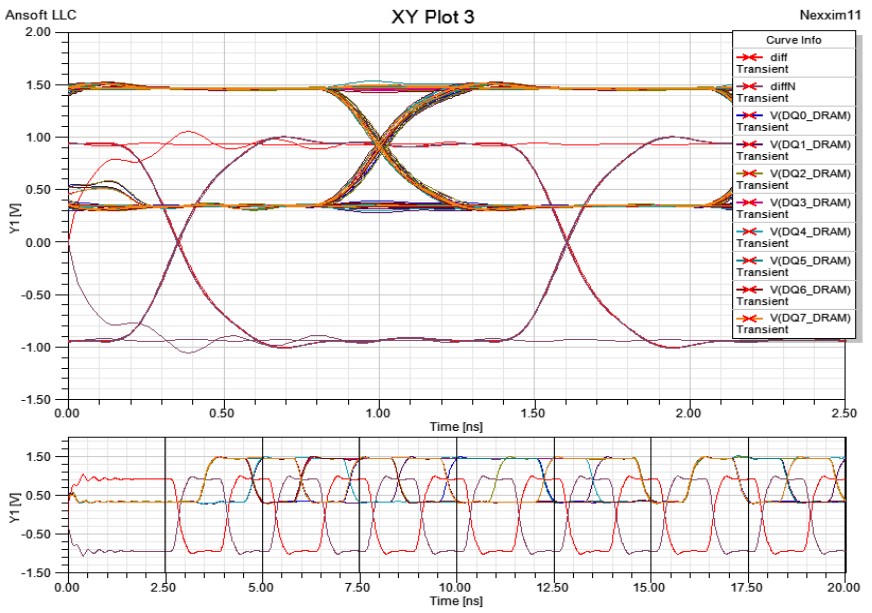
Chip-Package-Board Co-Simulation

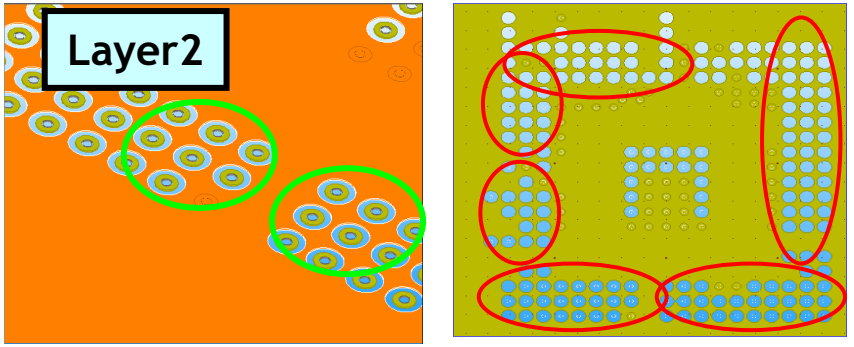
PCB GND shape voided (Original)





PCB GND shape filled (Modified)





Summary

- Package play as a carrier to offer highly density in 2D/3D integration which full fill consumer market demand in cost effective. Package design cope with system concept is essential in SiP.

- Package performance play significant part at overall product success. Chip-Packge-Board Co-Design/Co-Verification is crucial to products which operate at Gbps (or GHz).

- Package design optimization and modeling methodology transition ensure the quality signal integrity and power integrity performance to DDR2 which also been a basis for DDR3.