NBTI-Aware Power Gating Design

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Outline

- Introduction
- NBTI-Aware Power Gating Design
- Essential Issues of Arranging *On*/*Off* Signals in the Sequence
- Experimental Results
- Conclusions

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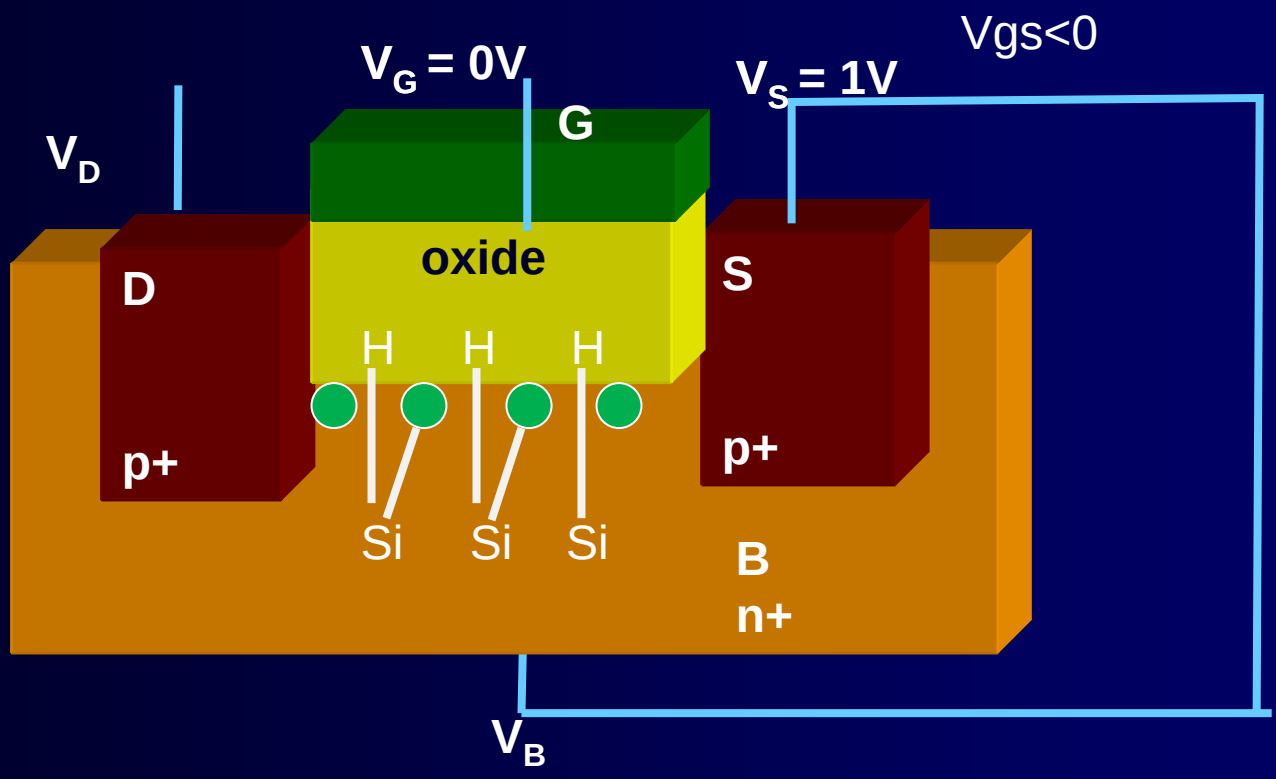
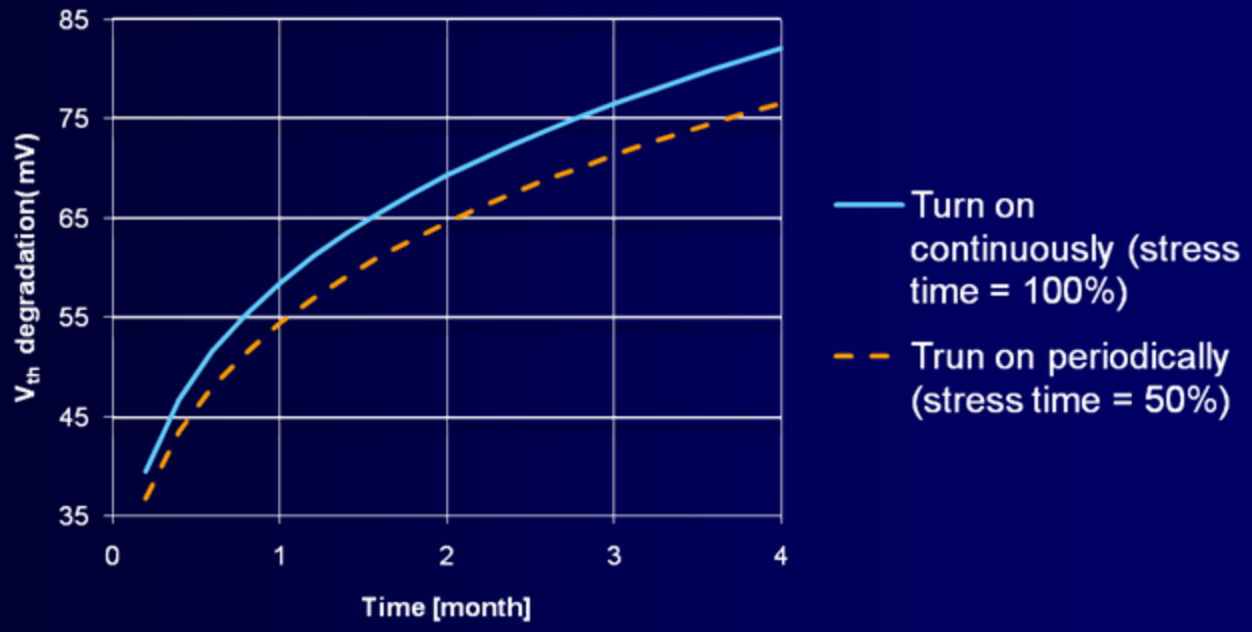
NBTI Effect

- Negative Bias Temperature Instability (NBTI)
- An inevitable side effect on the lifetime reliability of integrated circuits.



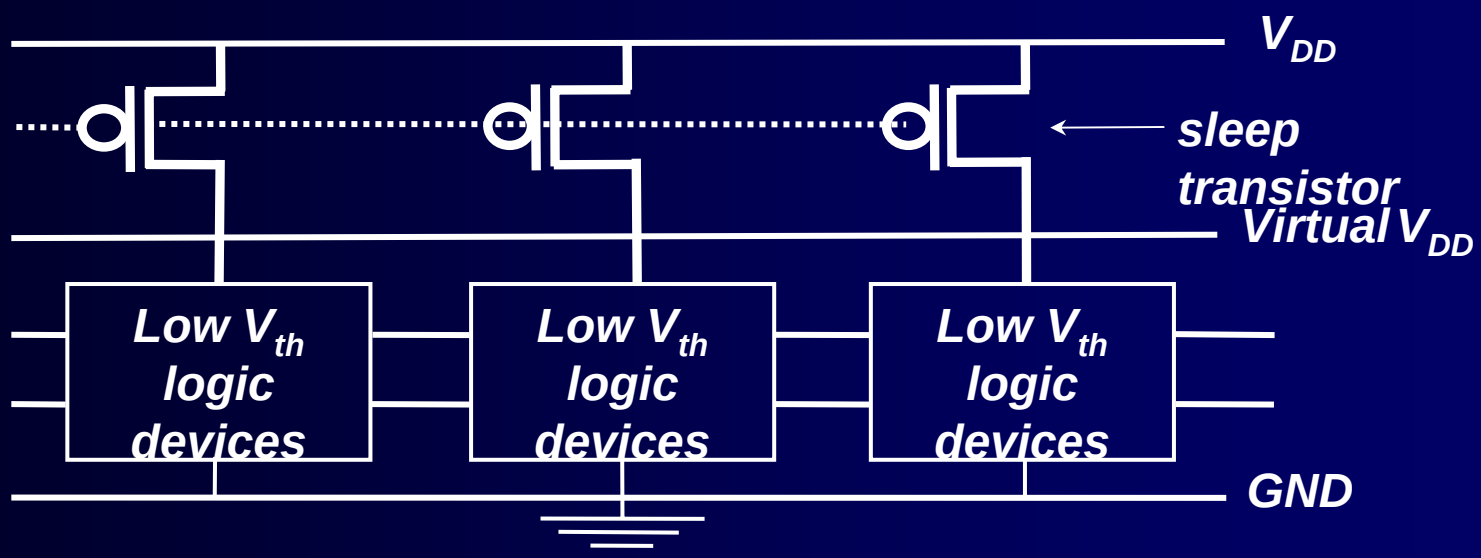
NBTI Effect

- Two phases ： **Stress** and **Recovery**.
- Stress phase results in increasing $|V_{TH}|$ and decreasing performance.
- Recovery phase can recover V_{TH} degradation.
- V_{TH} degradation is directly proportional to the stressed time of PMOS.



Header-Based Power Gating Design

- NBTI effect poses a serious problem on a header-based power gating design.
  - (i) PMOS sleep transistors are always turned-on.
  - (ii) PMOS sleep transistors are on the critical path from the power rail to the circuit.

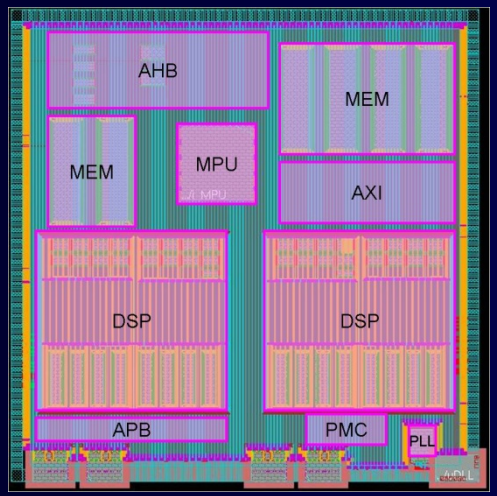


Related Works

- Three NBTI-tolerant PMOS sleep transistor cell design approaches：
  - (i) Sleep transistor over-sizing
  - (ii) Forward-body-biasing
  - (iii) Equivalent 0-probability reduction of the sleep transistor driving signal.
    - A. Calimera, E. Macii, and M. Poncino, “NBTI-Aware Sleep Transistor Design for Reliable Power-Gating,” *Proc. of the GLSVLSI*, pp. 333-338, 2009.

Problems on Power Gating Designs

- Entire circuit will slow down because of V_{TH} degradation on PMOS sleep transistors.
- A modern design usually operates in several different power modes.
- To safely maintain the functionality, sleep transistors are pessimistically sized.



Power Modes	MPU	DSP1	DSP2
Full speed	1.2V	1.2V	1.2V
Active1	1.2V	1.2V	1.0V
Active2	1.2V	1.0V	1.2V
Suspend	1.0V	1.0V	1.0V
Inactive	1.0V	0V	0V

Contributions

- No research considering NBTI effect on the modern power gating design.
- A novel power gating structure
  - Periodically turn on sleep transistors
  - Turn off unnecessary sleep
- A new flip-flop (FF) to alleviate two important phenomena
  - Voltage drop
  - Glitch on the VV_{DD} rail.
- Integrated smoothly with wakeup scheduling.
- 25% lifetime extension of PMOS sleep transistors.

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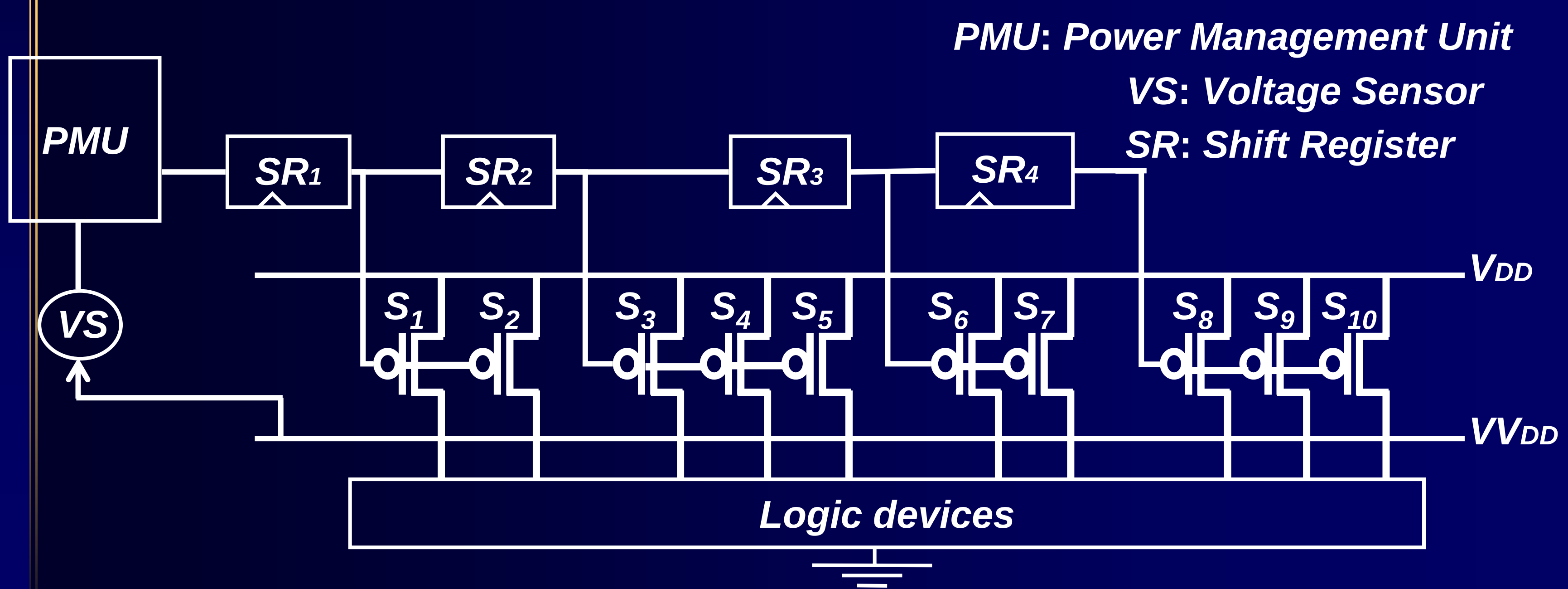
NBTI-Aware Power Gating Design

At the beginning, the shift register SR_1 turns off its corresponding PMOS sleep transistors S_1, S_2 while SR_2, SR_3, and SR_4 turn on sleep transistors from S_3 to S_{10}.

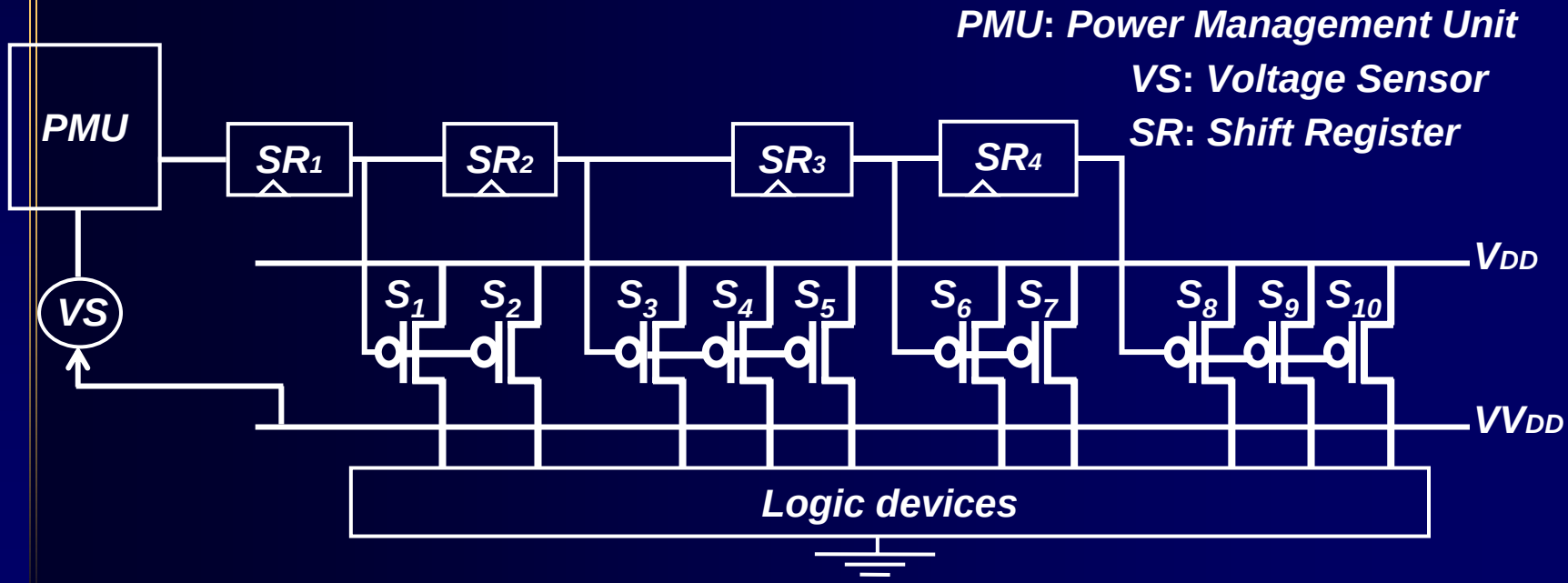
... the sequence of *On*/*Off* signals now is {*On*, *Off*, *On*, *On*}.

SR_2 turns off the PMOS sleep transistors from S_3 to S_5 while the rest of PMOS sleep transistors are turned on.



NBTI-Aware Power Gating Design

- Four states of *On*/*Off* signals in four *SR*s, {SR_1, SR_2, SR_3, SR_4},
  - {*Off*, *On*, *On*, *On*}, {*On*, *Off*, *On*, *On*}, {*On*, *On*, *Off*, *On*}, and {*On*, *On*, *On*, *Off*}.
- The duty cycle of each PMOS sleep transistors is 3/4 = 75%.



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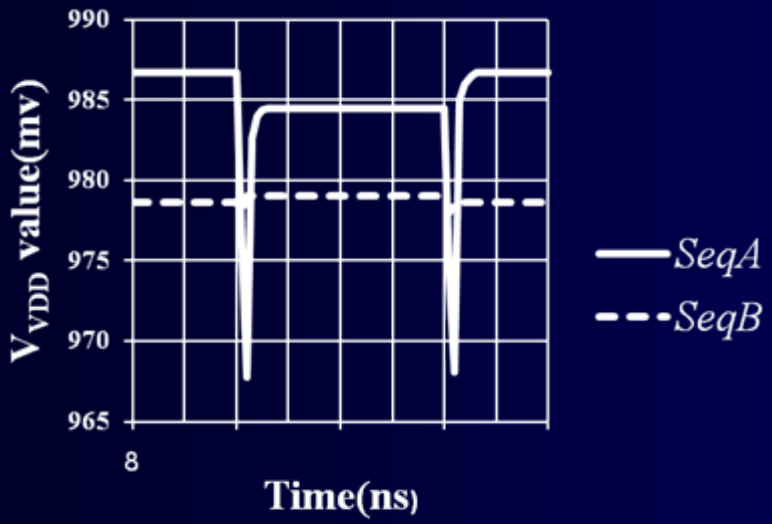
Preliminary

- In this paper, we assume that a wakeup scheduling of the power gating design is already determined.
  - Each SR_i connects to its corresponding group of PMOS sleep transistors.
  - The number and sizes of sleep transistors in each group have also been determined.
  - NBTI effect is directly proportional to the duty cycle of PMOS sleep transistors.
  - The duty cycle of PMOS sleep transistors is the ratio of the number of *SR*s whose input value is *On* to the total number of *SR*s.
  - Given the number of *SR*s whose input value is *On*, there are several ways to arrange *On*/*Off* signals in a sequence.

Examples

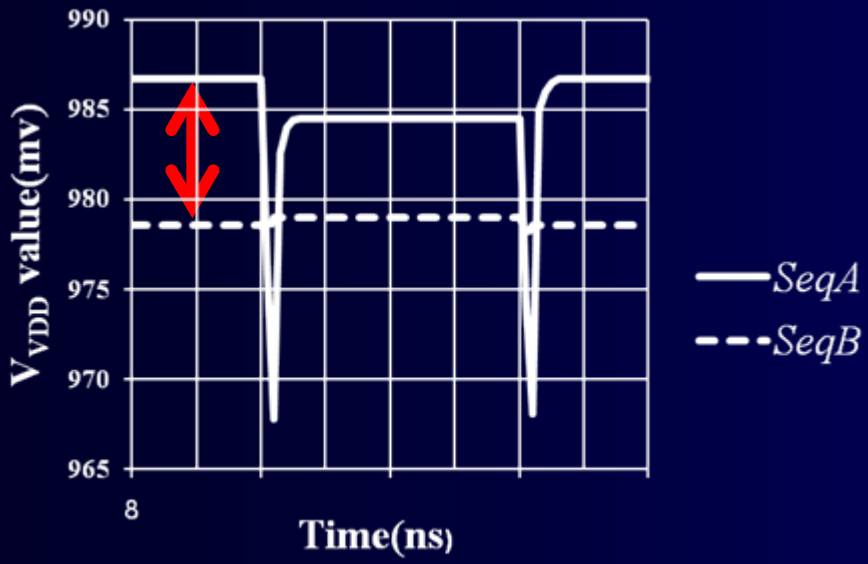
- Let us consider a real circuit with 12 *SR*s and 12 groups of sleep transistors.
  - *SeqA* and *SeqB*, both of which contain six *On* signals and six *Off* signals.
  - *SeqA* is interlaced *On* and *Off* signals.
  - *SeqB* has two continuous blocks of *On* and *Off* signals.



SeqA is {*Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*}.
SeqB is {*On*, *On*, *On*, *On*, *On*, *On*, *Off*, *Off*, *Off*, *Off*, *Off*, *Off*}.

Observation 1

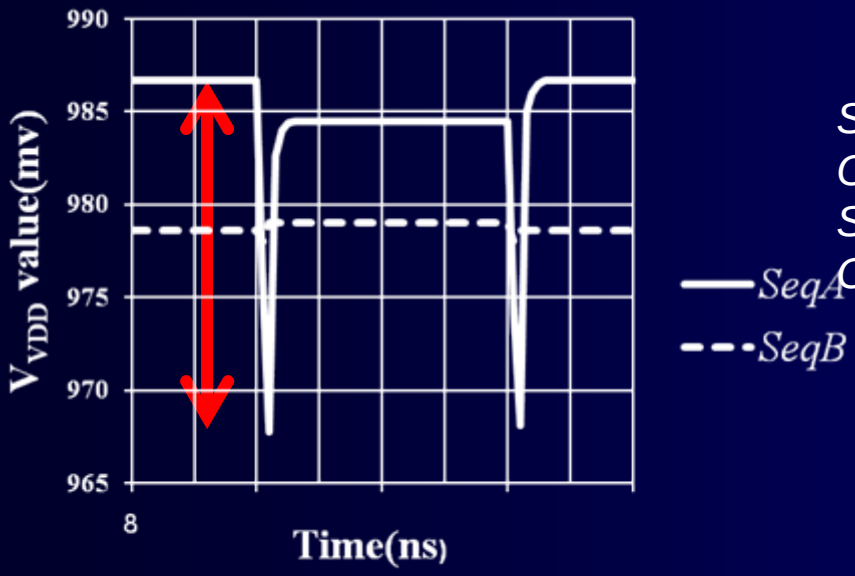
- The maximum voltage drop on the VV_{DD} rail for *SeqB* is about 38% larger than that for *SeqA*.
  - The reason is that *SeqA* can balance the flowing current better than *SeqB*.



SeqA is {*Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*}.
SeqB is {*On*, *On*, *On*, *On*, *On*, *On*, *Off*, *Off*, *Off*, *Off*, *Off*, *Off*}.

Observation 2

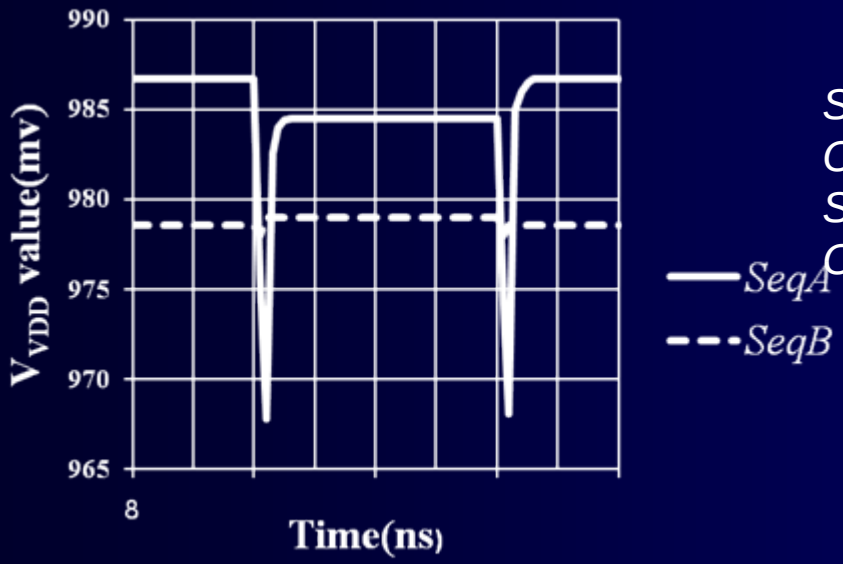
- The arrangement of *On* and *Off* signals may cause larger glitches on the VV_{DD} rail during the shifting process.
  - When *SeqA* is shifted, all *SR*s switch their values at the same time.



SeqA is {*Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*}.
SeqB is {*On*, *On*, *On*, *On*, *On*, *On*, *Off*, *Off*, *Off*, *Off*, *Off*, *Off*}.

Trade-Off

- Arranging *On* and *Off* signals in a balanced way, such as *SeqA*, can minimize the voltage drop but cause more glitches on the VV_{DD} rail.
- On the contrary, *SeqB* can cause less glitch on the VV_{DD} rail but have larger voltage drop.



SeqA is {*Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*, *Off*, *On*}.
SeqB is {*On*, *On*, *On*, *On*, *On*, *On*, *Off*, *Off*, *Off*, *Off*, *Off*, *Off*}.

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Experimental Setups

- Synopsys HSPICE reliability analysis to simulate NBTI effect
- TSMC 90nm CMOS technology
- An industrial benchmark: *AES*
- Two different power modes: 1.0V and 0.8V
- Decided number and sizes of sleep transistors and proper wakeup scheduling
- To consider NBTI effect, we also size additional 20% up sleep transistors by the over-sizing method.

Experimental Results

Table 1. Experimental results.			
The usage of low power mode (%)	Our approach lifetime (months)	Over-sizing method lifetime (months)	The lifetime extension (%)
100	200	135	48.15%
75	169	127	33.07%
50	154	123	25.20%
25	132	111	18.92%
0	73	60	21.67%
Average	145.6	111.2	30.94%

On average, our approach can achieve 30% lifetime extension compared with the over-sizing method [3].

Our approach, which includes the chain of *GA* FF and a voltage sensor, is only around 5.77% area overhead.

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Conclusions

- We have proposed a novel NBTI-aware power gating design to periodically turn on/off PMOS sleep transistors for the lifetime extension.
- We also consider two reliability issues which are the voltage drop and the glitch issue on the VV_{DD} rail.
- The experimental results clearly show that under the 50% usage of low power modes, our approach averagely achieves more 25% lifetime extension of PMOS sleep transistors than the sleep transistor over-sizing method [3] and also has few area overhead.

Thank you!