Simultaneous Redundant Via Insertion and Line End Extension for Yield Optimization

Shing-Tung Lin[1], Kuang-Yao Lee[2], Ting-Chi Wang[1], Cheng-Kok Koh[3], and Kai-Yuan Chao[4]

[1]Department of Computer Science, National Tsing Hua University, Taiwan

[2]Taiwan Semiconductor Manufacturing Company, Taiwan

[3]Electrical and Computer Engineering, Purdue University, USA

[4]Intel Corporation, USA

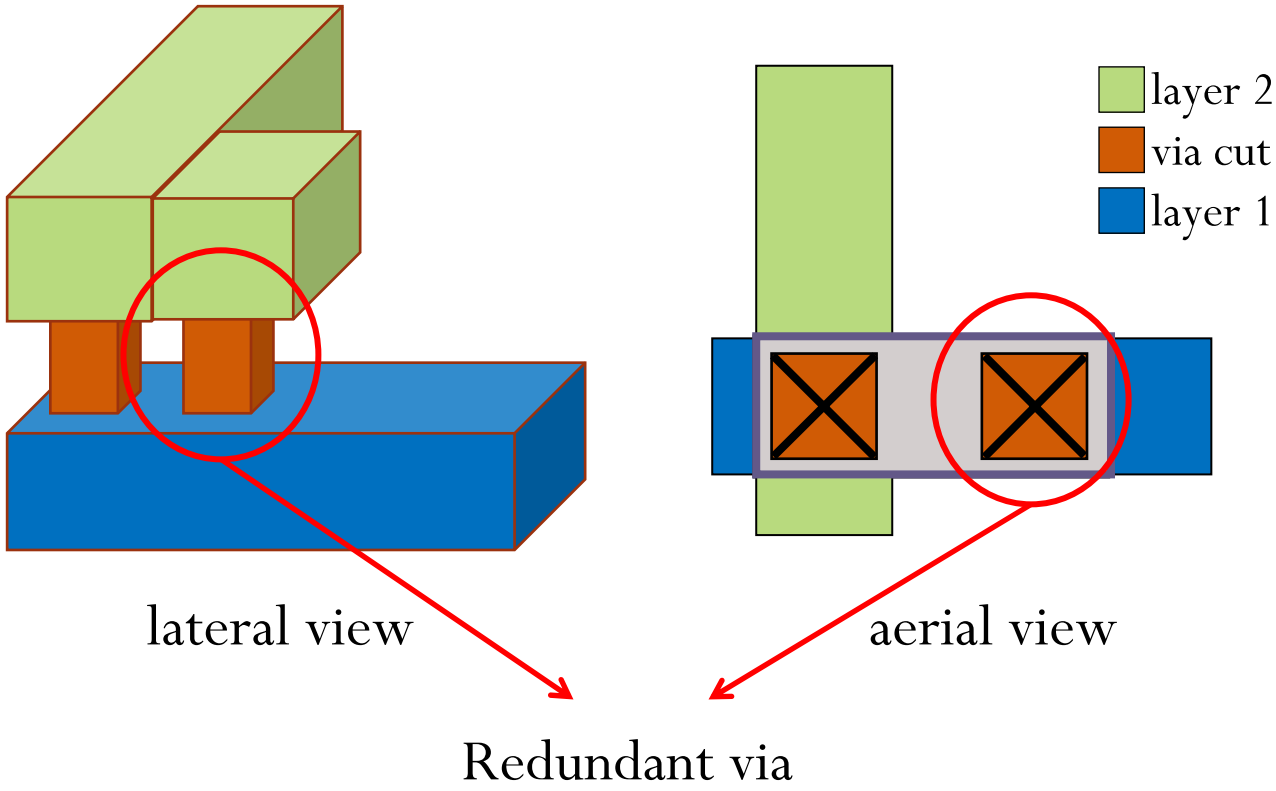
Outline

- **Introduction**
- Preliminaries and Problem Definition
- Conflict Graph Construction
- ILP Approach
- Experimental Results
- Conclusion

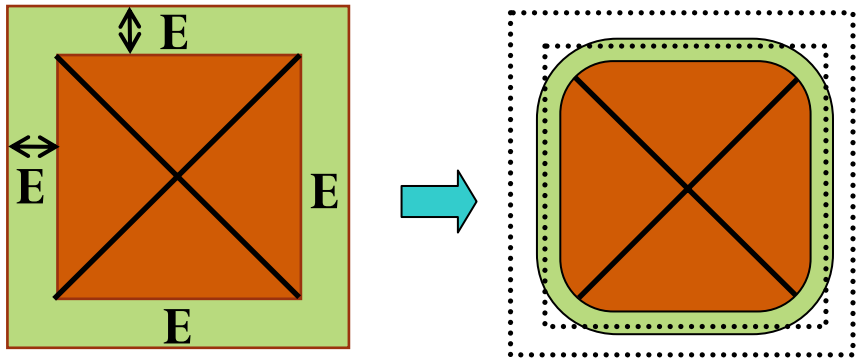
Introduction

- One popular topic of DFM is to minimize the chip failure rate caused by via defects.
- Reducing via defects and improving IC yield can be done by techniques such as **redundant via insertion** and **line end extension**.

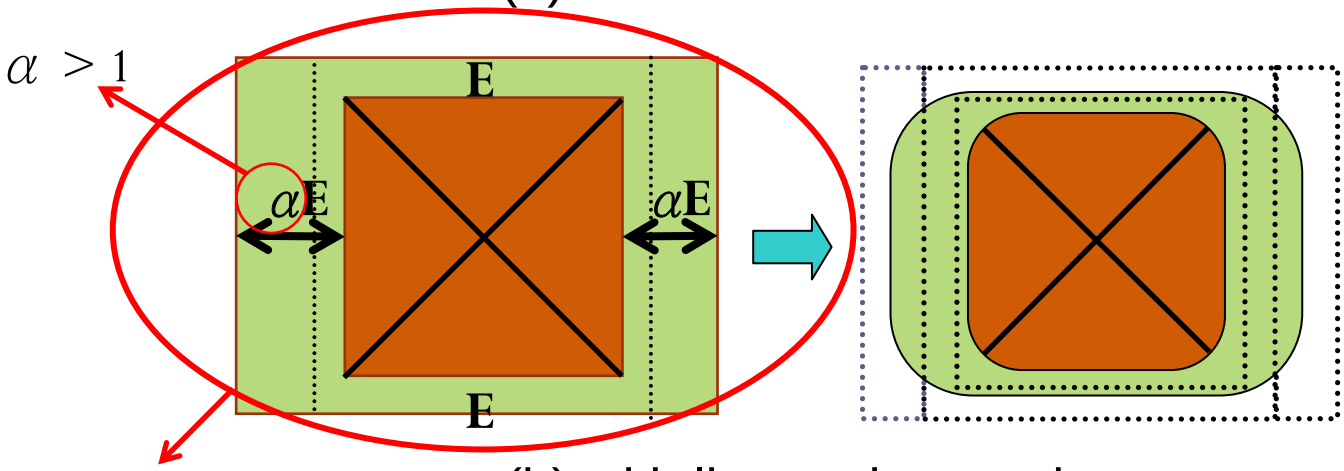
Redundant Via Insertion



Line End Extension



(a) without line end extension



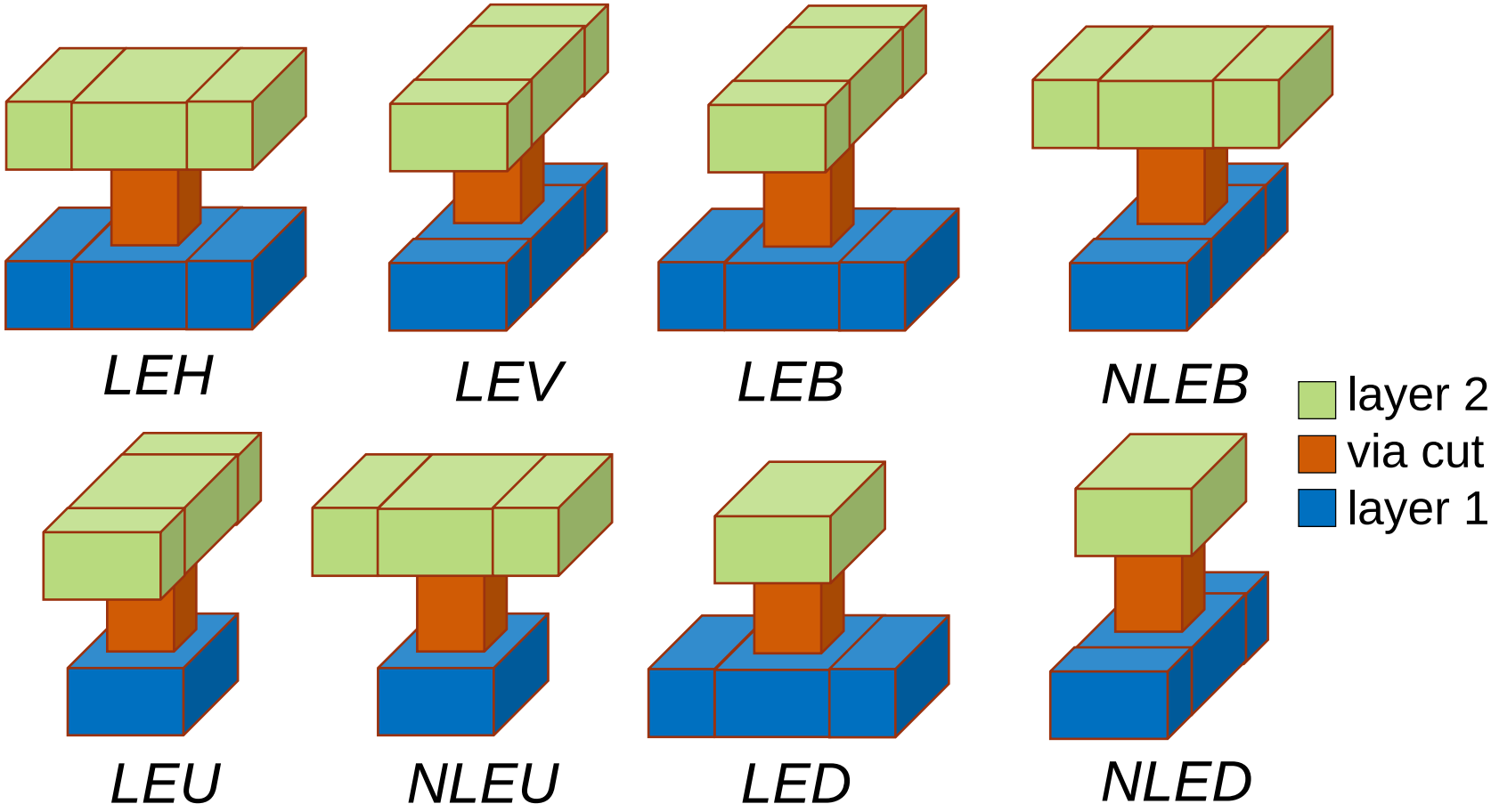
Line End Extended Via (*LEEV*)

(b) with line end extension

[ICCAD '06] K.-Y. Lee, T.-C. Wang, and K.-Y. Chao, "Post-routing redundant via insertion and line end extension with via density consideration," in *Proceedings of International Conference on Computer-Aided Design,* 2006

Line End Extension (Cont'd)

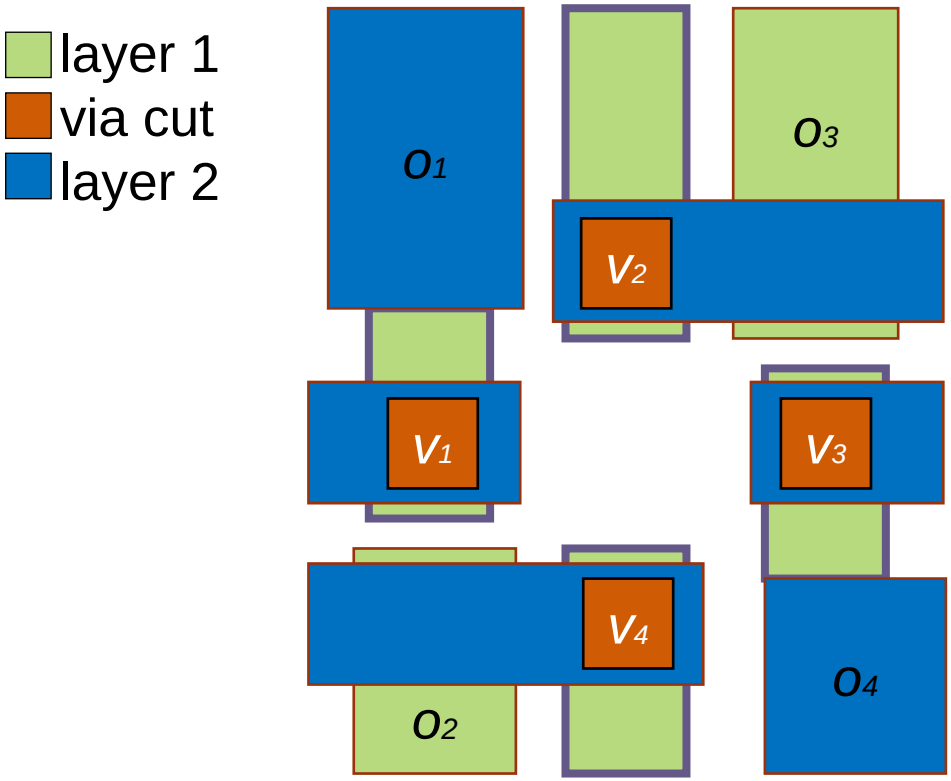
- Eight types



Motivating Example

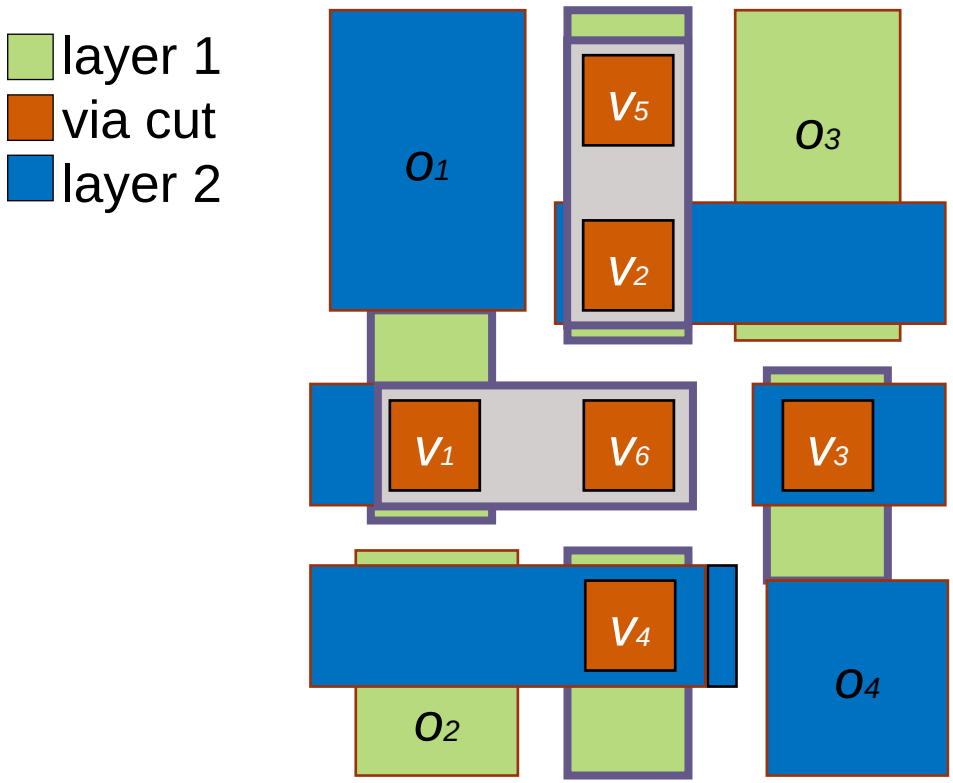
- Four single vias (v_1, v_2, v_3, v_4) and four obstacles (o_1, o_2, o_3, o_4).
- Failure probabilities

Single via	Redundant via	*LEB*	*LEH/LEV*
0.005	0.0001	0.0003	0.0006



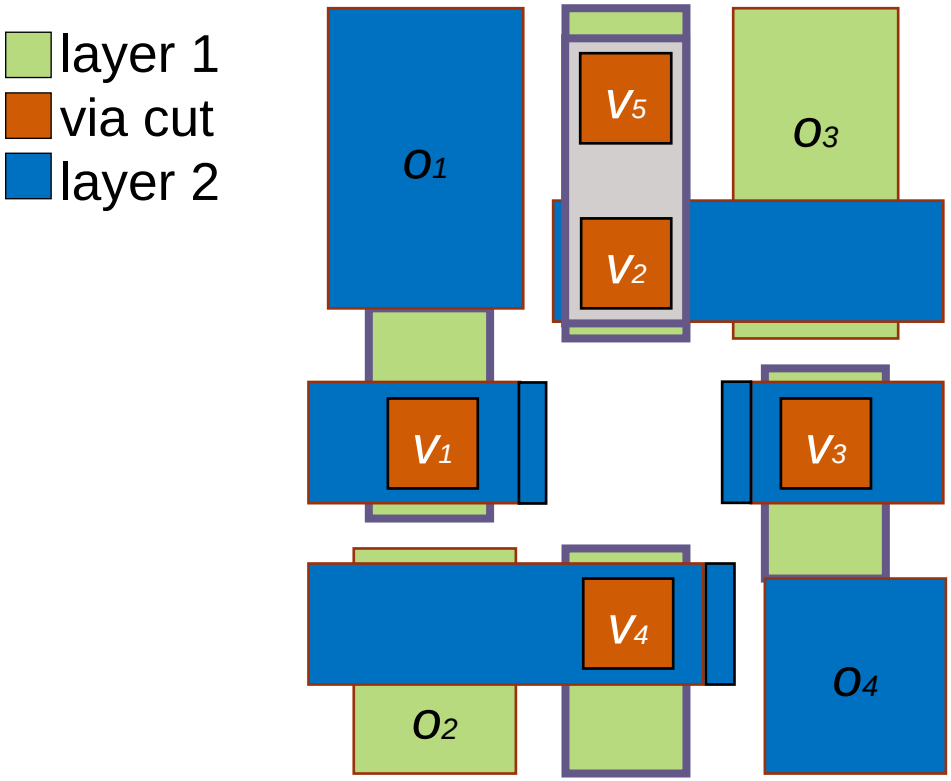
Motivating Example – Case A ([ICCAD '06])

- Two redundant vias.
- One line end extension (*LEH*).
- Via yield = $(1-0.005)\times(1-0.0001)^2\times(1-0.0006) = 0.9942$



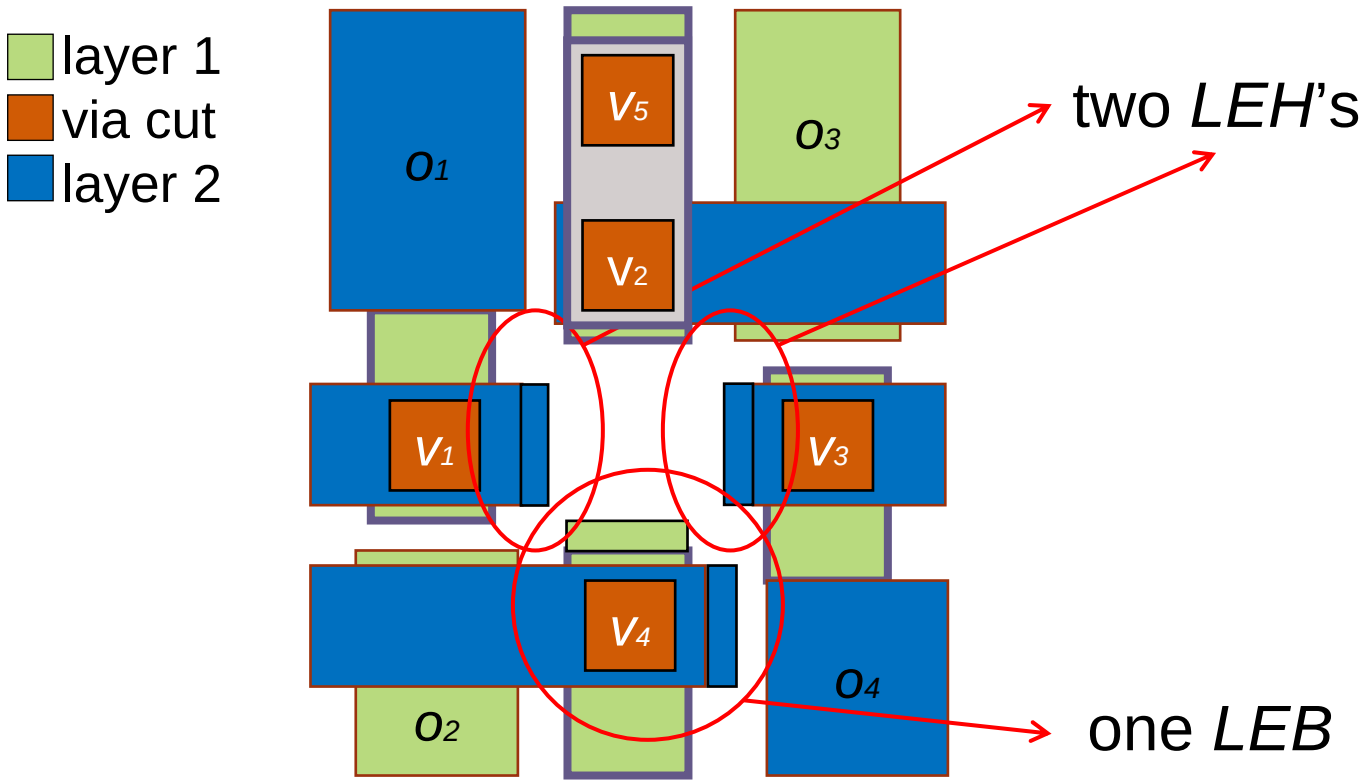
Motivating Example – Case B

- One redundant via.
- Three line end extensions (*LEH*).
- Via yield = $(1\text{-}0.0001)\times(1\text{-}0.0006)^3 = 0.9981$



Motivating Example – Case C (using our algorithm)

- One redundant via
- Three line end extensions (one *LEB* via and two *LEH* vias)
- Via yield = $(1\text{-}0.0001)\times(1\text{-}0.0003)\times(1\text{-}0.0006)^2 = 0.9984$



Our Contributions

- Considering eight types of line end extensions.
- Formulating a via yield optimization problem by simultaneous Redundant Via Insertion and Line End Extension (RVI/LEE).
- Proposing a zero-one Integer Linear Program (0-1 ILP) based approach to solve the RVI/LEE problem optimally.
- Using two speedup techniques to reduce runtime.
- Providing extensive experimental results to support our apporach.

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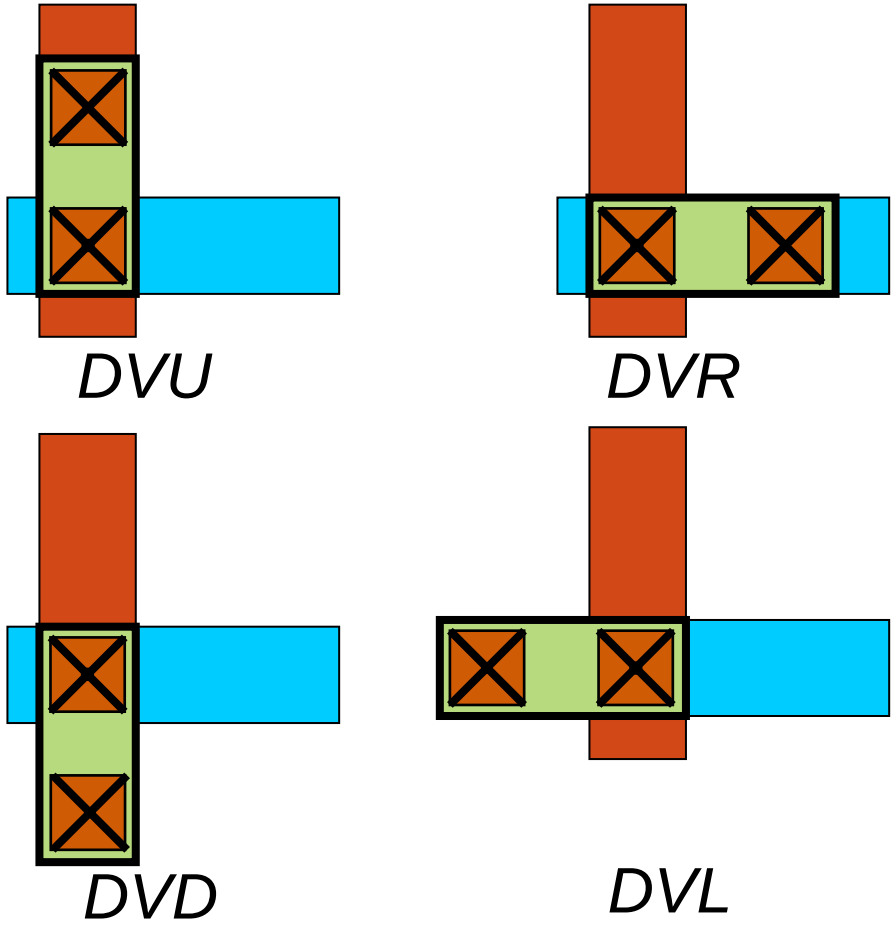
Double Via (DV)

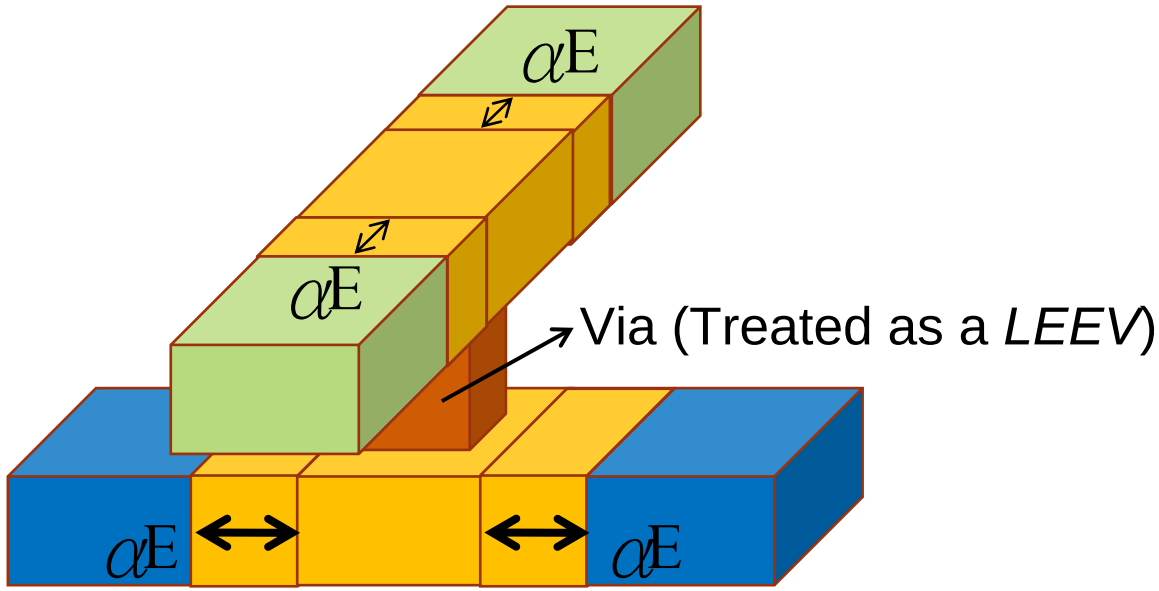
- Four types



- Feasible Double Via (*fDV*)
  - No violation of any design rule

Line End Extended Via (LEEV)

- Eight types (*LEH*, *LEV*, *LEB*, *NLEB*, *LEU*, *NLEU*, *LED*, and *NLED*)
- Feasible Line End Extended Via (*fLEEV*)
  - No violation of any design rule
- Special cases



Failure Probabilities

- Thirteen types of vias
  - *DVU*, *DVR*, *DVD*, *DVL*
  - *LEH*, *LEV*, *LEB*, *NLEB*, *LEU*, *NLEU*, *LED*, *NLED*
  - Single Via type (*SV*)
- Each type of via has an independent failure probability.
- Via yield is computed by the product of non-failure probabilities of all vias.

Problem Definition

- RVI/LEE problem
  - Given a routed design, maximizing the **via yield** of the design by **Redundant Via Insertion** and **Line End Extension**.
- Via yield model

$$Yield = \prod_{i \in AV} (1 - Prob(vt(i)))$$

  - *AV*: the set of all single vias in the original layout.
  - *vt*(*i*): the resultant via type of *i* after redundant via insertion and line end extension.

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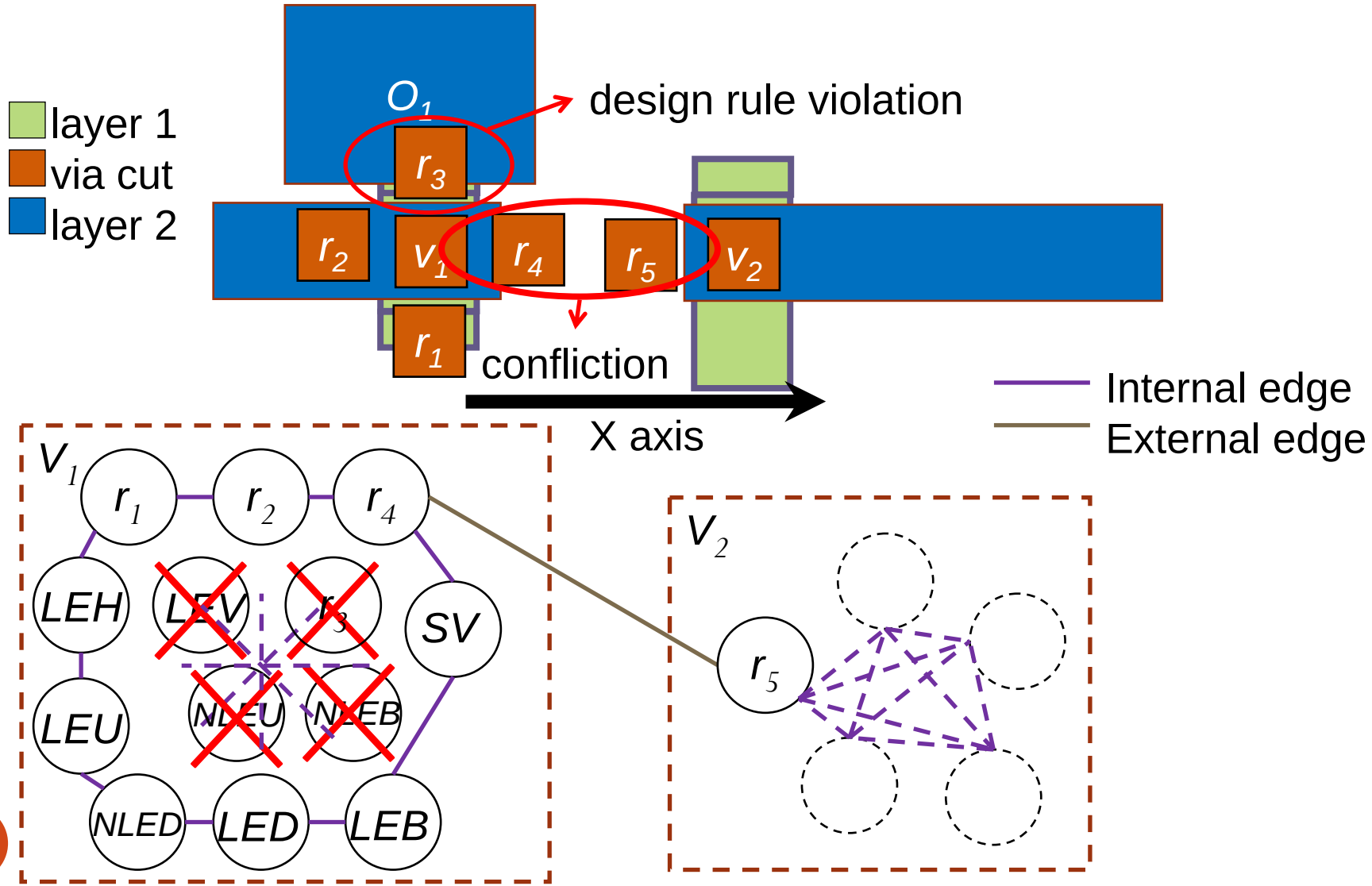
Conflict Graph (CG)

- $CG(V, E = E_I \cup E_X)$
- Vertex set V
  - At most thirteen vertices (four *fDV* vertices, eight *fLEEV* vertices, one *SV* vertex) for each single via.
- Edge set E
  - An edge exists if two end vertices cannot be chosen simultaneously.
  - Internal edge set E_I: each edge connects two vertices from the same single via.
  - External edge set E_X: each edge connects two vertices from different single vias.

Construction of CG



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0-1 ILP Formulation

$$Yield = \prod_{i \in AV} (1 - Prob(vt(i)))$$

$$\log Yield = \log(\prod_{i \in AV} (1 - Prob(vt(i))))$$

$$= \sum_{i \in AV} \log(1 - Prob(vt(i)))$$

$$= \sum_{i \in AV} \left[\sum_{v_{i,j} \in V_i} r_{i,j} \times \log\left(1 - Prob\left(t(v_{i,j})\right)\right) \right.$$

V_i: the set of vertices that originate from single via i.

$t(v_{i,j})$: via type of vertex $v_{i,j}$.

$r_{i,j}$: binary variable (1: $v_{i,j}$ is chosen; 0: $v_{i,j}$ is not chosen)

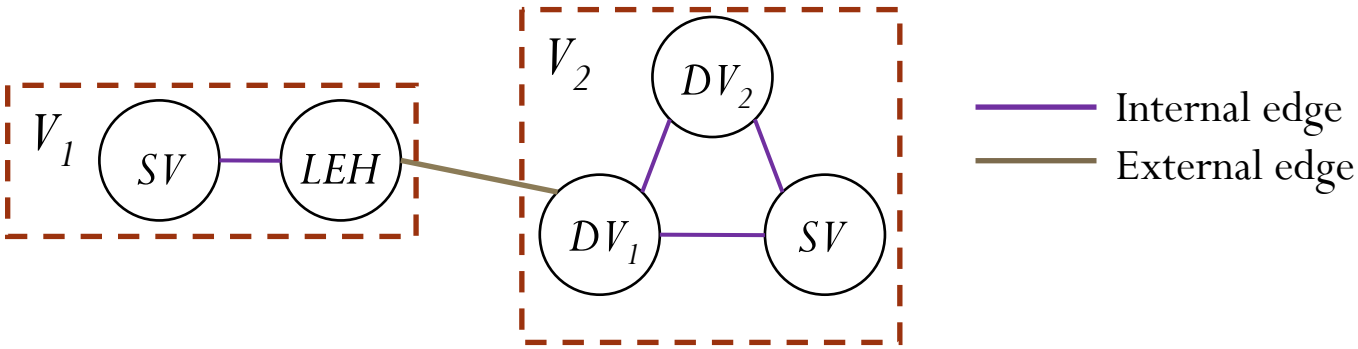
0-1 ILP Formulation (cont'd)

$$\max \sum_{i \in AV} \left[\sum_{v_{i,j} \in V_i} r_{i,j} \times \log\left(1 - Prob\left(t\left(v_{i,j}\right)\right)\right) \right]$$

Subject to: $r_{i,j} \in \{0,1\}$ $\quad \forall\, i \in AV, \forall\, v_{i,j} \in V_i$

$$\sum_{v_{i,j} \in V_i} r_{i,j} \leq 1 \qquad \forall\, i \in AV$$

$$r_{i,j} + r_{i',j'} \leq 1 \qquad \forall \left(v_{i,j}, v_{i',j'}\right) \in E_x$$



$$AV = \{V_1, V_2\}$$

$$V_1 = \{v_{1,SV}, v_{1,LEH}\}$$

$$V_2 = \{v_{2,DV1}, v_{2,DV2}, v_{2,SV}\}$$

$$\max \; r_{1,SV} \times \log(1\text{-}Prob(t(v_{1,SV}))) + r_{1,LEH} \times \log(1\text{-}Prob(t(v_{1,LEH})))$$
$$+ r_{2,DV1} \times \log(1\text{-}Prob(t(v_{2,DV1}))) + r_{2,DV2} \times \log(1\text{-}Prob(t(v_{2,DV2})))$$
$$+ r_{2,SV} \times \log(1\text{-}Prob(t(v_{2,SV})))$$

subject to:

$$r_{1,SV} = \{0,1\} \quad r_{1,LEH} = \{0,1\} \quad r_{2,DV2} = \{0,1\} \quad r_{2,DV3} = \{0,1\} \quad r_{2,SV} = \{0,1\}$$

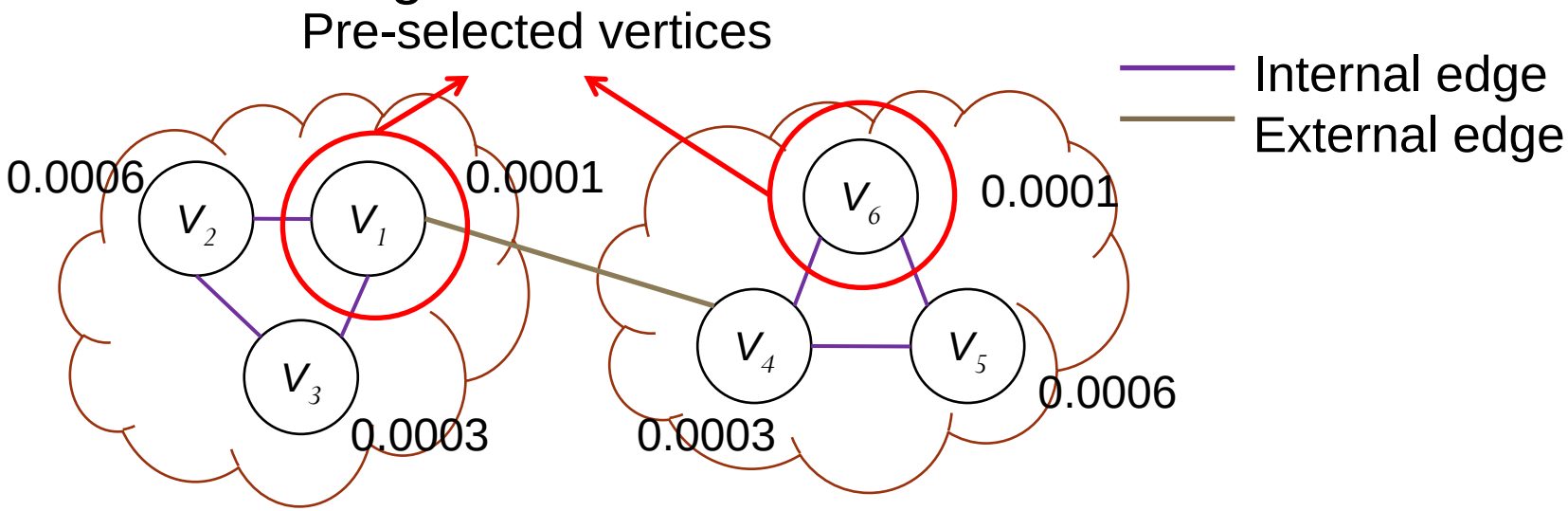
$$r_{1,SV} + r_{1,LEH} = 1$$

$$r_{2,DV1} + r_{2,DV2} + r_{2,SV} = 1$$

$$r_{1,LEH} + r_{2,DV1} \leq 1$$

Speedup Methods (Pre-selection)

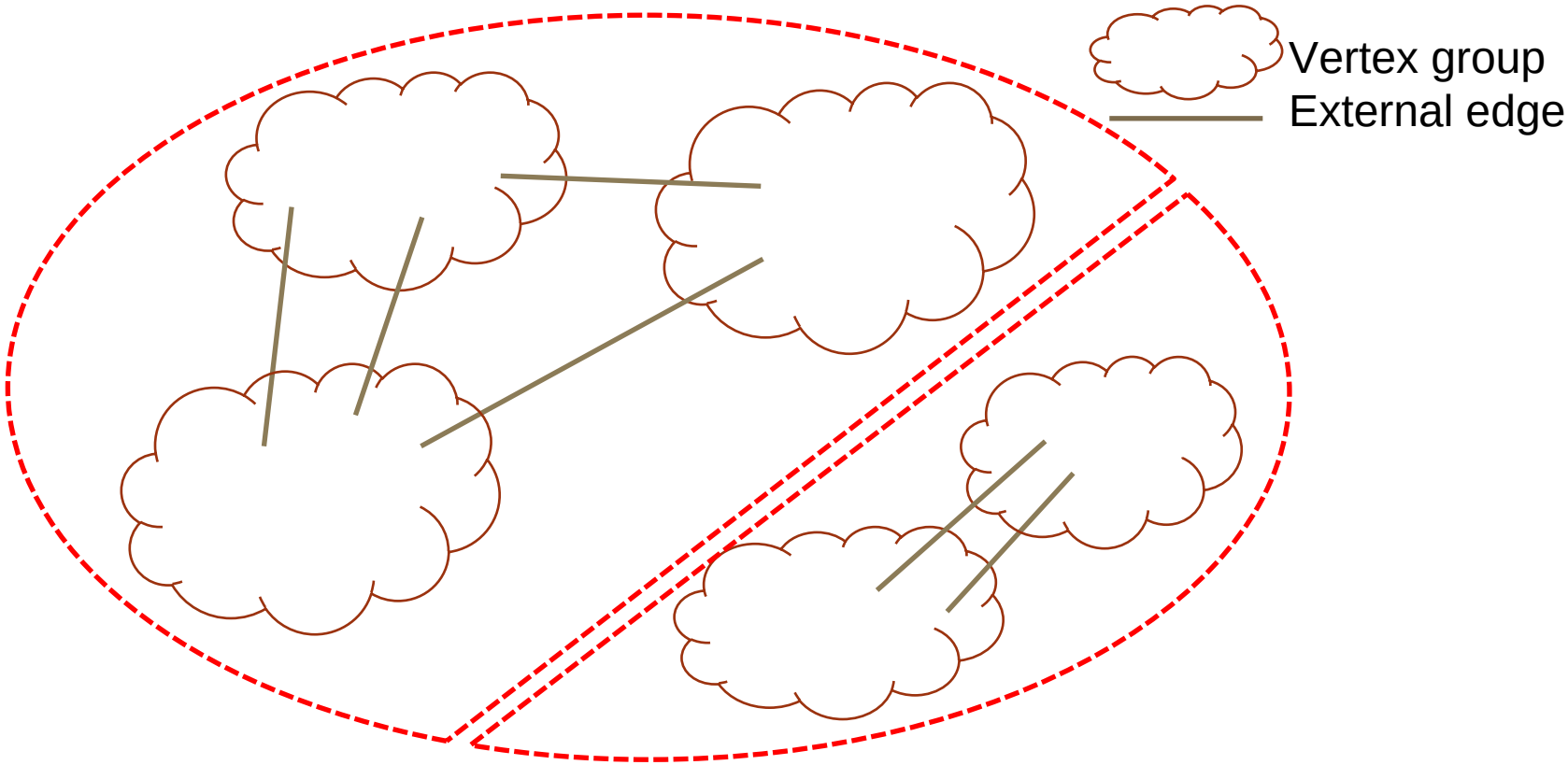
- Pre-selection
  - Reducing *CG* size.
  - A vertex can be pre-selected if its failure probability is the lowest almost all vertices originating from the same single via and it is not connected by any external edges.



Pre-select v_6 first, then pre-select v_1.

Speedup Methods (Connected Components)

- Connected components
  - Each is separately solved by a 0-1 ILP.



Two connected components.

Speedup Methods (Cont'd)

- Overall approach
  - First reducing the size of the conflict graph by pre-selecting vertices.
  - Then dividing the remaining graph into connected components, and using the 0-1 ILP approach for every connected component.
  - At the end, collecting all the individual solutions of connected components and the pre-selected vertices to produce the final solution.

Extension

- RVI/LEH problem [ICCAD '06]
  - Objectives: to first insert as many redundant vias as possible and to then replace as many remaining single vias by *LEH* vias as possible.
- Modifications
  - *CG*: keeping vertices of double vias, *LEH*'s, and *SV*'s as well as their associated edges.
  - Objective function of 0-1 ILP:

$$\max \sum_{i \in AV} \{C_1 \times \sum_{v_{i,j} \in DV_i} r_{i,j} \times \log(1 - Prob(DV))$$

$$+C_2 \times \sum_{v_{i,j} \in LEH_i} r_{i,j} \times \log(1 - Prob(LEH))$$

$$+C_3 \times \sum_{v_{i,j} \in V_i - DV_i - LEH_i} r_{i,j} \times \log(1 - Prob(SV))\}$$

$$C_3 < 0$$

$$C_2 < C_3 \times \frac{\log(1-Prob(SV))}{\log(1-Prob(LEH))} \times (|AV| + 1)$$

$$C_1 < \frac{C_2 \times \log(1-Prob(LEH)) - \log(1-Prob(SV))}{\log(1-Prob(DV))} \times (|AV| + 1)$$

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Experiment Platform and Test Cases

- CPU: 2.4GHz
- RAM: 8GB
- ILP solver: lp_solve

Circuit	#Layers	#Nets	#Vias	#Objects
struct	3	1920	7598	39984
primary1	3	904	5536	26911
primary2	3	3029	23154	110776
s5378	3	1694	6739	35117
s9234	3	1478	5365	28985
s13207	3	3778	13972	75080
s15850	3	4471	16922	90085
s38417	3	11309	40942	221006
s38584	3	14754	55381	297442
mcc1	4	802	5948	26852
mcc2	4	7118	34376	154560
C1	5	4309	24594	267403
C2	5	5252	41157	350983
C3	5	18157	127059	1187970
C4	5	17692	151912	1237897
C5	5	44720	357386	3566384
dma_dfm	6	13256	108401	100699
dsp1_dfm	6	28447	223550	182326
dsp2_dfm	6	28431	232613	191614
risc1_dfm	6	34034	344391	294973
risc2_dfm	6	34034	350558	294500

Failure Probabilities

Prob(SV)	*Prob(DV)*	*Prob(LEB)*	*Prob(NLEB)*
5E-6	(5E-6)/40	(5E-6)/11	(5E-6)/10

Prob(LEH)|Prob(LEV)	*Prob(LEU)|Prob(LED)*
(5E-6)/8	(5E-6)/6

Prob(NLEU)|Prob(NLED)
(5E-6)/5

Yield Comparison (Original vs. Ours)

	Original							Ours							
Circuit	SV	NLEU+ NLED	LEU/ LED	NLEB	LEH/ LEV	LEB	Yield	SV	NLEU+ NLED	LEU+ LED	NLEB	LEH+ LEV	LEB	DV	Yield
struct	7425	0	173	0	0	0	96.34%	3	0	14	0	0	1	7580	99.90%
primary1	5333	0	203	0	0	0	97.35%	0	1	37	0	0	4	5494	99.93%
primary2	22316	0	838	0	0	0	89.38%	17	0	221	0	0	48	22868	99.69%
s5378	6559	0	180	0	0	0	96.76%	35	4	87	0	2	82	6529	99.89%
s9234	5239	0	126	0	0	0	97.40%	23	1	81	0	0	49	5211	99.91%
s13207	13573	0	399	0	0	0	93.41%	50	5	181	0	4	148	13584	99.78%
s15850	16465	0	457	0	0	0	92.06%	69	7	265	0	4	191	16386	99.73%
s38417	39692	0	1250	0	0	0	81.91%	170	25	549	1	8	385	39804	99.35%
s38584	53526	0	1855	0	0	0	76.40%	256	25	788	0	19	558	53735	99.11%
mcc1	5056	22	121	749	0	0	97.45%	8	3	80	1	2	176	5678	99.91%
mcc2	29125	26	64	5161	0	0	86.16%	62	1	802	1417	3	20	32071	99.41%
C1	24216	7	371	0	0	0	88.57%	1108	848	1888	63	467	525	19695	98.91%
C2	40039	0	1118	0	0	0	81.78%	3835	2213	2747	31	393	654	31284	97.23%
C3	124112	2	2945	0	0	0	53.63%	10041	6036	10540	64	367	1513	98498	92.47%
C4	142954	0	8958	0	0	0	48.57%	12866	8535	15212	64	840	3546	110849	90.35%
C5	347669	7	9710	0	0	0	17.44%	25058	12505	30717	97	4366	10499	274144	81.47%
dma_dfm	106041	2315	45	0	0	0	58.71%	875	298	4645	21	151	2741	99670	97.79%
dsp1_dfm	220094	3293	163	0	0	0	33.16%	4150	1667	30830	151	760	6335	179657	92.87%
dsp2_dfm	229969	2487	157	0	0	0	31.59%	4114	1663	29999	107	699	7164	188867	92.82%
risc1_dfm	339283	5020	88	0	0	0	18.24%	4775	2171	32931	301	985	12074	291154	90.84%
risc2_dfm	343012	7458	88	0	0	0	17.86%	5587	2622	39010	363	1104	12233	289639	89.97%
Normalized	1						1	0.02							1.91

1

1.91

Yield Comparison (RVI vs. Ours)

	RVI								Ours							
Circuit	SV	NLEU+ NLED	LEU+ LED	NLEB	LEH+ LEV	LEB	DV	Yield	SV	NLEU+ NLED	LEU+ LED	NLEB	LEH+ LEV	LEB	DV	Yield
struct	18	0	0	0	0	0	7580	99.90%	3	0	14	0	0	1	7580	99.90%
primary1	40	0	1	0	0	0	5495	99.91%	0	1	37	0	0	4	5494	99.93%
primary2	274	0	3	0	0	0	22877	99.58%	17	0	221	0	0	48	22868	99.69%
s5378	198	0	3	0	0	0	6538	99.82%	35	4	87	0	2	82	6529	99.89%
s9234	149	0	0	0	0	0	5216	99.86%	23	1	81	0	0	49	5211	99.91%
s13207	375	0	3	0	0	0	13594	99.64%	50	5	181	0	4	148	13584	99.78%
s15850	513	0	3	0	0	0	16406	99.54%	69	7	265	0	4	191	16386	99.73%
s38417	1081	0	6	0	0	0	39855	98.97%	170	25	549	1	8	385	39804	99.35%
s38584	1565	0	14	0	0	0	53802	98.55%	256	25	788	0	19	558	53735	99.11%
mcc1	247	1	2	16	0	0	5682	99.80%	8	3	80	1	2	176	5678	99.91%
mcc2	1908	2	3	284	0	0	32179	98.63%	62	1	802	1417	3	20	32071	99.41%
C1	4810	0	30	0	0	0	19754	97.38%	1108	848	1888	63	467	525	19695	98.91%
C2	9714	0	32	0	0	0	31411	94.88%	3835	2213	2747	31	393	654	31284	97.23%
C3	28088	0	83	0	0	0	98888	85.82%	10041	6036	10540	64	367	1513	98498	92.47%
C4	39466	0	789	0	0	0	111657	80.90%	12866	8535	15212	64	840	3546	110849	90.35%
C5	81400	0	549	0	0	0	275437	64.28%	25058	12505	30717	97	4366	10499	274144	81.47%
dma_dfm	8246	32	7	0	0	0	100116	94.76%	875	298	4645	21	151	2741	99670	97.79%
dsp1_dfm	42421	137	51	0	0	0	180941	79.06%	4150	1667	30830	151	760	6335	179657	92.87%
dsp2_dfm	42273	92	44	0	0	0	190204	79.04%	4114	1663	29999	107	699	7164	188867	92.82%
risc1_dfm	51171	395	29	0	0	0	292796	74.61%	4775	2171	32931	301	985	12074	291154	90.84%
risc2_dfm	58337	419	33	0	0	0	291769	71.99%	5587	2622	39010	363	1104	12233	289639	89.97%
Normalized	0.11							1.71	0.02							1.91

1.71

1.91

CG Information (RVI vs. Ours)

	RVI			Ours		
Circuit	Nodes	Edges	Time (s)	Nodes	Edges	Time (s)
struct	24112	29440	1.4	66181	313310	3.86
primary1	15922	17845	0.85	43288	190936	2.38
primary2	63410	67617	3.95	171738	723978	11
s5378	16479	16827	1.39	45017	174191	4.02
s9234	13408	13843	1.11	36557	143390	3.22
s13207	34536	34885	3.48	95304	367716	9.5
s15850	41153	41327	4.18	113373	435579	11.06
s38417	100942	102277	11.2	277394	1075496	28.42
s38584	135146	136004	18.48	369109	1411406	39.78
mcc1	13770	13212	1.67	42511	166815	4.62
mcc2	75730	69017	11.2	229029	836759	23.98
C1	43246	53564	10.65	122804	393763	16.98
C2	67312	54376	11.74	187404	571140	25.35
C3	215647	179307	42.09	589164	1845152	85.31
C4	220538	159691	45.17	617188	1704640	92.95
C5	574142	444754	130.48	1619410	4754188	256.66
dma_dfm	214961	182628	31.26	610020	2065947	72.94
dsp1_dfm	367578	297176	71.45	1094016	3522803	185.54
dsp2_dfm	385204	306133	74.29	1143760	3625584	159.92
risc1_dfm	584185	447912	128.87	1740405	5385784	246.99
risc2_dfm	562965	420460	127.93	1700580	5190739	243.25
Normalized	1	1	1	2.83	10.87	2.37

Runtime Comparison (RVI vs. Ours)

	RVI		Ours	
Circuit	Graph time (s)	Solving time (s)	Graph time (s)	Solving time (s)
struct	1.4	0.09	3.86	0.10
primary1	0.85	3.13	2.38	3.16
primary2	3.95	3.41	11	3.53
s5378	1.39	3.14	4.02	3.19
s9234	1.11	3.13	3.22	3.16
s13207	3.48	3.28	9.5	3.35
s15850	4.18	3.35	11.06	3.46
s38417	11.2	3.78	28.42	3.96
s38584	18.48	4.03	39.78	4.18
mcc1	1.67	3.17	4.62	3.17
mcc2	11.2	3.83	23.98	3.87
C1	10.65	3.41	16.98	3.51
C2	11.74	3.62	25.35	3.75
C3	42.09	4.87	85.31	5.13
C4	45.17	5.22	92.95	5.70
C5	130.48	7.81	256.66	9.81
dma_dfm	31.26	5.21	72.94	5.16
dsp1_dfm	71.45	7.71	185.54	7.24
dsp2_dfm	74.29	7.74	159.92	7.21
risc1_dfm	128.87	9.45	246.99	9.45
risc2_dfm	127.93	10.38	243.25	9.55
Normalized	1	1	2.37	1.03

RVI/LEH Results ([ICCAD '06] vs. Ours)

	[ICCAD 06]									Ours								
Circuit	SV	NLEU+ NLED	LEU+ LED	NLEB	LEV	LEB	LEH	DV	Yield	SV	NLEU+ NLED	LEU+ LED	NLEB	LEV	LEB	LEH	DV	Yield
struct	18	0	0	0	0	0	0	7580	99.90%	18	0	0	0	0	0	0	7580	99.90%
primary1	40	0	1	0	0	0	0	5495	99.91%	40	0	1	0	0	0	0	5495	99.91%
primary2	274	0	2	0	0	0	1	22877	99.58%	274	0	2	0	0	0	1	22877	99.58%
s5378	208	0	4	0	0	0	0	6527	99.81%	198	0	3	0	0	0	0	6538	99.82%
s9234	152	0	0	0	0	0	1	5212	99.86%	148	0	0	0	0	0	1	5216	99.86%
s13207	376	0	3	0	0	0	4	13589	99.64%	372	0	3	0	0	0	3	13594	99.64%
s15850	520	0	3	0	0	0	0	16399	99.54%	513	0	3	0	0	0	0	16406	99.54%
s38417	1083	0	7	0	0	0	4	39848	98.96%	1077	0	6	0	0	0	4	39855	98.97%
s38584	1573	0	15	0	0	0	3	53790	98.55%	1562	0	14	0	0	0	3	53802	98.56%
mcc1	229	1	1	17	0	0	19	5681	99.81%	229	1	1	16	0	0	19	5682	99.81%
mcc2	1909	2	3	287	0	0	3	32172	98.63%	1906	2	3	283	0	0	3	32179	98.64%
C1	4602	1	30	0	0	0	207	19754	97.47%	4602	1	30	0	0	0	207	19754	97.47%
C2	9713	0	32	0	0	0	1	31411	94.88%	9713	0	32	0	0	0	1	31411	94.88%
C3	28018	0	83	0	0	0	77	98881	85.85%	28011	0	83	0	0	0	77	98888	85.85%
C4	39459	0	791	0	0	0	18	111644	80.90%	39448	0	789	0	0	0	18	111657	80.91%
C5	80088	0	552	0	0	0	1320	275426	64.66%	80080	0	0	0	0	0	1869	275437	64.67%
dma_dfm	8038	33	7	0	0	0	227	100096	94.85%	8012	32	7	0	0	0	234	100116	94.86%
dsp1_dfm	41714	148	30	0	0	0	746	180912	79.31%	41668	134	31	0	0	0	776	180941	79.33%
dsp2_dfm	41583	98	33	0	0	0	735	190164	79.28%	41526	91	33	0	0	0	759	190204	79.30%
risc1_dfm	49611	397	17	0	0	0	1612	292754	75.13%	49531	0	0	0	0	0	2064	292796	75.17%
risc2_dfm	56683	420	26	0	0	0	1726	291703	72.52%	56571	0	0	0	0	0	2218	291769	72.57%
Normalized									1.71									1.71

Outline

- Introduction
- Preliminaries and Problem Definition
- Conflict Graph Construction
- ILP Approach
- Experimental Results
- **Conclusion**

Conclusion

- We have formulated a problem of simultaneous redundant via insertion and line end extension.
  - More than one type of line end extension is considered.
  - The objective function to be optimized directly accounts for via yield.
- We have presented a 0-1 ILP based approach.
  - Equipped with two speedup techniques.
- Extensive experimental results have been shown to support our approach.