Variation-Tolerant and Self-Repair Design Methodology for LTPS LCD and OLED Display

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- Introduction
- Proposed System
 - Detector
 - Memory Unit
 - CLK Generator
- Device Modeling
- Simulation Results
 - Conclusion

Outline

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Introduction

Emerging Displays3D Display

- More attractive and exciting experience
- Touch Display
 - Intuitive Screen Operation
- Memory-Integrated Display
 - Low Power consumption
- Photo-Sensor Display
 - Scan and Security









 Low transmittance of pixel circuit
~70% of power consumption of LCD module comes from backlight

Scaling of Device Size is Important

Scaling Issues in Poly-Si TFT

Device Degradation

- Hot carrier
- Self-heating

Process Variation

- > Variation of device parameters
- Grain boundary (GB) induced variation (dominant)





Random dopant fluctuation

Grain Boundary in Poly-Si TFT







- GB 🛛 Device Channel

- GB position is difficult to control
- GB acts as energy barrier for carriers
- Mobility and Vth depend on the number of GBs in channel
- GB Variation increases as device size decreases

Pixel Circuit: Parameter Variations



- Variation caused by insufficient drivability of pixel switches induces defective pixels
- Large supply voltage margin for addressing worst-case variability

Related Work

• Tile alignment

Uniformity is still bad as the size of device is comparable to the grain size

Multi-Finger

Not suitable for pixel switch considering the transmittance



- GB-induced variation is unavoidable
- System-level compensation technique is required

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Proposed Compensation Technique



- Charging time for defective pixels is extended
- Margin of supply voltage can either be decreased for lower power, or kept the same for higher yield
- Better reliability can be achieved

Proposed System



Operation Phases

Setup Phase

Setup the worse charging case for detection

Detection Phase

Determine and record the locations of defective pixel

Display Phase

Adaptive CLK is applied for compensation



Setup and detection phases performed only once

Detector Structure



- Data lines are precharged to the maximum level
- Charge sharing starts after one row of pixel switches is turned on by gate driver
- Voltage drop is detected by comparator
- If detective row contains defective pixel, a pulse is generated

Memory Unit Structure



Detection Phase

The output of the detector is recorded in SRAMs

Display Phase

The values in SRAMs are forwarded sequentially to CLK Gen.

CLK Generator Structure



• Five-bit Counter

Counting the number of defect rows

- CLK Selector
 - Selecting CLK according to four-bit counter
- Two-cycle Generator
 - Generating Adaptive CLK

Two Cycle Generator Structure



If output of memory unit is high (defective row)
Selected CLK is isolated from the output
Output value of previous cycle is held
If output of memory unit is low
Selected CLK proceeds without modification

Timing Diagram



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Device Modeling

Poisson area scatter distribution

$$\mathbf{P}(k) = \left[\exp(-\lambda) \cdot \lambda^k \right] / k!$$

k is Poisson random variable with mean λ
To correlate the average grain size (L_{g,TFT}) with k, k is assume to be the number of grains in this channel <-- L -->

$$k = (W \cdot L) / A_g$$
$$L_{g,TFT} = \sqrt{W \cdot L / k}$$



• Ag is the average area of one grain

[Wang, TED'2006]

Device Modeling (cont.)

Threshold Voltage Model

$$V_{th} = V_{FB} + \left[1 - \left(\frac{\varepsilon_{Si}E_{sc}L_{g,TFT}}{qN_{tr}L}\right)\right] \sqrt{\frac{8kTN_{tr}t_{ox}}{C_{ox}L_{g,TFT}}} \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{oxi}}}$$

Mobility Model

$$\mu = \left(\frac{l_{gb}}{L_{g,TFT}}\right) \cdot \mu_{gb,\Box} + \left[1 - \left(\frac{l_{gb}}{L_{g,TFT}}\right)\right] \mu_g$$
$$\mu_g = \mu_{gi} L_{eff} \left\{ (N-1) \left[l_{gi} + \left(\frac{\mu_{gi}}{\mu_{gb,\bot}}\right) l_{gb}\right] + L_{g,TFT} \right\}^{-1}$$

• Deviation of Vth and Mobility



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Panel Simulation Setting

Panel size (inch)	3.9	0.85	0.4
Switch TFT (W/L)	3/3µm	1/1µm	0.5/0.5µm
Resolution (H/V)	640/480		
Gray level	256		
V _{th} of LC (V)	3.3		
Refresh rate (Hz)	60		

- Three different sizes of TFT are evaluated
- Simulation results are obtained by Monte Carlo simulations (640x480x100)
- One pixel model with 12 sets of RC loading is applied for simplicity
- The power consumption is evaluated by HSPICE

Simulation Results

Smaller supply voltage (Iso yield : 99%)

Advantage becomes more apparent as the device size shrinks



2000

3µm

1µm

200

0.5µm

0

50

0

3µm

0.5µm

1µm

-5

Panel Simulation Results

Higher yield (Same supply voltage) > Better yield improvement as resolution increases



Better reliability

- Smaller supply voltage
- Self-repair capability as the three phases are redone

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Conclusion

An adaptive design technique for variation tolerant and self-repair display panel is reported

Adaptive CLK eliminates the need for large voltage margin

Lower power (up to 16%) for small sized display (less variation) or higher yield (up to 7%) for large sized and high resolution display (large variation) **THANK YOU**