Session 8D-2

Development of Low Power and High Performance Application Processor (T6G) for Multimedia Mobile Applications

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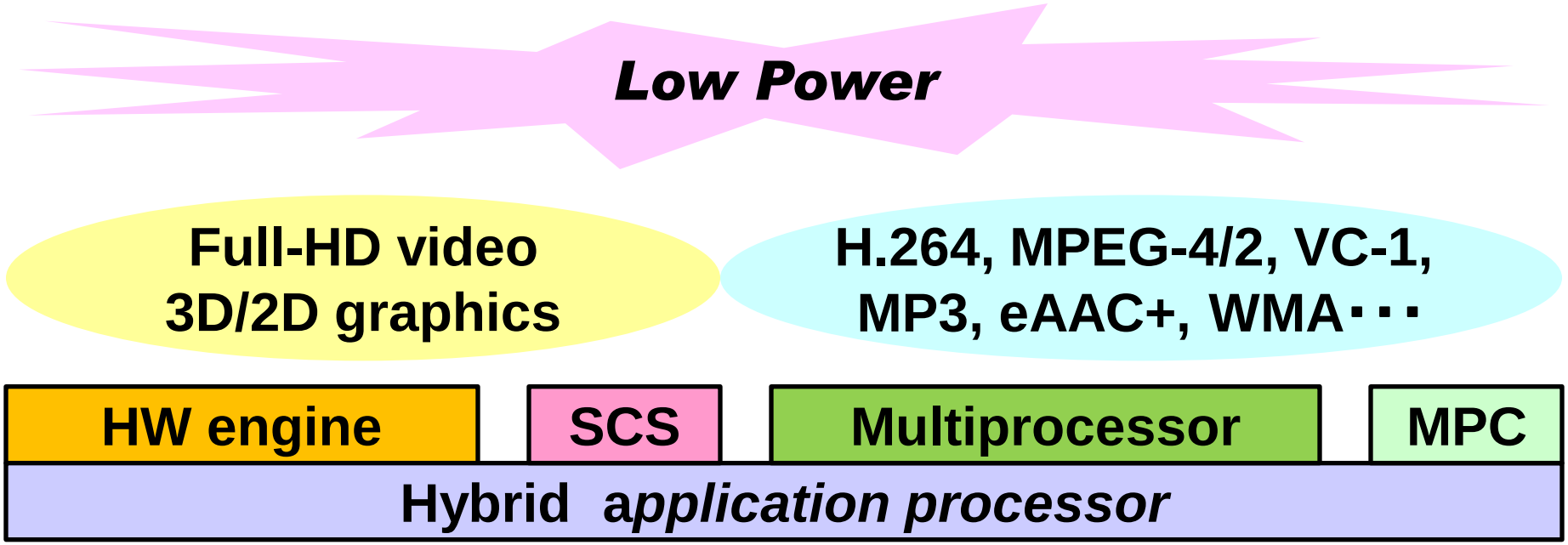
Outline

- Background
- Chip Overview
- Stacked DRAM Architecture
- Multiple Power Domain Control
- Chip Power Consumption
- Summary

Background

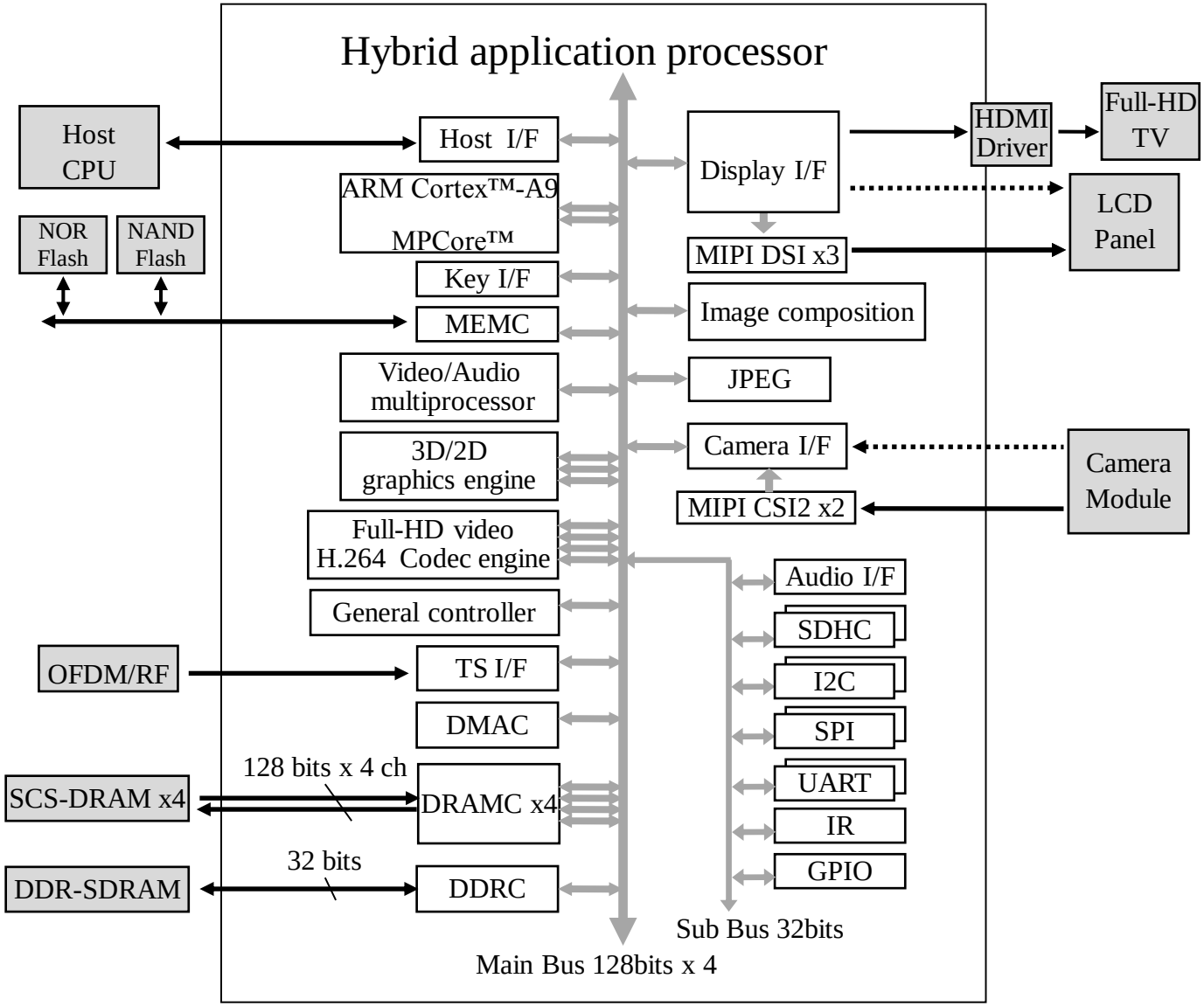
Chip Concept



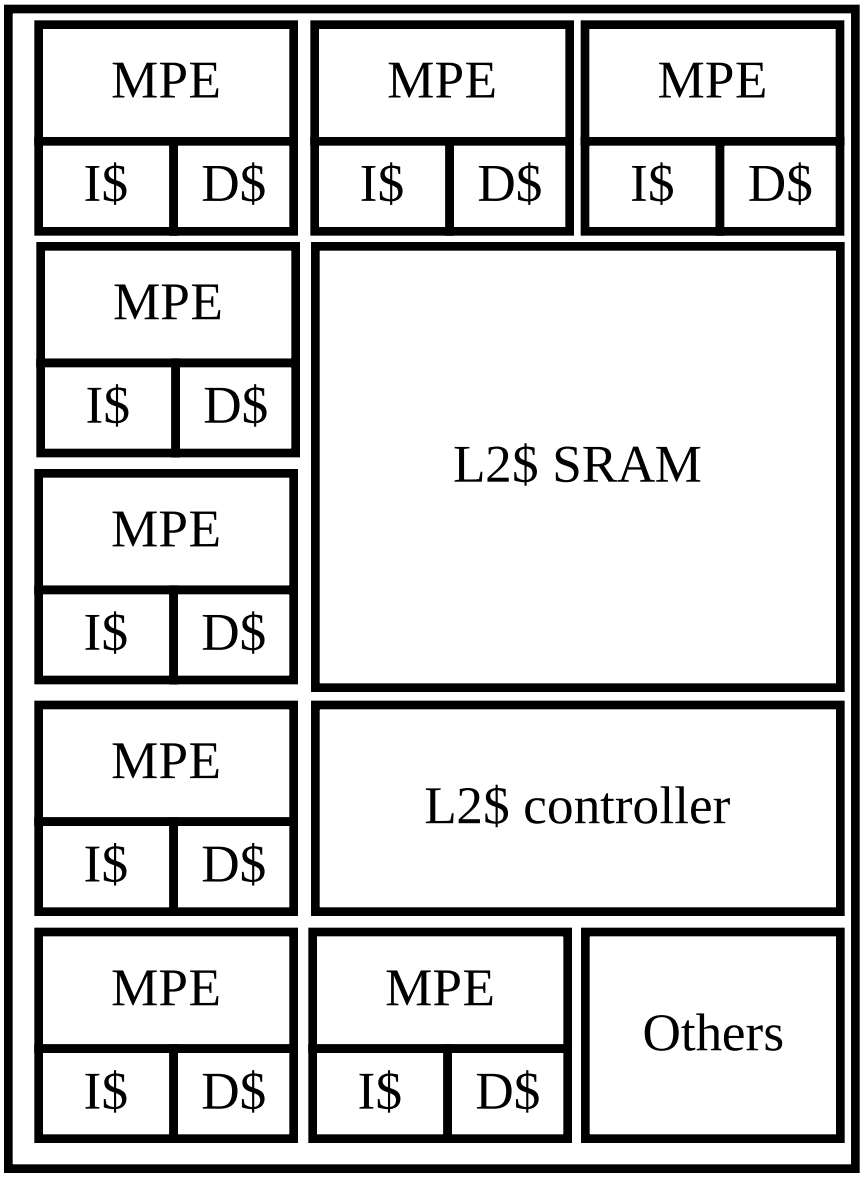
- HW engine : High performance (Full-HD video, 3D/2D graphics) & Low power
- Multiprocessor : Various multimedia applications (H.264, MPEG-4/2, VC-1, MP3, eAAC+, WMA …)
- Stacked Chip SoC (SCS) : High memory bandwidth & Low power
- Multiple Power domain Control (MPC) : Low power

Chip Overview

Block Diagram

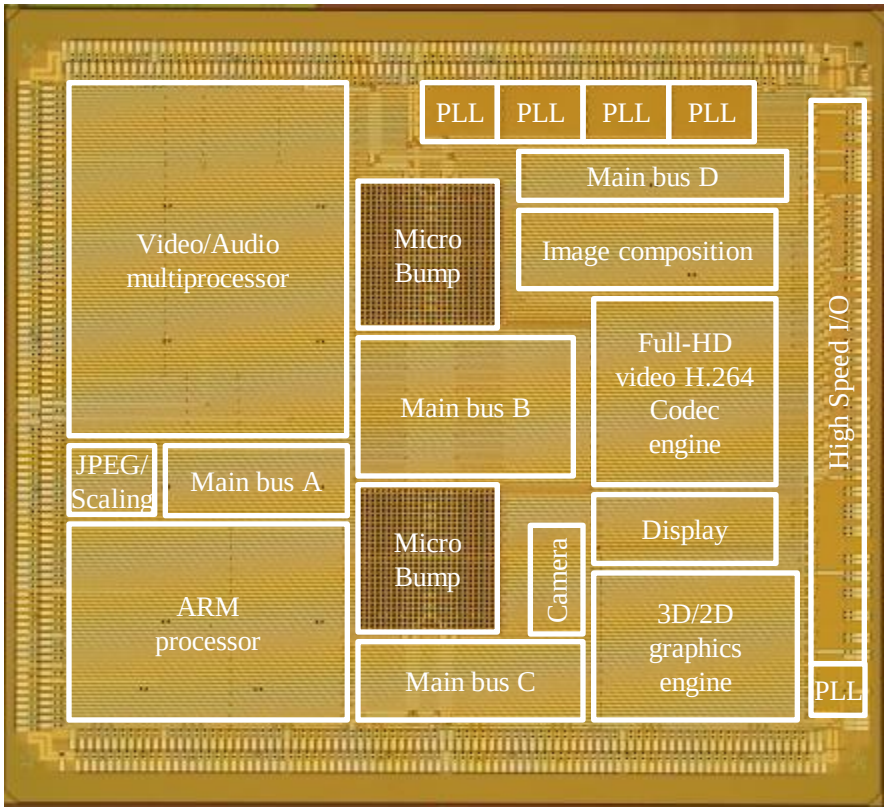


Video/Audio Multiprocessor



- 8 Media Processing Engines (MPEs)
- L1$ (I$ 16KB / D$ 8KB)
- L2$ controller
- L2$ SRAM 256KB
- Others : Assistant logic for specific video codec

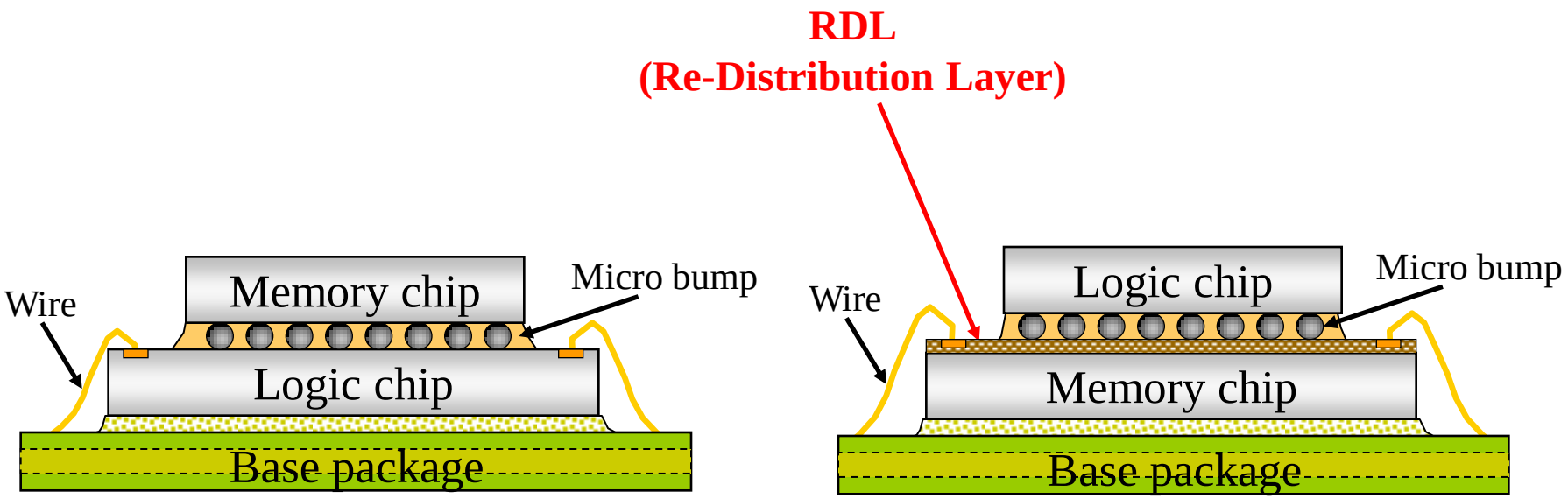
Micrograph



- **Technology**
  - 40 nm CMOS, triple-well,7-layer-metal
- **Chip size**
  - 6.0 mm x 6.2 mm
- **Gate counts**
  - 18.5 M gates (Logic), 9 M bit (SRAM)
- **Clock frequency**
  - 435 MHz(ARM), 400 MHz(HS I/O), 333 MHz(Video/Audio), 255MHz(H.264 dec.), 166 MHz(Main bus, HS peripheral), 83 MHz(Sub bus, LS peripheral)
- **CPU**
  - ARM Cortex™-A9 MPCore™ (I$:16 KB, D$:16 KB) x2
  - Video/Audio MPE x8
  - H.264 Full-HD Video CPU x2
  - TS CPU x1
  - General CPU x1
- **External memory I/F**
  - DRAM 128 bits x 4 ch. 166 MHz (SCS)
  - Mobile-DDR SDRAM 32 bit 166 MHz (SIP)

Stacked DRAM Architecture

SCS Technology



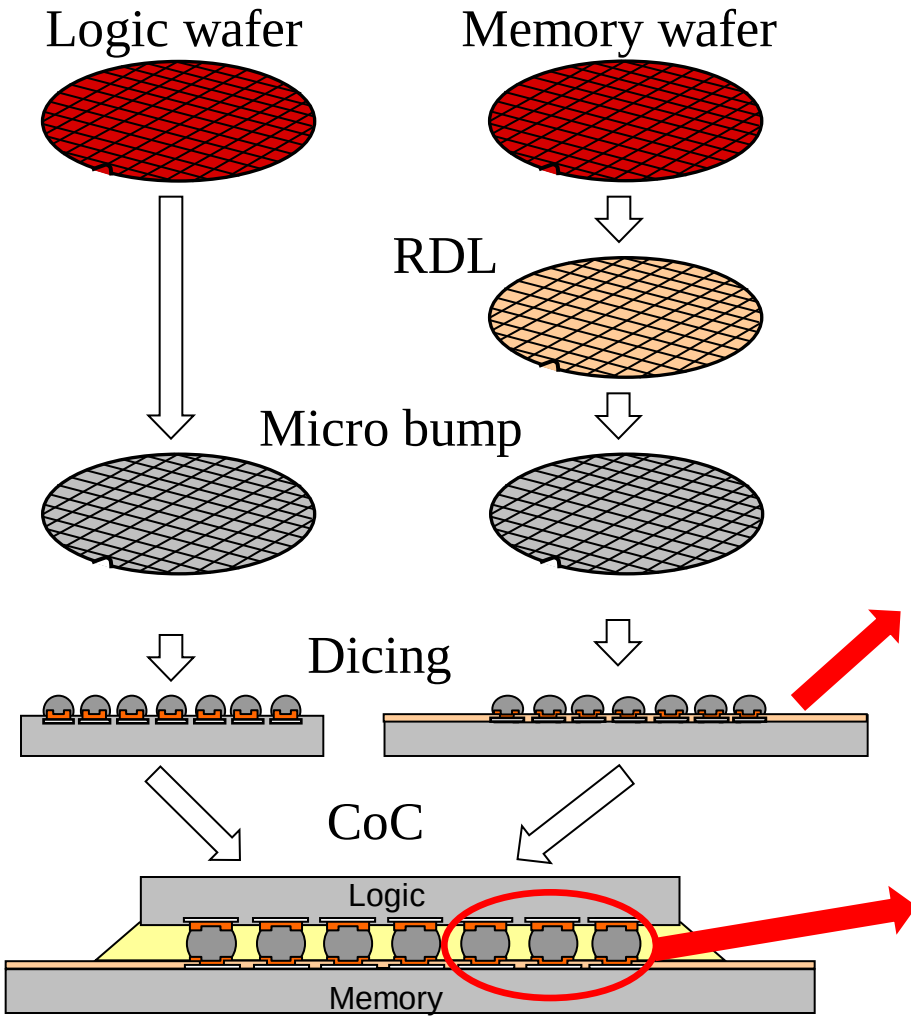
Type 1

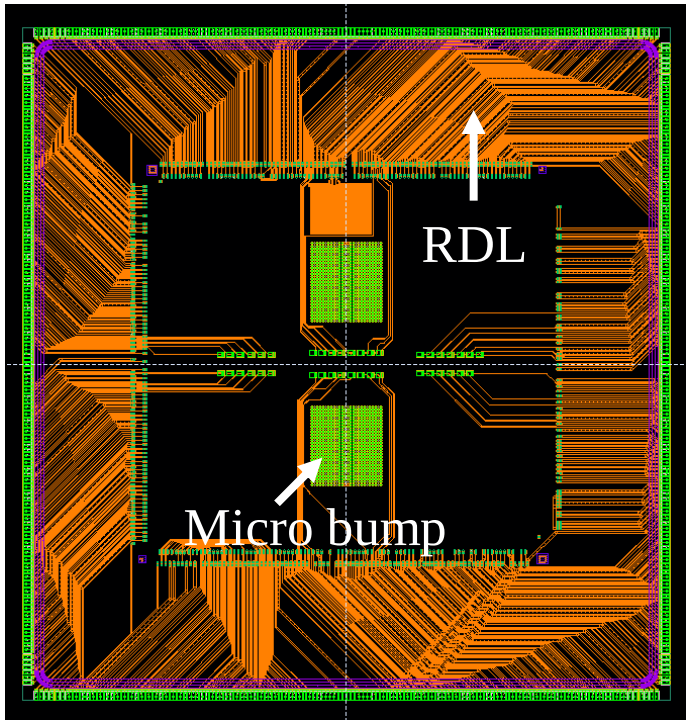
Type 2

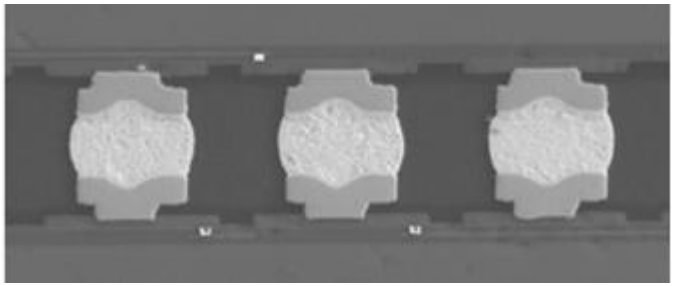
Logic Chip > Memory Chip

Logic Chip < Memory Chip

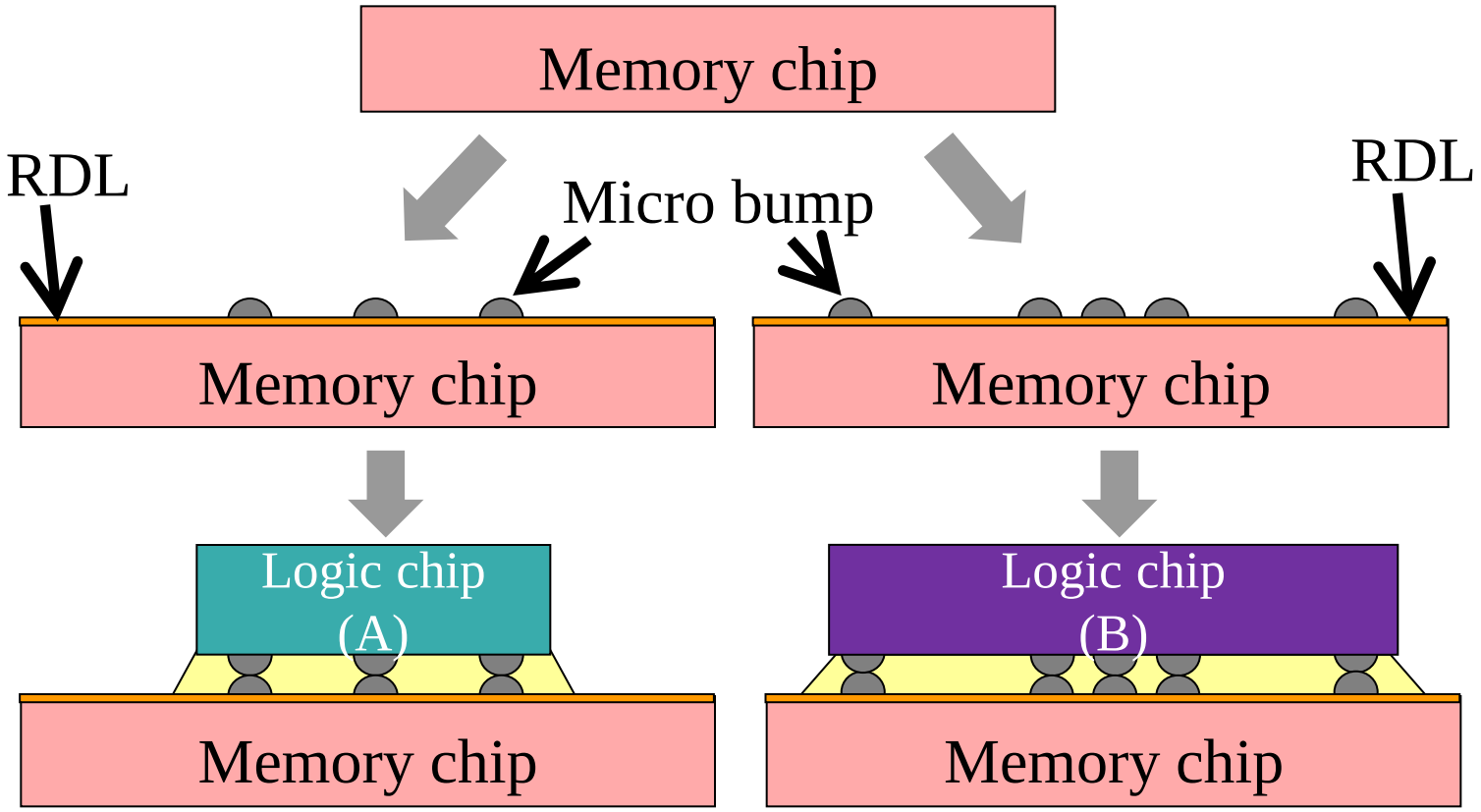
Stacked DRAM Flow





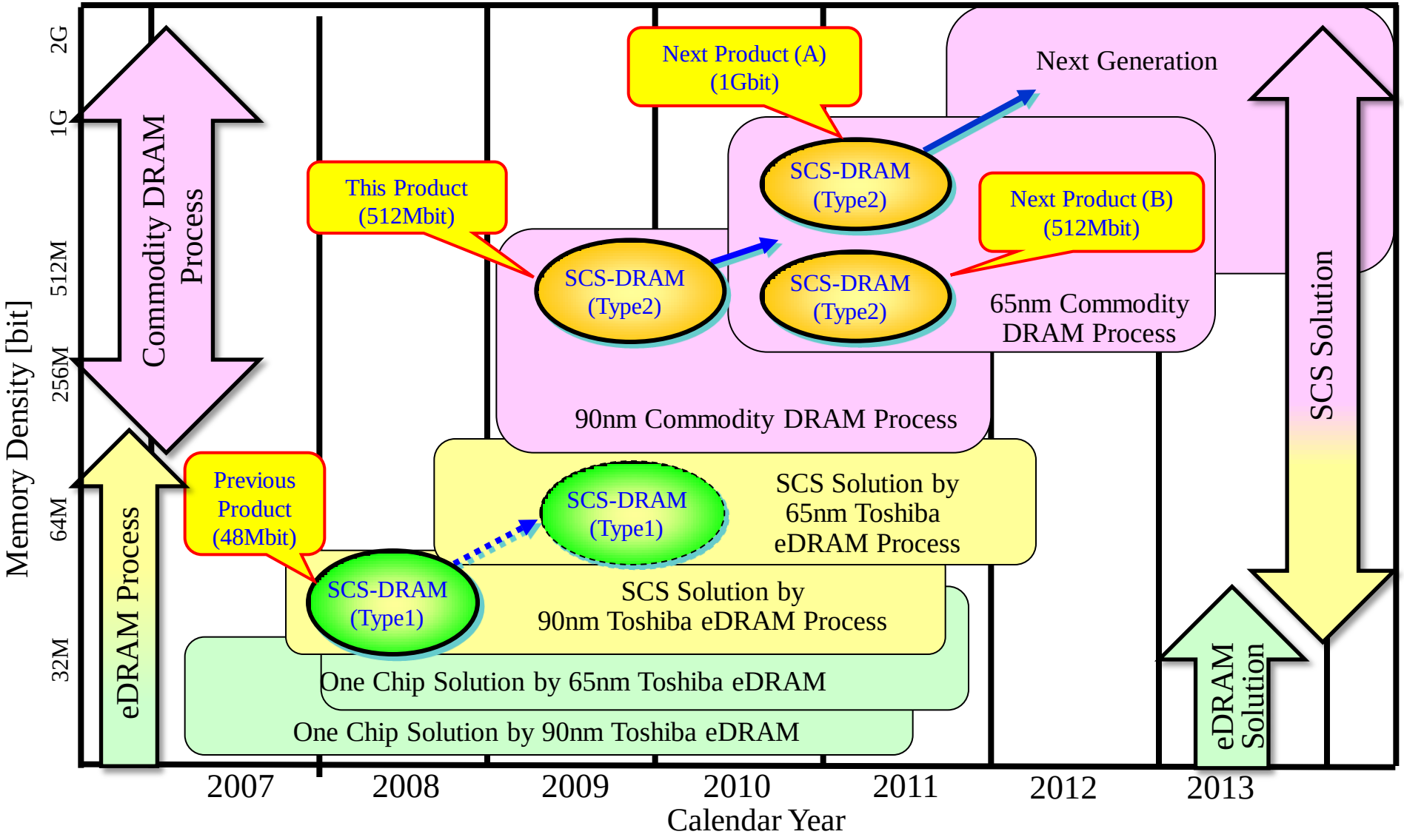


Using the same memory chip with different logic chip



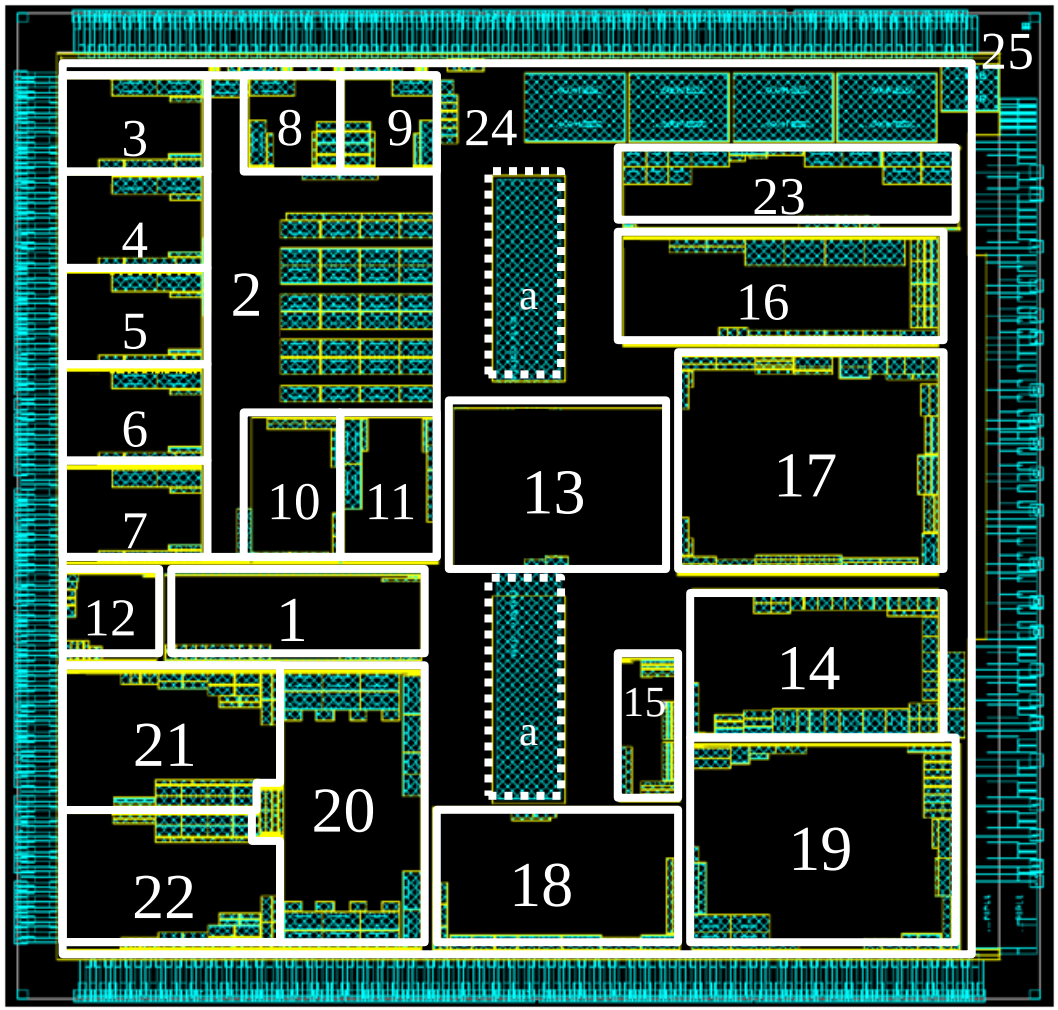
Various products used same memory chip

SCS Roadmap



Multiple Power Domain Control

Chip Power Domain

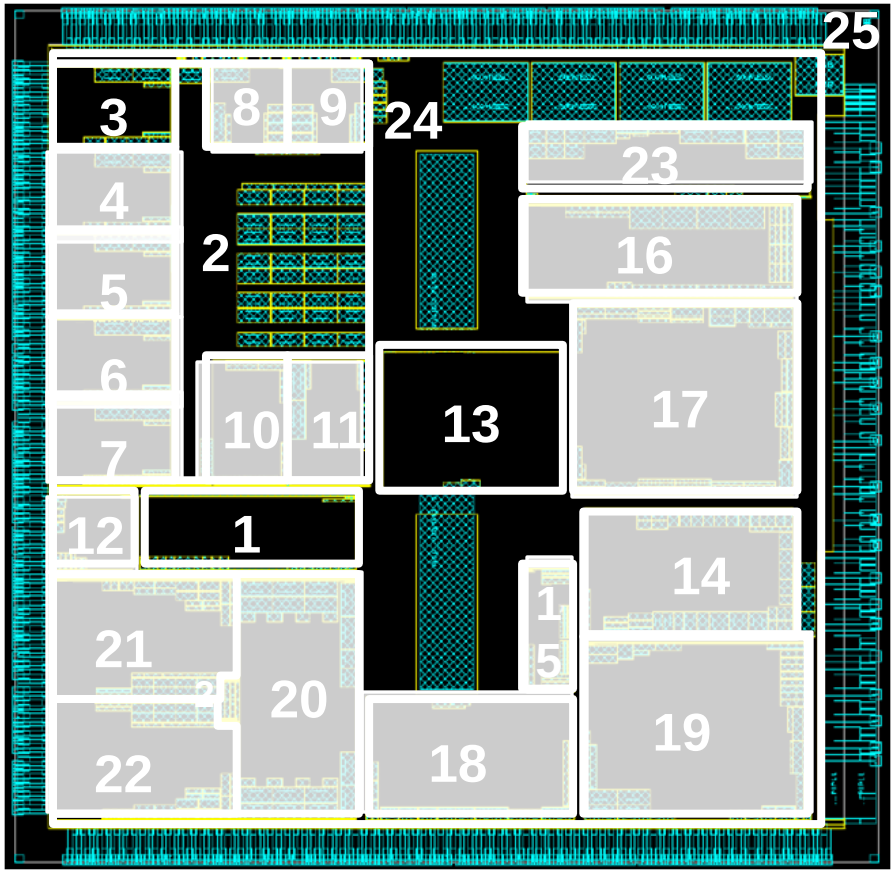


(2)-(11) Video/Audio multiprocessor
(17) Full-HD video H.264 Codec engine
(19) 3D/2D graphics engine
(20)-(22) ARM processor
(15) Camera I/F
(14) Display I/F
(16) Image composition
(12) JPEG/Video scaling
(1)(13)(18)(23) Main bus
(24) Control bus / Peripheral I/F
(25) I/O

(a) SCS-DRAM I/F

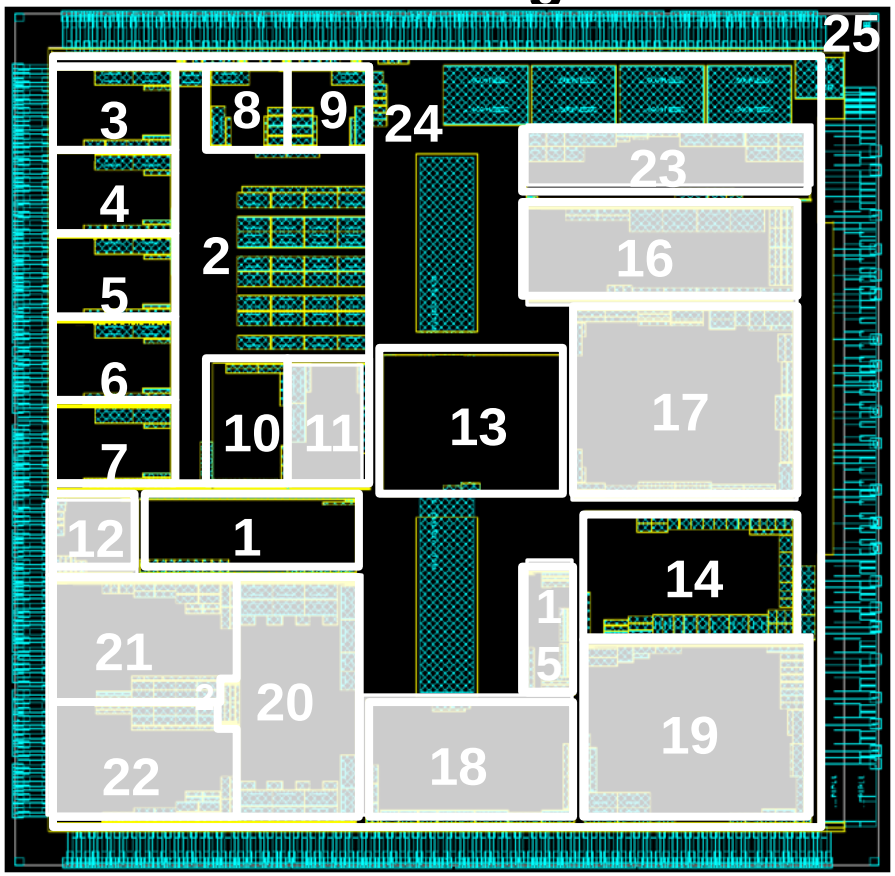
Chip power domain by Use Case

Audio playback



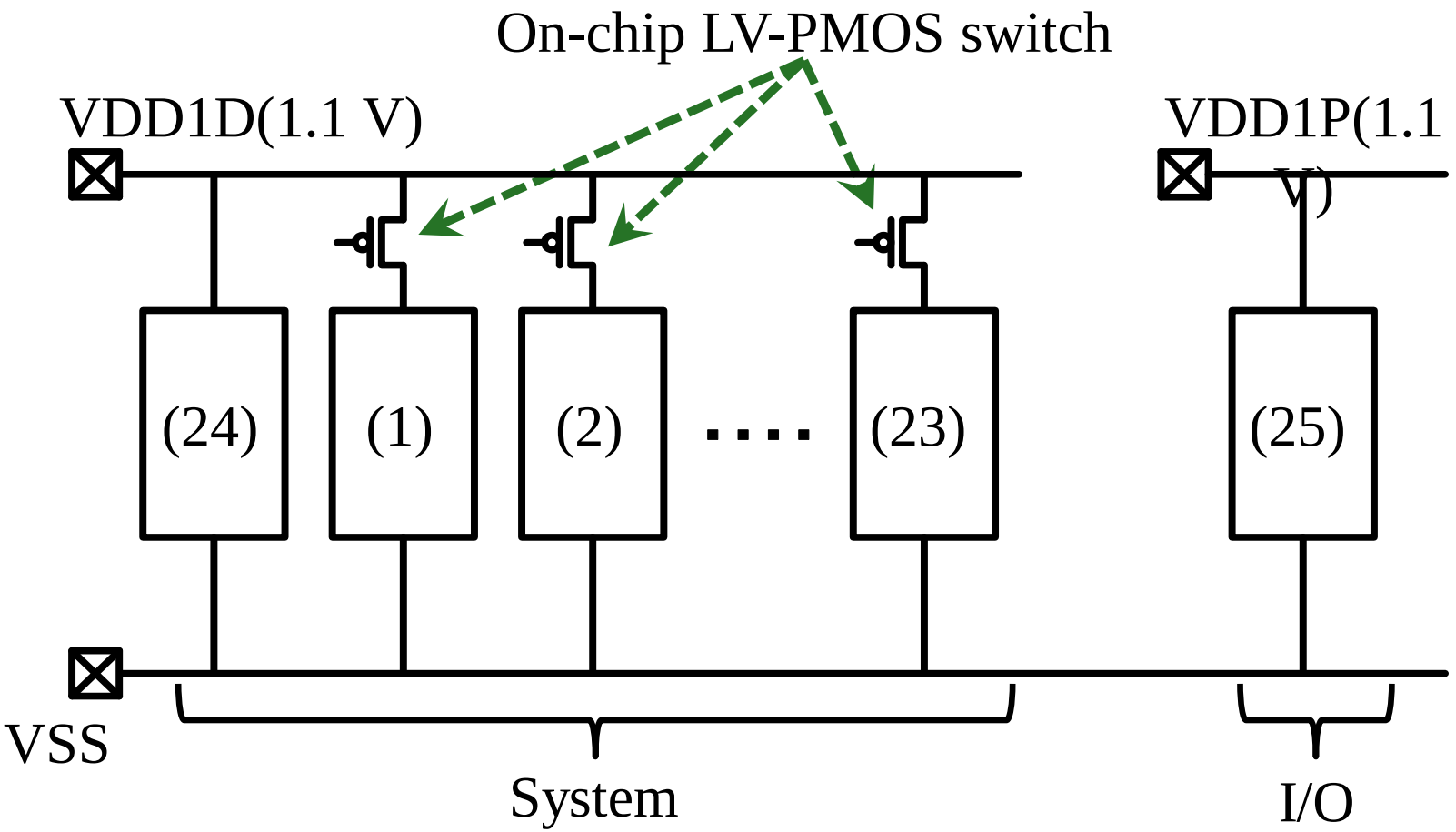
L2$ SRAM & controller (2)
+ 1MPE (3)

Audio playback
+ Video decoding + LCD out



L2$ SRAM & controller(2)
+ 8MPEs (3)-(10)

Power Supply System Chart

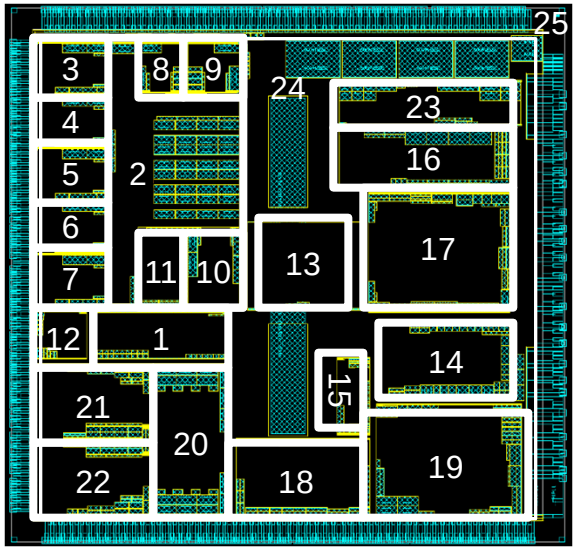


23 power domains are controlled by on-chip switches

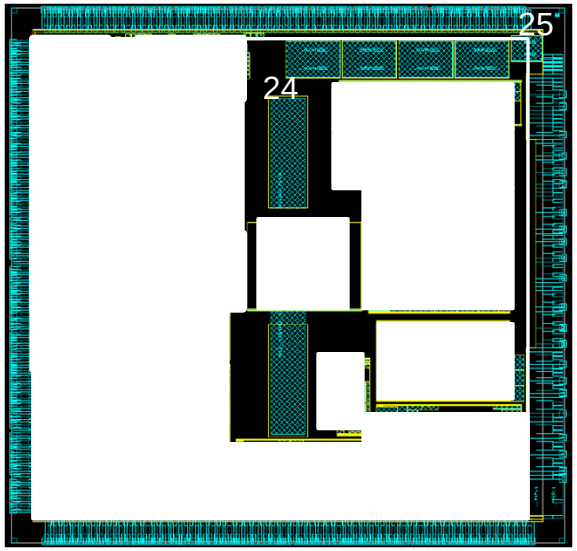
Chip Power Consumption

Leakage Current

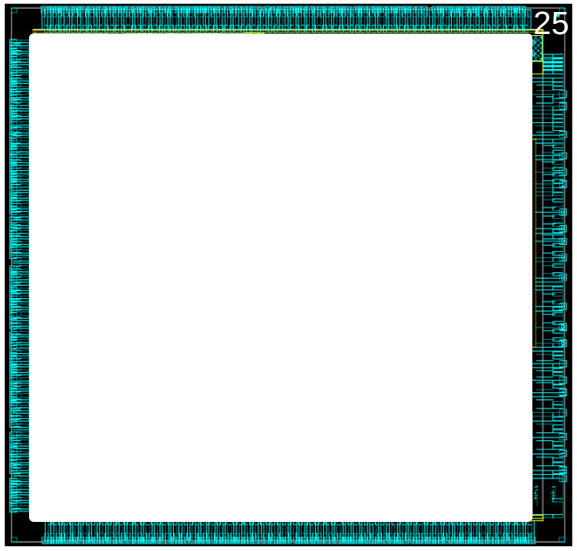
All On Mode



Sleep Mode



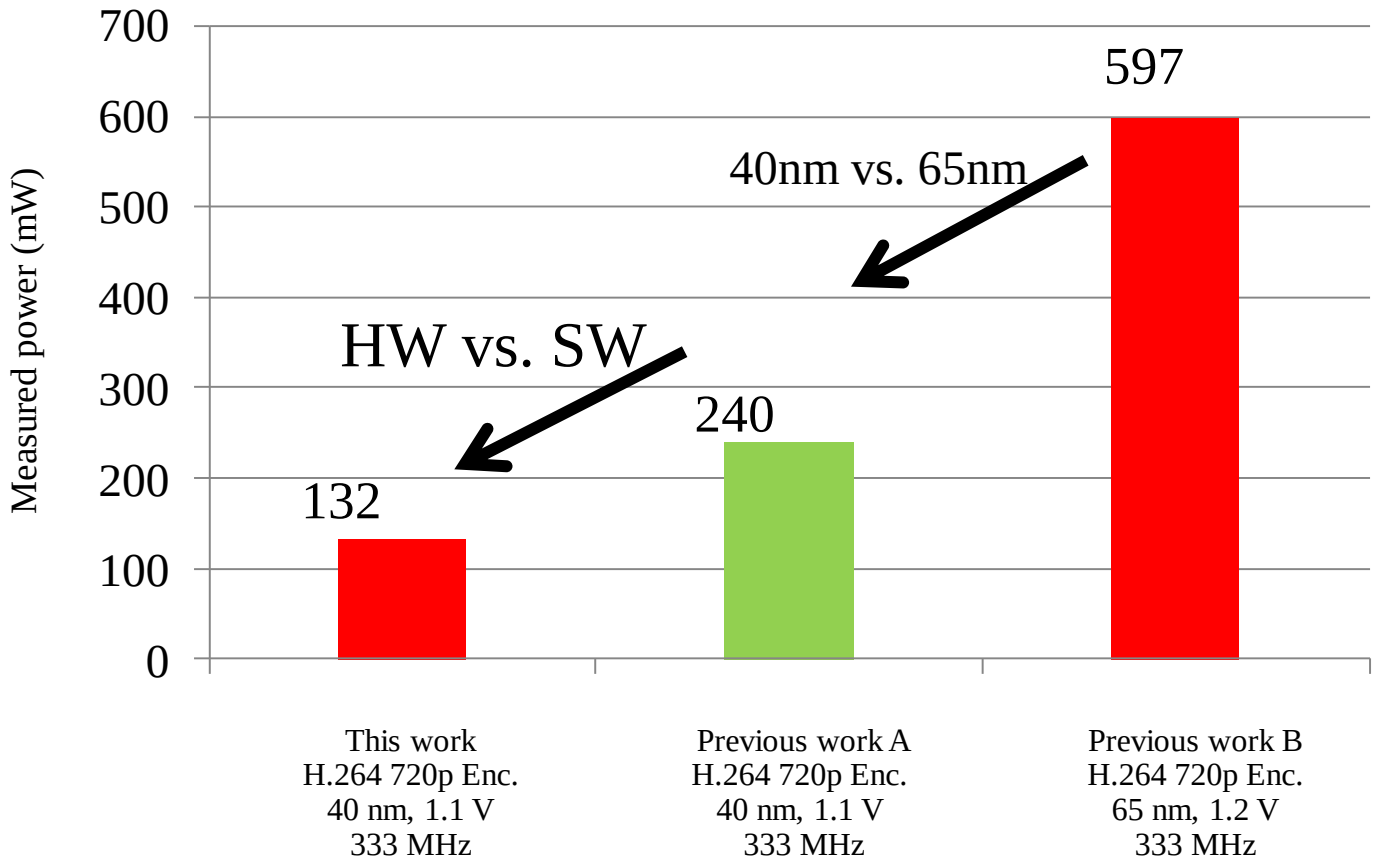
Standby Mode



Power Mode	Turn On Domain	Power
Standby Mode	25	15μW
Sleep Mode	24,25	1.7mW
All On Mode	1,2,3,4,5,6,7,8,・・・・,24,25	22mW

Vdd = 1.1 V, Process = center, Temp. = 25 deg.C.

Comparison with previous work



The HW engine achieves low power compare with SW

Hardware Based Solution

Application	Scenario	Resolution	Frame Rate	Power
H.264	High Profile Decoding	1920x1080	30 fps	222 mW
		640x480	15 fps	71 mW
	High Profile Encoding	1920x1080	10 fps	232 mW
		1280x720	30 fps	132 mW
3D	OpenGL® ES2.0	40 M polygon/s		124 mW

Vdd = 1.1 V, Process = center, Temp. = 25deg.C.

The HW engine achieves high performance with low power consumption

Software Based Solution

Application	Scenario	Audio Option	Resolution	Frame Rate	Number of Active MPE	Power
MPEG-4	Simple Profile Dec.	None	640x480	15 fps	7 MPEs	79 mW
		AAC Dec. 48 kHz 256 kbps stereo x 2	854x480x2	30 fps	8 MPEs	237 mW
	Main Profile at High Level Dec.	None	960x1080	30 fps	8 MPEs	249 mW
	Simple Profile Enc.	None	320x240	15 fps	7 MPEs	72 mW
H.264	Baseline Profile Dec.	None	320x240	15 fps	3 MPEs	37 mW
		AAC Dec. 48 kHz 128 kbps stereo	320x240	15 fps	3 MPEs	42 mW
	High Profile Dec.	None	640x480	15 fps	2 MPEs	70 mW
	Baseline Profile Enc.	AAC Enc. 48 kHz 64 kbps stereo	320x240	15 fps	7 MPEs	79 mW
		None	854x480	30 fps	8 MPEs	315 mW

Vdd = 1.1 V, Process = center, Temp. = 25deg.C.

The multiprocessor achieves the same degree of low power as the HW engine using 2 MPEs by multiple power domain control at H.264 VGA 15fps decoding.

Summary

Summary

- **Hybrid application processor**
  - HW Solution
    - H.264 Full-HD 30fps decoding : **222mW**
    - 3D / 2D graphics : **40M polygons/s, 300M pixels/s**
  - SW solution
    - H.264 VGA 15fps decoding : **71mW**
- **SCS technology**
  - Peak memory bandwidth : **10.6GB/s**
  - Four 128-bit channels at 2.4GB/s : **3.9mW**
- **Multiple power domain control**
  - Power domains : **controllable 23 of 25 power domains**
  - Total leakage power : **1.7mW (sleep mode)**

The chip achieves low power at high performance for Mobile Market.