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ASP-DAC 2011 Designer's Forum
Session 8D-3: State-of-The-Art SoCs and Design Methodologies

Design Constraint for Fine Grain Supply Voltage Control LSI

January 28, 2011

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Agenda

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- Background
  - Fine grain supply voltage control
- Energy gain concept
- Power gating case
  - Various energy losses
  - Results with simple assumption
  - Modification for actual devices
  - Comparison with simulation results
  - Minimum sleep duration time
- DVFS* case (results only)
- Summary

*DVFS: Dynamic Voltage and Frequency Scaling

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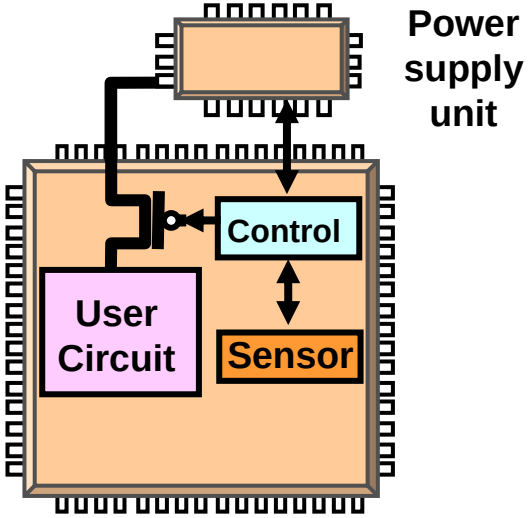
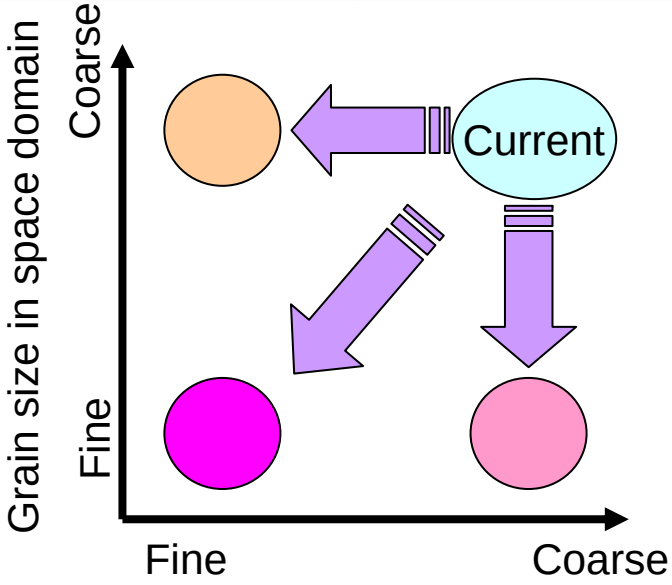
General expectation for fine grain supply control



Supply voltage control LSI



Grain size in time domain

- Concept of supply voltage control:
  - Collaboration between power supply unit and user circuit optimizes energy consumption
  - Power gating and DVFS are typical controls.
- Two types of grain size
  - Grain size in time domain
  - Grain size in space domain
- General expectation
  - Fine grain control will improve power efficiency.

We will discuss the time domain control in this paper.

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Fine grain supply control in time domain

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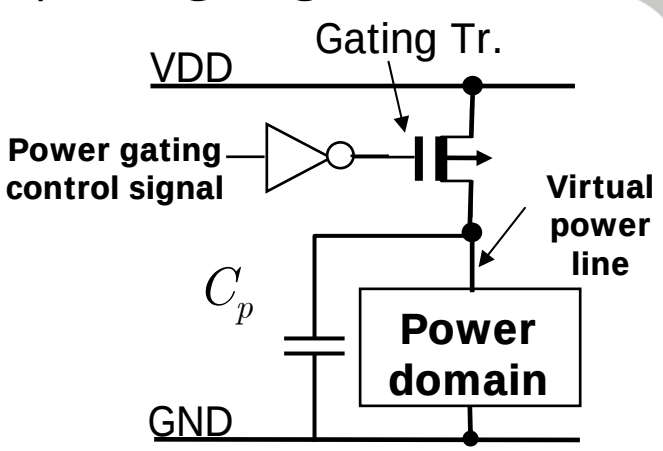
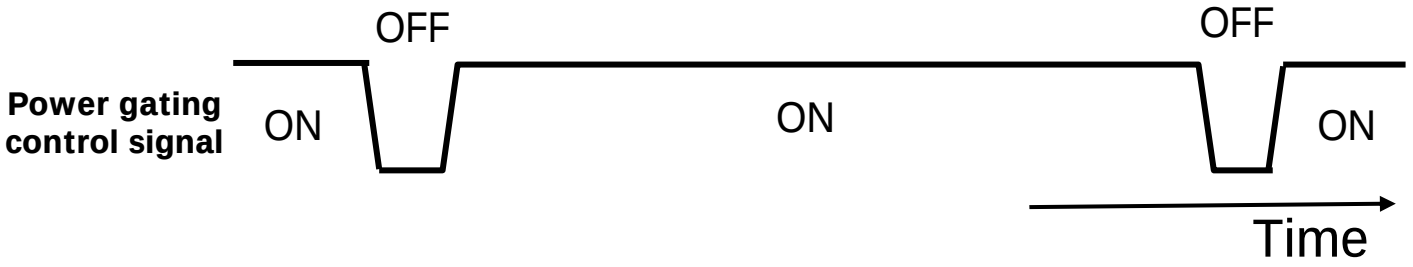
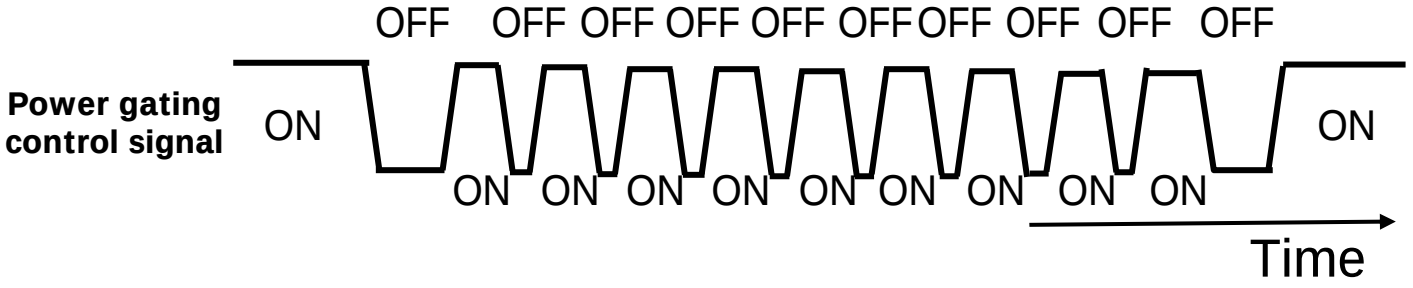
(power gating case)



More frequent controls are expected to reduce leakage power.



Coarse grain



Fine grain

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Energy gain concept to derive design constraint

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E_a

Dissipated energy when supply voltage control technique is applied.

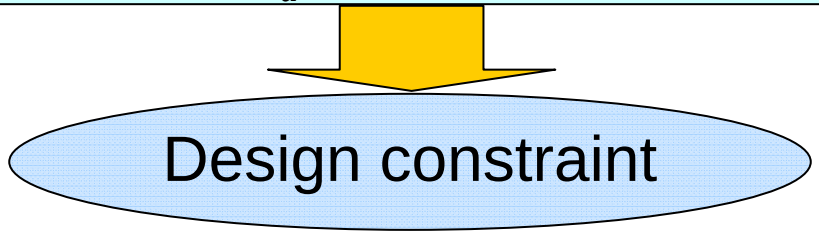
- Energy for circuit operation itself
- Energy overhead for changing supply voltage

E_{na}

Dissipated energy when supply voltage control technique is not applied.

- Energy for circuit operation itself

Energy gain : $n = \frac{E_{na}}{E_a} > 1$ necessary condition



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Power gating case

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Energy losses at power gating

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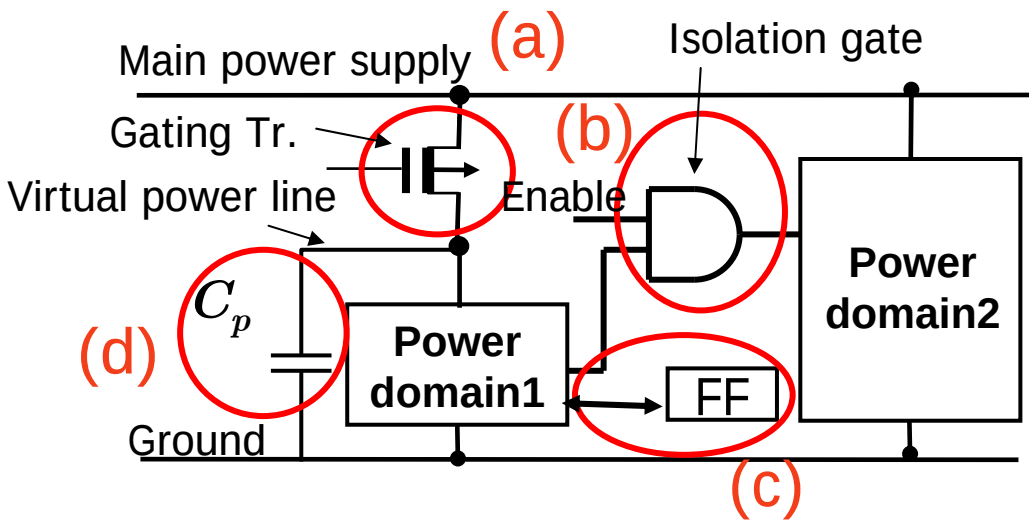
(a) Switching energy of gating transistor

(b) Switching energy of isolation gates

(c) Storing/restoring energy for internal information

(d) Charging/discharging energy of virtual power line



Only (d) is dependent of sleep duration time

(a)-(c) is independent of sleep duration time.

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Start with simple assumptions

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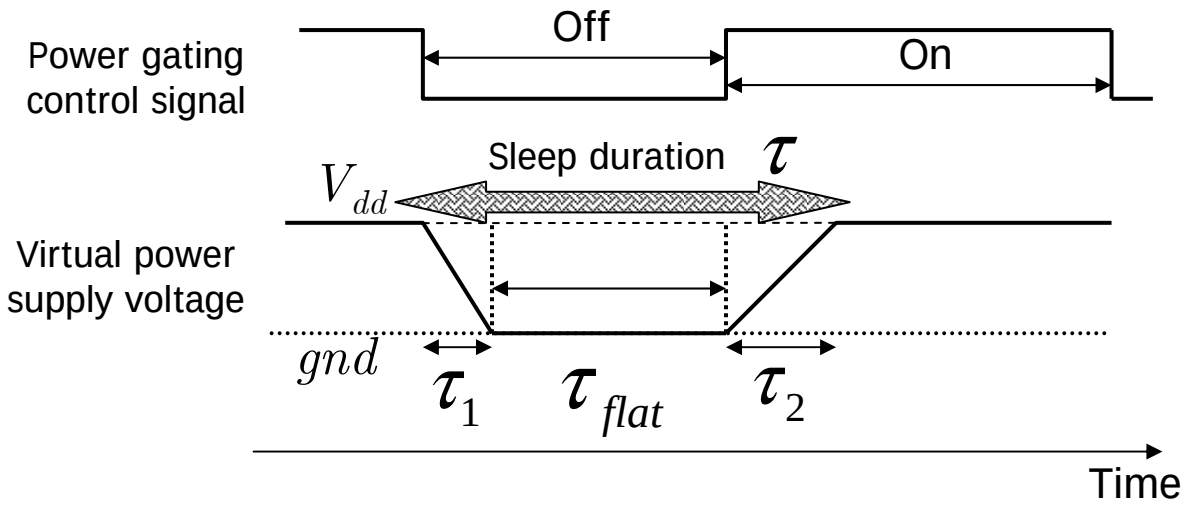
Start with the following simple assumptions.

1. Leakage current is independent on drain voltage.
2. Consider charging energy of virtual power line only.

   (Other energy losses (a)-(c) are ignored.)

Then we modify the theory excluding these assumptions



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Energy losses for charging virtual power line

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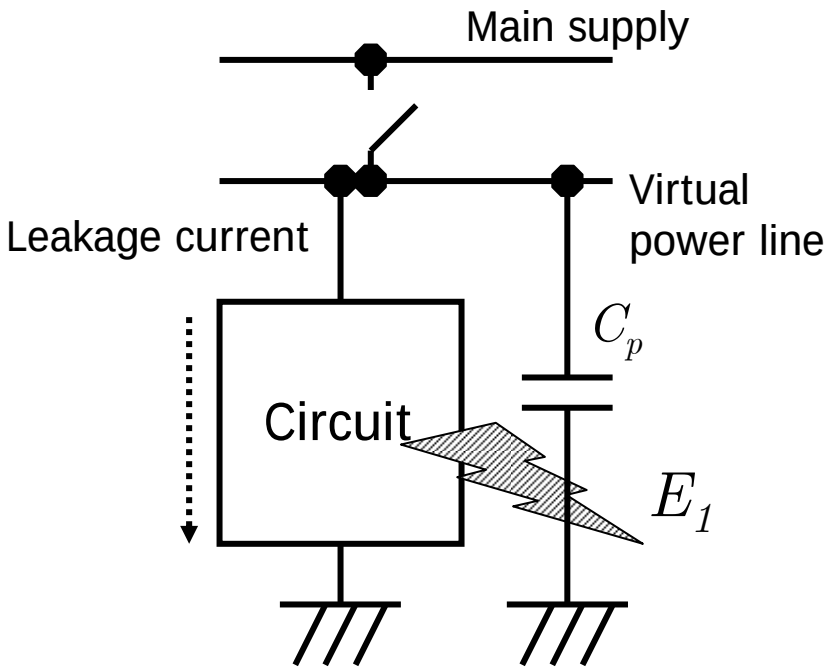
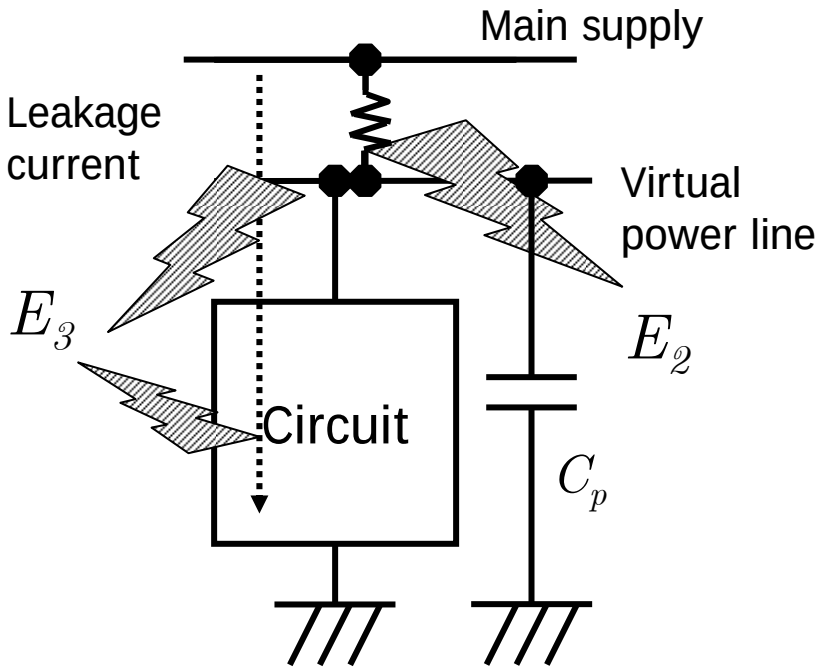
Energy with power gating : $E_a = E_1 + E_2 + E_3$

Energy without power gating : $E_{na} = I_{off} V_{dd} \tau = I_{off} V_{dd} (\tau_1 + \tau_2 + \tau_{flat})$



(a) Discharging phase



(b) Charging phase

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Minimum sleep duration time

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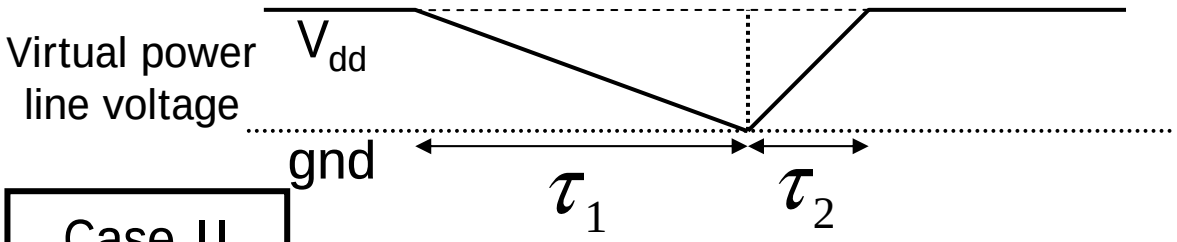
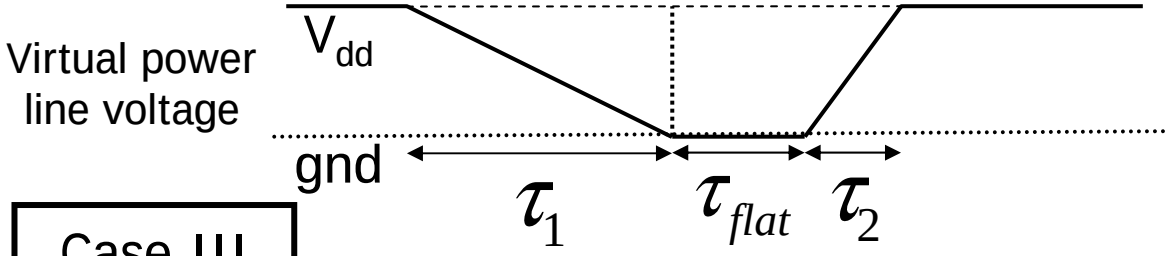
Case I



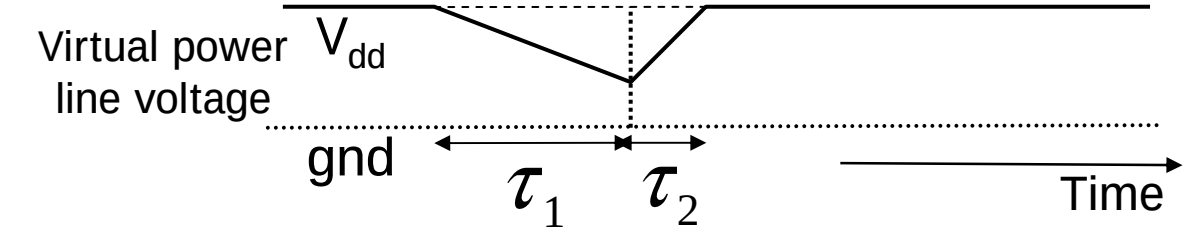
$$E_{na} = E_a$$

Case II



$$E_{na} > E_a$$

Case III



$$E_{na} < E_a$$

(if other energy losses exist)

Minimum sleep duration time: $$\tau_{\min}^{0} = \frac{C_p V_{dd}}{I_{off\ @\ V_{dd}}}$$

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Leakage current dependence on drain voltage

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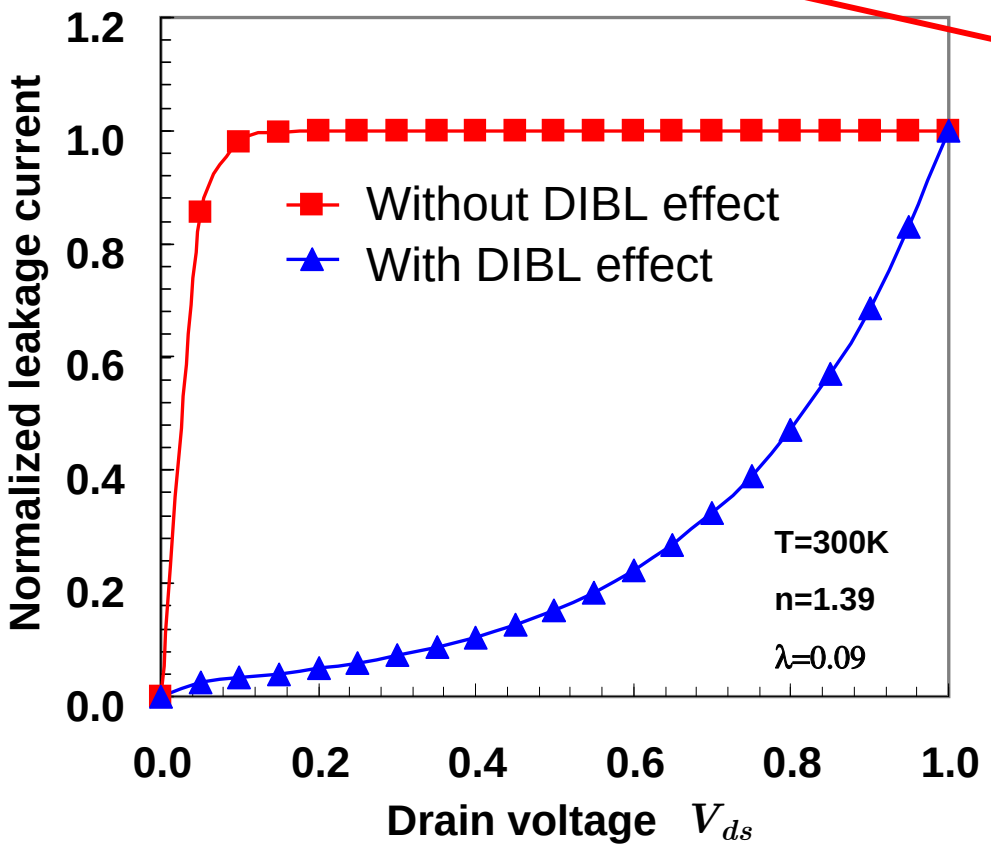
- Actual transistors have DIBL* effects and leakage current does depend on drain voltage.

$$I_{off}(V_{ds}) = Ae^{\frac{V_{gs}}{nv_i}} e^{\frac{\lambda V_{ds}}{nv_i}} (1 - e^{-\frac{V_{ds}}{v_i}}), \qquad v_i = \frac{kT}{q}$$

DIBL effect term



We assume

$$I_{off}(V_{ds}) \propto V_{ds}^{\beta}$$

$$\beta = 1 \sim 2$$

DIBL: Drain Induced Barrier Lowering

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E_{ov} : Other energy loss

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- Other energy loss E_{ov} is independent of sleep duration time.
- (a) & (c) are proportional to decoupling capacitor C_p
  - Total load capacitance of power domain C_L is proportional to C_p due to power line noise constraint.
  - Capacitance of gating Tr. C_x is proportional to C_L due to IR drop voltage limitation.
  - Capacitance of storage elements is proportional to total load capacitance C_L.
- (b) is small enough to be ignored for usual cases.

$$\frac{C_L}{C_p} \propto \frac{v_{noise}}{\alpha}$$

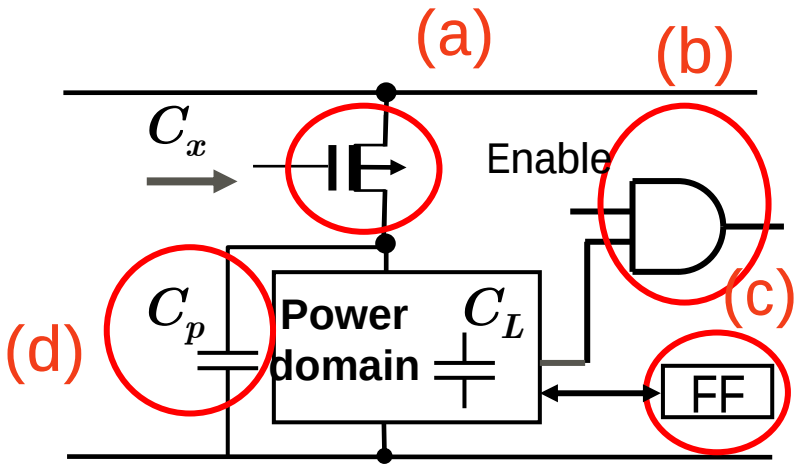
$$\frac{C_x}{C_p} \propto \frac{f_{op}(Circuit)}{f_T(GatingTransistor)}$$

We can assume other energy loss E_{ov} is proportional to C_p.

$$E_{ov} = z * C_p V_{dd}^2$$

$$z = 20\% \quad typical$$

z : Energy overhead factor



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Energy gain diagram for power gating

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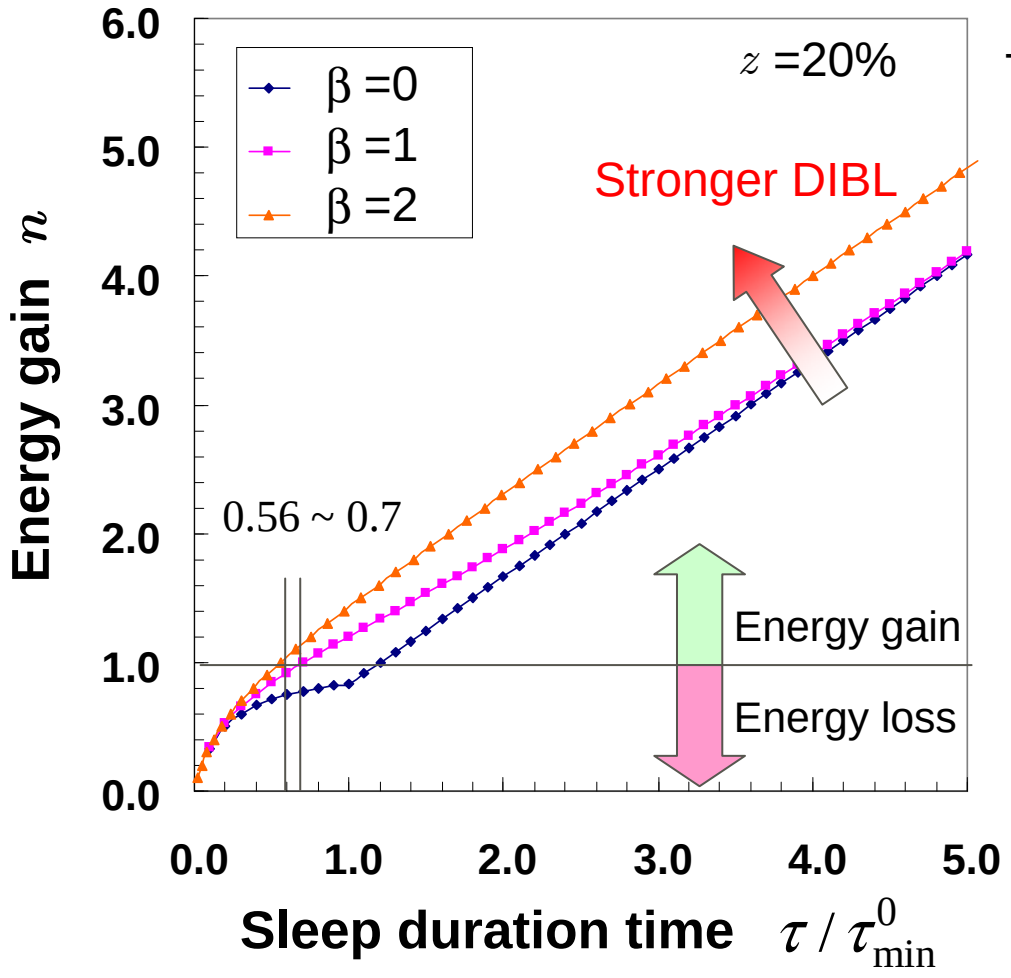
Including other energy loss and non-constant leakage current effect

Energy with power gating : $E_a = E_1 + E_2 + E_3 + E_{ov}$

Energy without power gating : $E_{na} = I_{off} V_{dd} \tau = I_{off} V_{dd} (\tau_1 + \tau_2 + \tau_{flat})$



The modified theory predicts:

- Longer sleep time gives higher energy gain.

$$When \quad \tau \to \infty, \qquad n \to \infty$$

- Stronger DIBL effect gives higher gain and shorter minimum sleep duration time.

$$\tau_{\min} = F_{leak} \tau^0_{\min}$$

When β is larger, F_{leak} is smaller.

$$F_{leak} = 0.56 \sim 0.7 \quad (1 < \beta < 2)$$

(Correction factor)

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Comparison with simulation results

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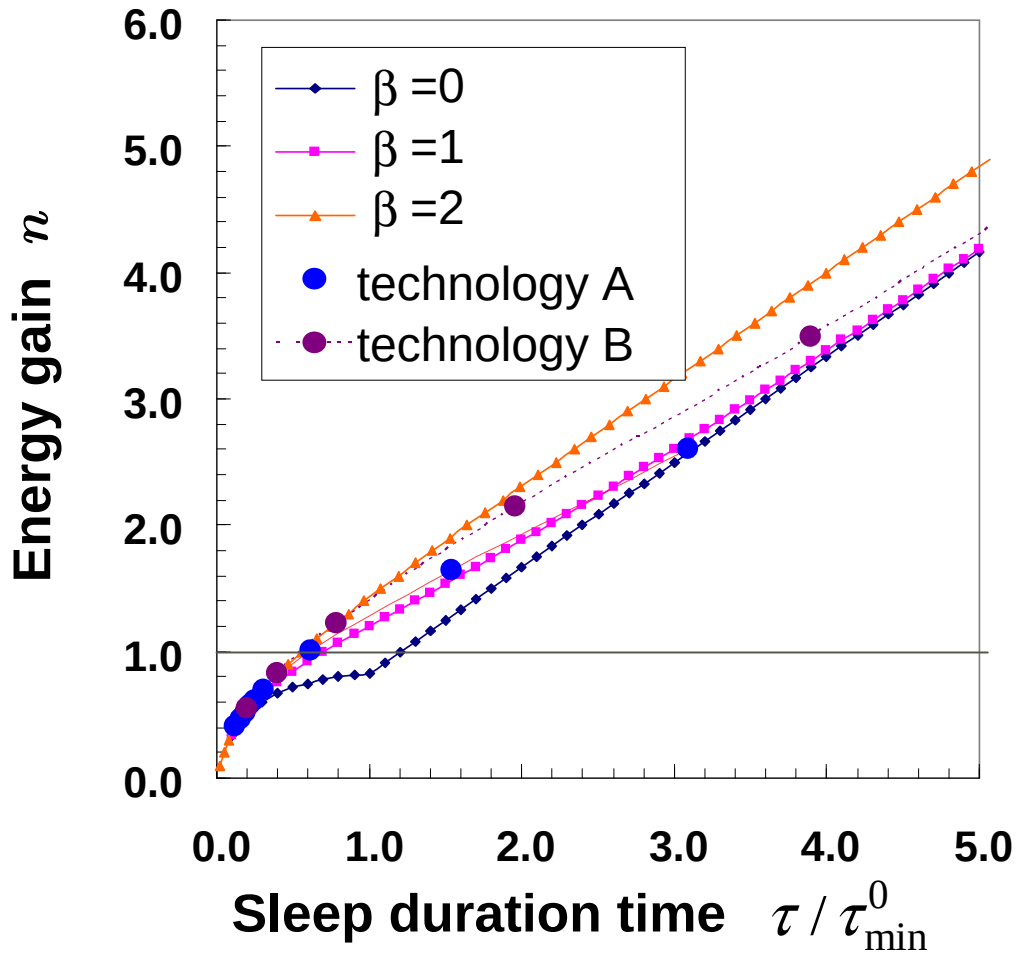
Target circuit : 1.1K gates



z =20%

Technology A

- I_{on}/I_{off}= 1.2x10^3
- τ_{min}^0= 3.24μs
- β~1(weak DIBL)

Technology B

- I_{on}/I_{off}=1.0x10^3
- τ_{min}^0= 0.26μs
- 1<β<2(strong DIBL)

$$\tau_{\min} = F_{leak}\tau^0_{\min}$$

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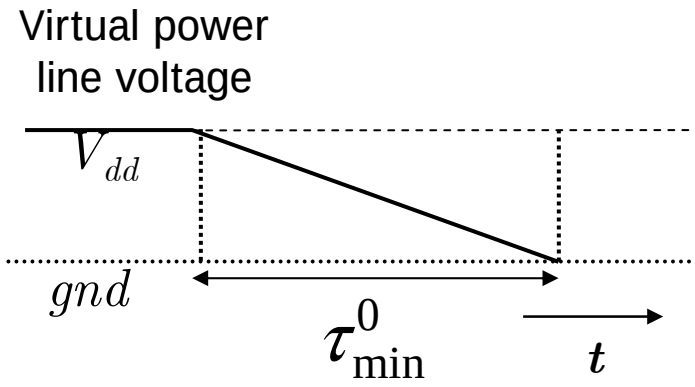
Which design parameters determines $\tau^0_{\min}$? FUJITSU

Minimum duration

$$\tau^0_{\min} = \frac{C_p V_{dd}}{I_{off}(V_{dd})}$$



- Discharging time from V_{dd} to gnd.
- It does not depend on power domain size.

$$\tau^0_{\min} \approx \left(\frac{C_p}{C_L}\right)_{gate} * \left(\frac{I_{on}}{I_{off}}\right)_{Tr.} * \tau_g$$

Design dependent

Technology dependent

τ_g : Average gate delay

C_p : Virtual power line cap.

C_L : Average load cap.

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Evaluation of $\tau_{\min}^{0}$ value

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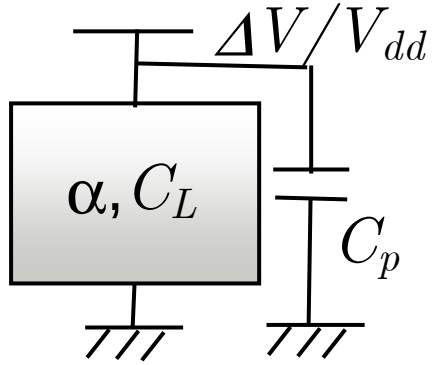
$$\left(\frac{C_p}{C_L}\right)_{gate} \approx 5$$

Restriction of supply voltage fluctuation

Ex. Activity factor α=25%, $\Delta V/V_{dd}$ = 5%



$$\left(\frac{I_{on}}{I_{off}}\right)_{Tr.} \approx 1\text{x}10^{7} - 3\text{x}10^{7} \rightarrow 1\text{x}10^{5} - 3\text{x}10^{5}$$

*Low standby power technology 2010-2020

Assume process/temperature coefficient to be 100

$$\tau_g \approx 8\,ps - 40\,ps$$

*Low standby power technology 2010-2020

$$\therefore \tau_{\min}^{0} \approx 5\mu s - 60\mu s$$

Relatively long time constant compared with clock cycle time

* From ITRS roadmap 2009

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Minimum sleep cycle number

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$$\tau_{\min}^{0} \approx \frac{1}{Ng}\left(\frac{C_p}{C_L}\right)_{gate} * \left(\frac{Ion}{Ioff}\right)_{Tr.} * T_{cycle}$$

N_g : Gate number per one pipeline stage

When

$N_g = 18$ $FO4$ (Power performance optimized design*)

$$\tau_{\min}^{0} \approx (3 \sim 8) \times 10^4 T_{cycle}$$

*V. Zyuban et. al., “Integrated Analysis of Power and Performance for Pipelined Microprocessors,” *IEEE Trans. On Computer*, pp.1004-1016, Vol.53, No.6, Aug. 2004.

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DVFS case (results only)

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Minimum DVFS cycles

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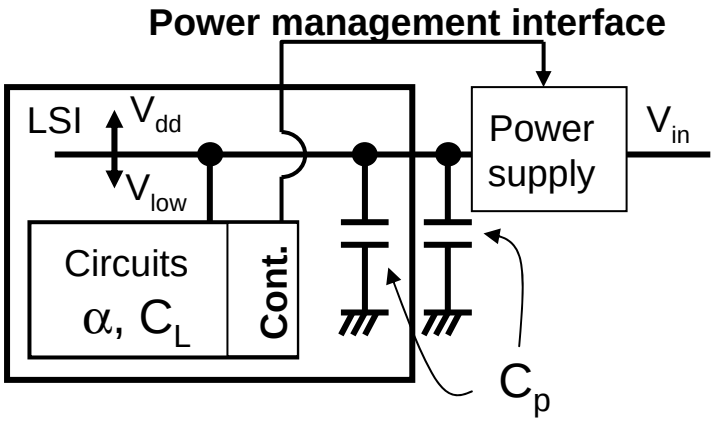
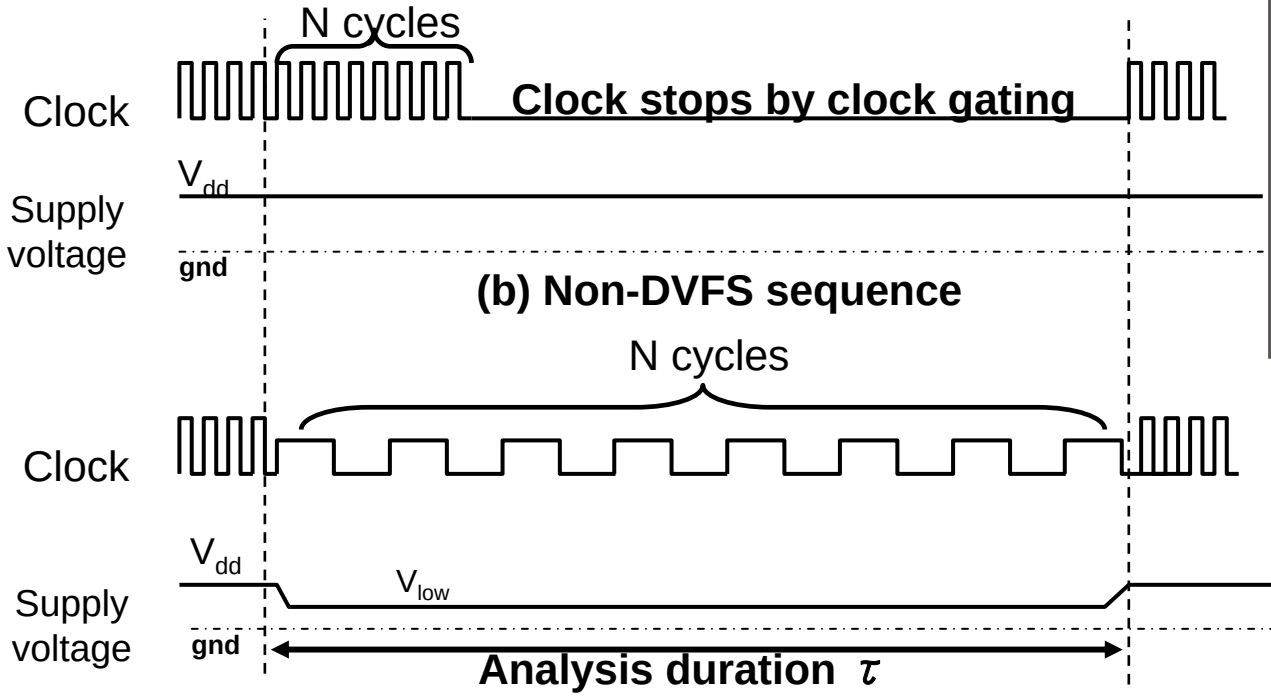


(a) DVFS scheme

Minimum DVFS cycles exist.

$$N > N_{\min}^{0} = \frac{C_p}{\alpha C_L}$$



(b) Non-DVFS sequence

(c) DVFS sequence

α :	Activity factor
C_L :	Total load capacitance
C_p :	Total power line capacitance

Simple assumption:

Leakage current is ignored and efficiency of power supply unit is ideal.

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Power configuration

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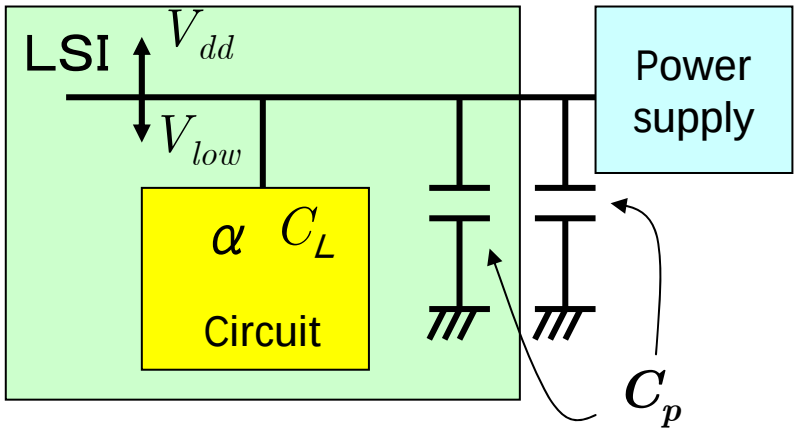
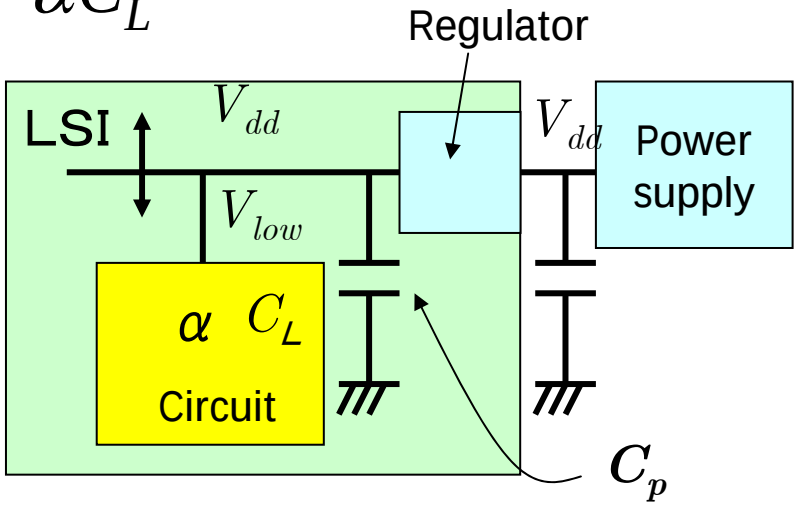
$$N > N_{\min}^{0} = \frac{C_p}{\alpha C_L}$$



(a) External power supply



(b) On-chip regulator and external power supply

- Larger C_p, Larger $N_{min}{}^{0}$
- Higher efficiency of power supply

- Smaller C_p, Smaller $N_{min}{}^{0}$
- Lower efficiency of power supply

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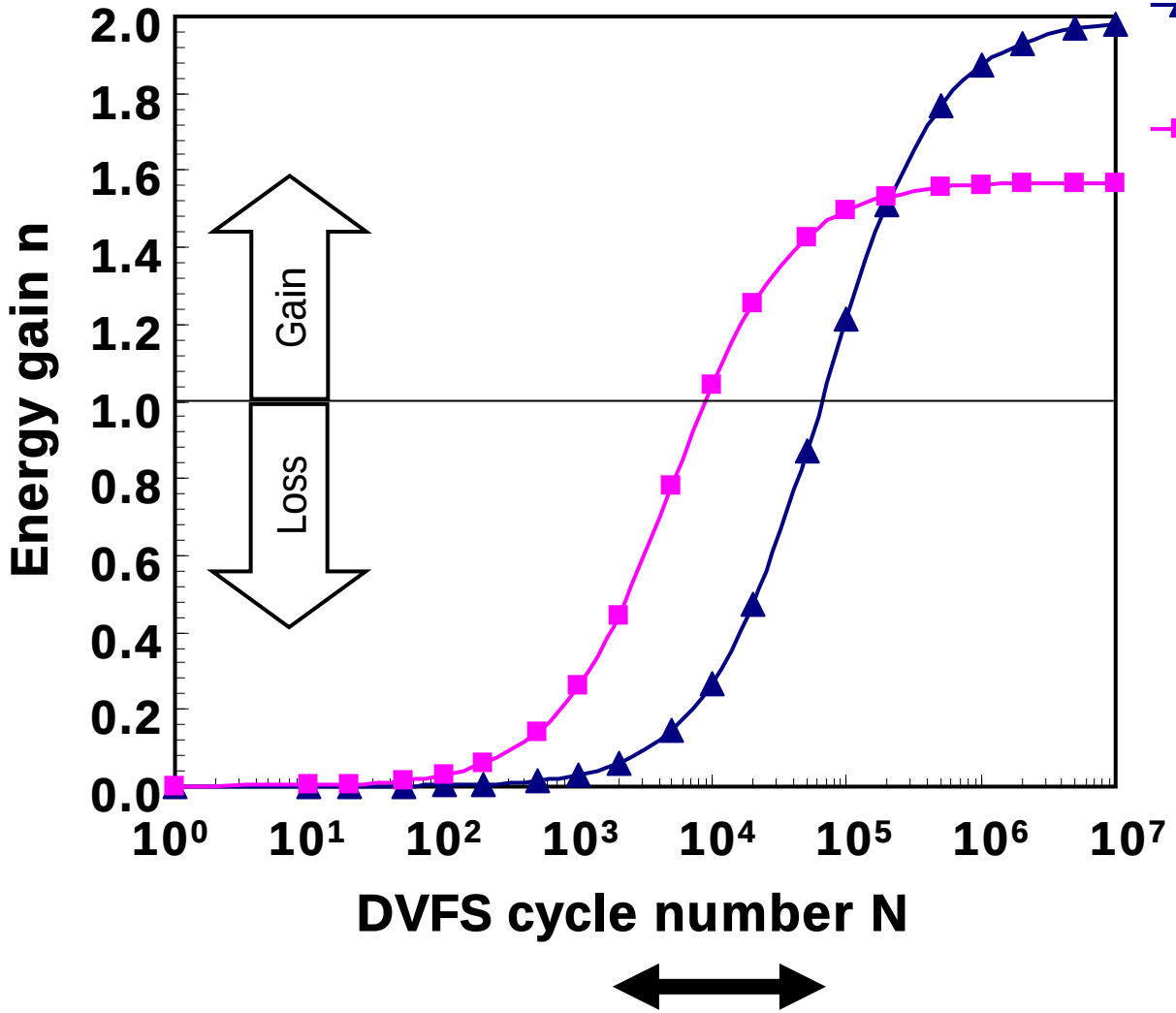
Energy gain diagram for DVFS



External power supply

$C_p / C_L = 5000$

External power supply +regulator

$C_p / C_L = 500$

$x = \frac{V_{low}}{V_{dd}} = 0.7$

$k = 0.3$

$\eta_d = 0.9$

$\eta_l = 0.8$

$\beta = 2$

$10^3 - 10^5$ Cycles are required to obtain energy gain larger than unity.

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Summary

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	Power gating	DVFS
Minimum sleep duration **Minimum cycle number**	$\tau_{\min}^{0} = \frac{C_p V_{dd}}{I_{off}}$	$N_{\min}^{0} = \frac{C_p}{\alpha C_L}$
Correction factor	$F_{leak} = 0.56 \sim 0.70$	$F_{leak} = 0.56 \sim 0.86$ $F_{\text{supply}} = 1 \sim \infty$
Maximum energy gain	$n \to \infty$, when $\tau \to \infty$	$n \to \frac{x+k}{x(1+k)} \frac{1}{x^2}$, when $N \to \infty$
Important design parameters	$\frac{I_{on}}{I_{off}}, \tau_g$	**1. Power supply configuration** C_p **2. Efficiency** $\eta_{d,l}$

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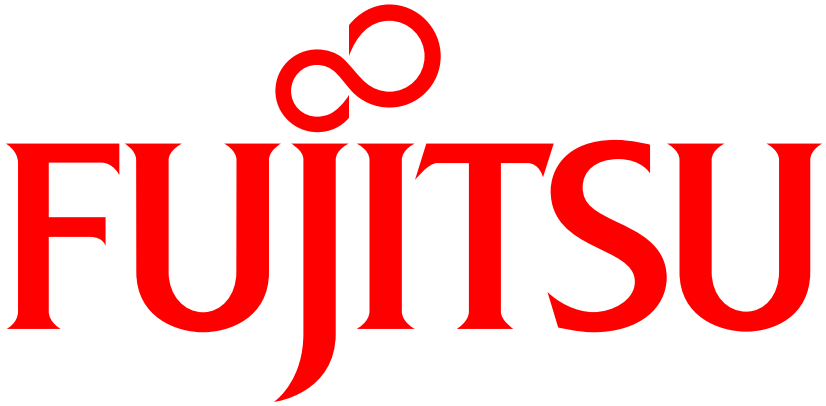

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