FPGA Prototyping using Behavioral Synthesis for Improving Video Processing Algorithm and FHD TV SoC Design

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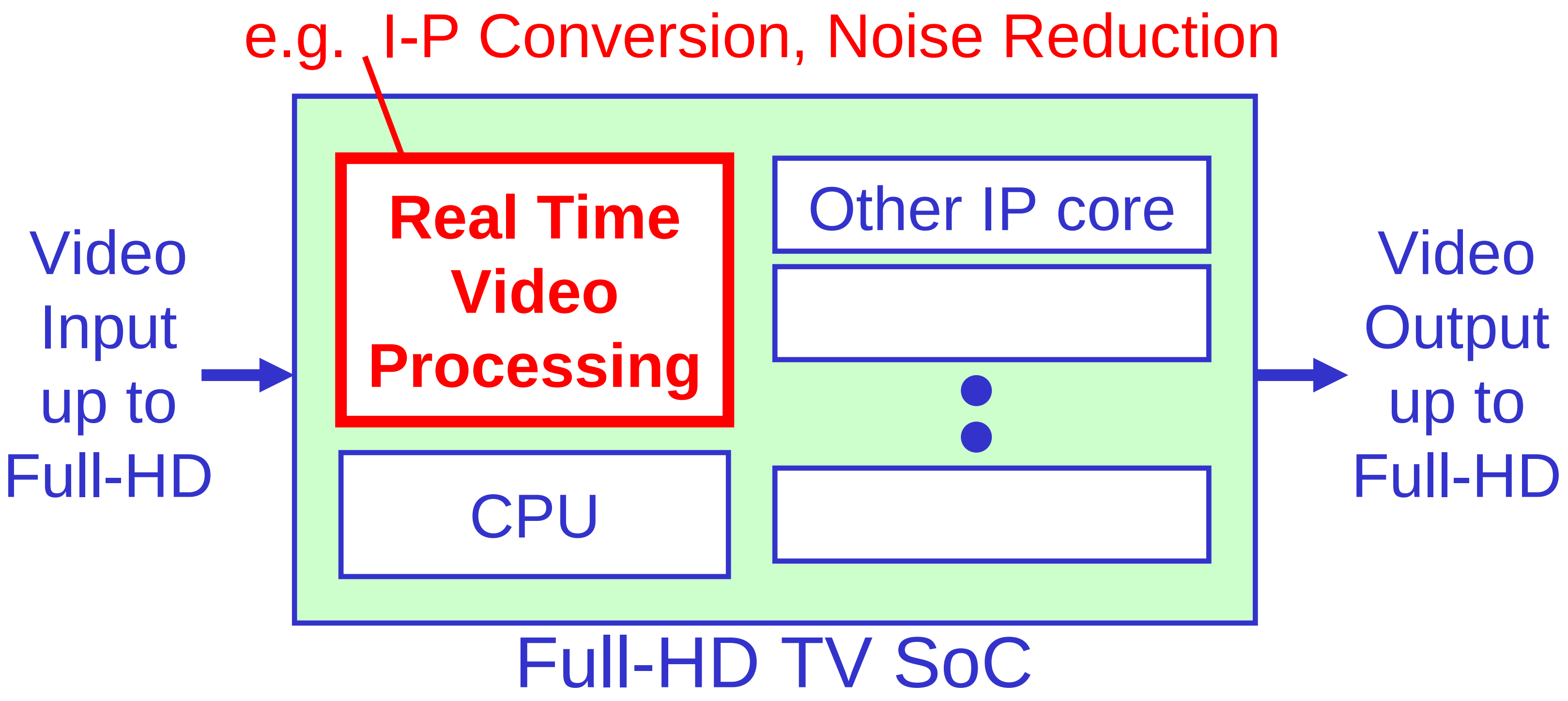
January 28, 2011

Outline

- Background and Issues
    - Video Processing for FHD TV SoC
    - Estimation System
    - Conventional Design Flow
- Proposal Design Flow
- SystemC Description
- Results of Development
- Conclusion

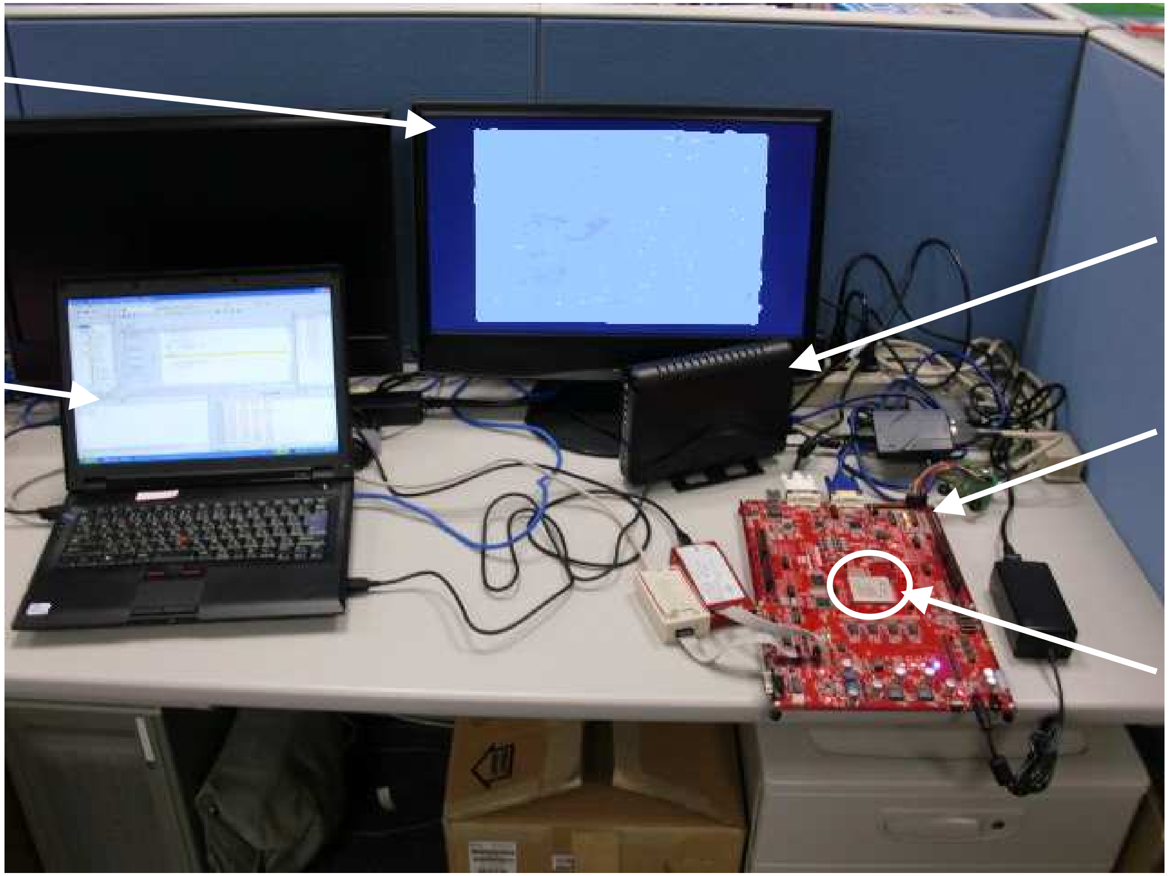
Background and Issues: Video Processing for FHD TV SoC


e.g. I-P Conversion, Noise Reduction
Video Input up to Full-HD
Real Time Video Processing
Other IP core
CPU
Video Output up to Full-HD
Full-HD TV SoC

- Picture Quality of SoC is affected by **Video Processing Algorithm**
- **Estimation and Improvement** are necessary before Implementation

Background and Issues: Estimation System

- Example of Estimation System
- Real Time Estimation by **FPGA Prototyping**



TV Monitor

PC for FPGA configuration and control

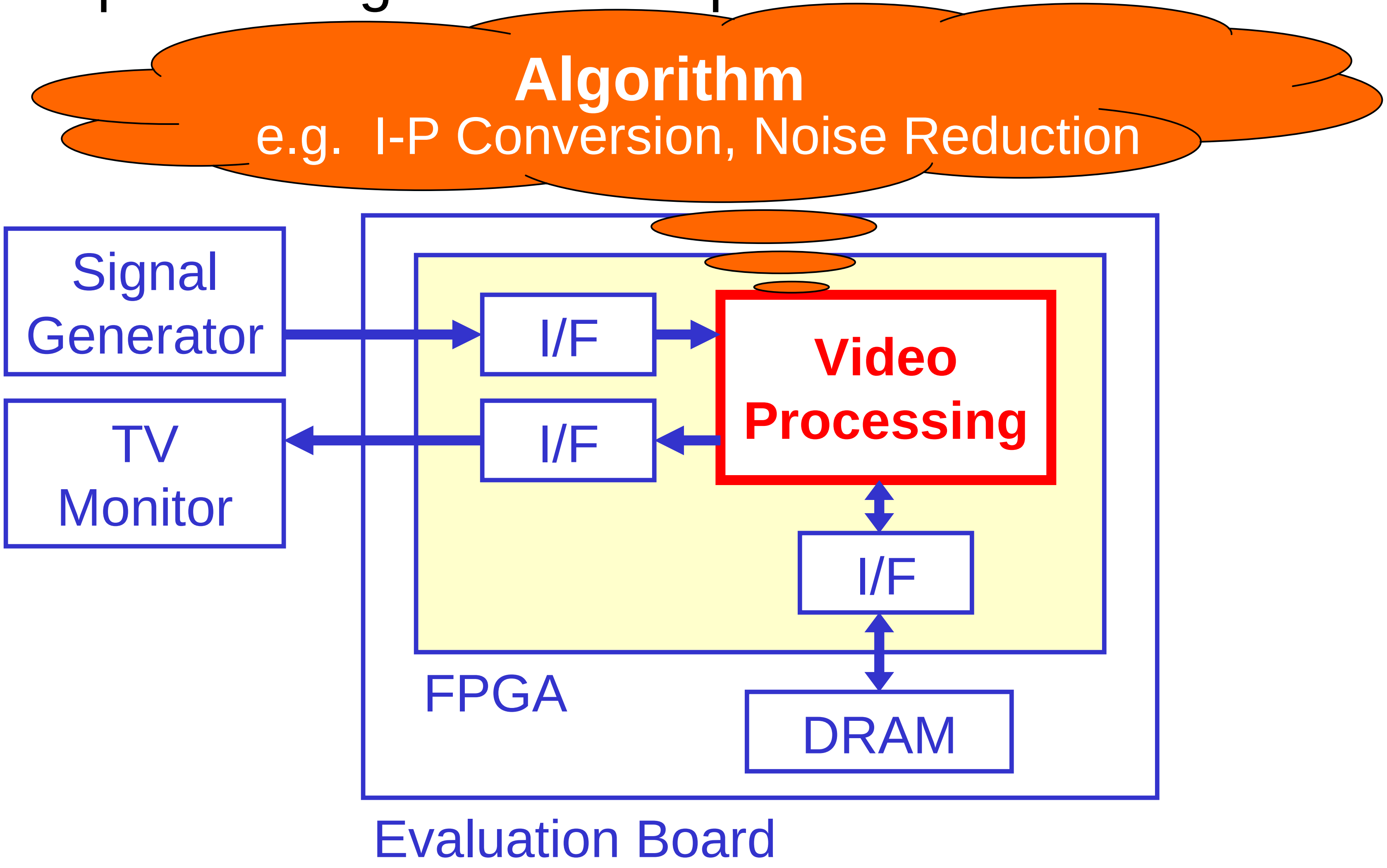
Signal Generator (HDD recorder)

Evaluation Board

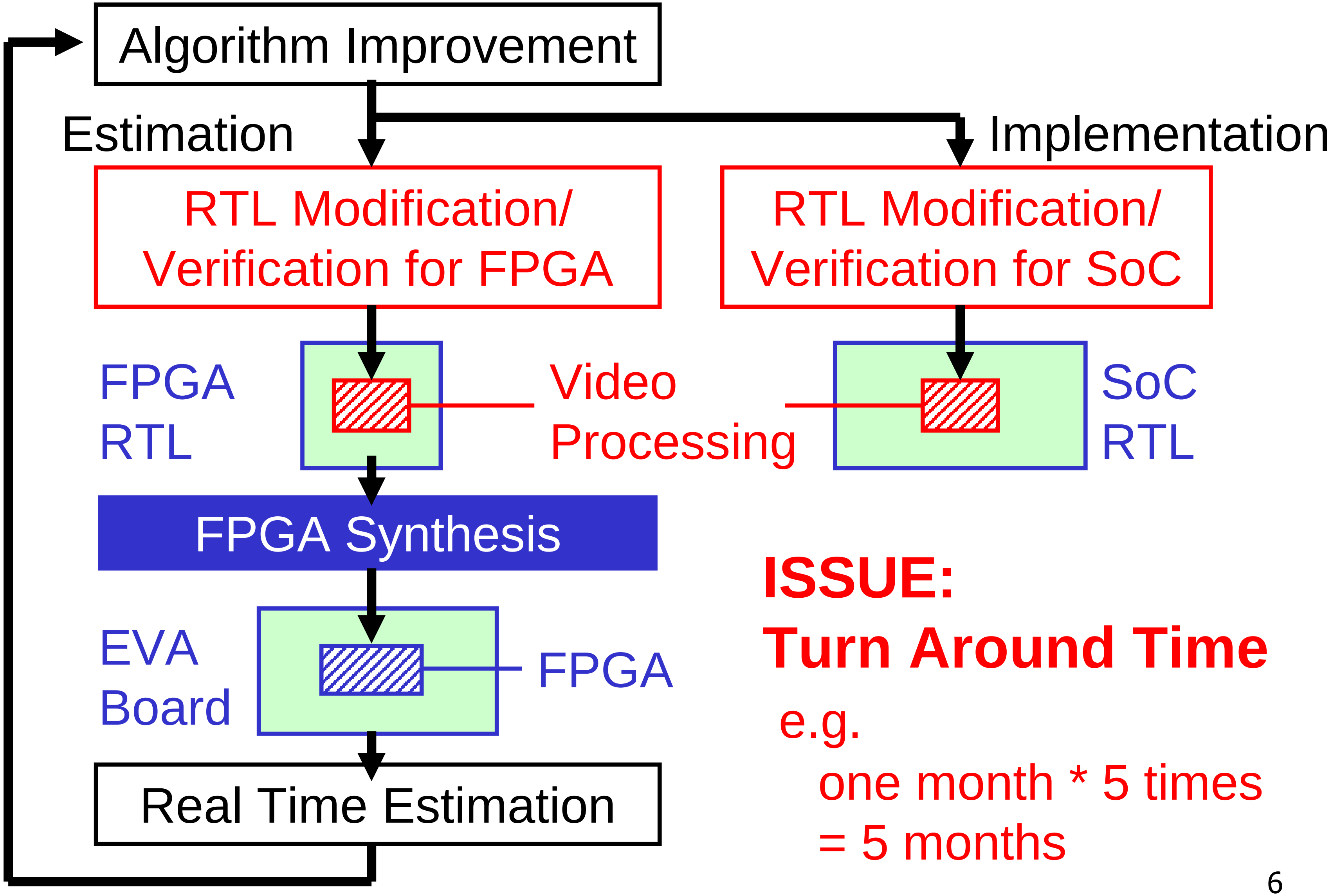
FPGA

Background and Issues: Estimation System

- Improved Algorithm is implemented on FPGA



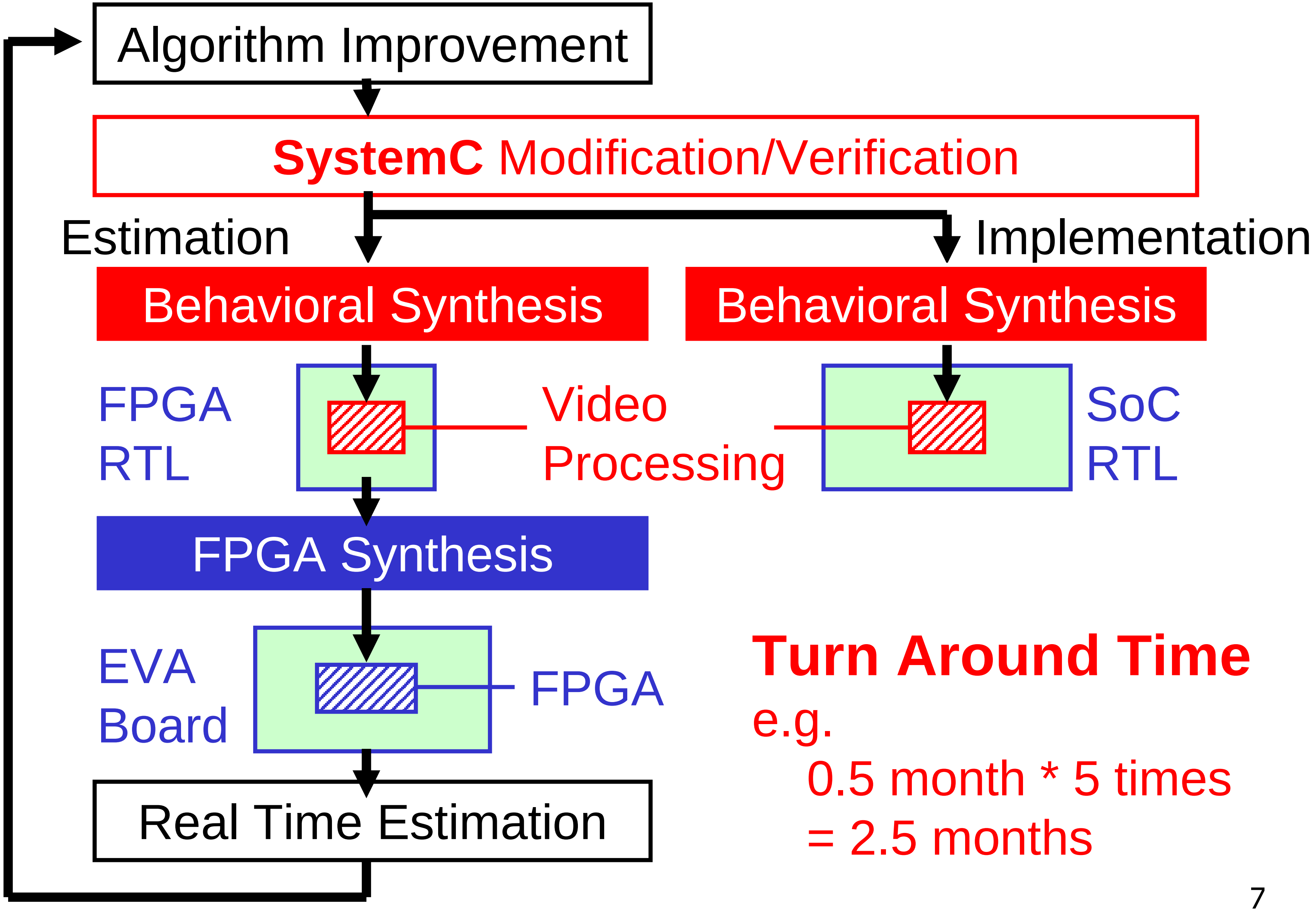
Background and Issues: Conventional Design Flow



ISSUE:
Turn Around Time

e.g.
one month * 5 times
= 5 months

Proposal Design Flow



Algorithm Improvement

SystemC Modification/Verification

Estimation

Implementation

Behavioral Synthesis

Behavioral Synthesis

FPGA
RTL

Video
Processing

SoC
RTL

FPGA Synthesis

EVA
Board

FPGA

Real Time Estimation

Turn Around Time

e.g.

0.5 month * 5 times
= 2.5 months

Proposal Design Flow: Summary

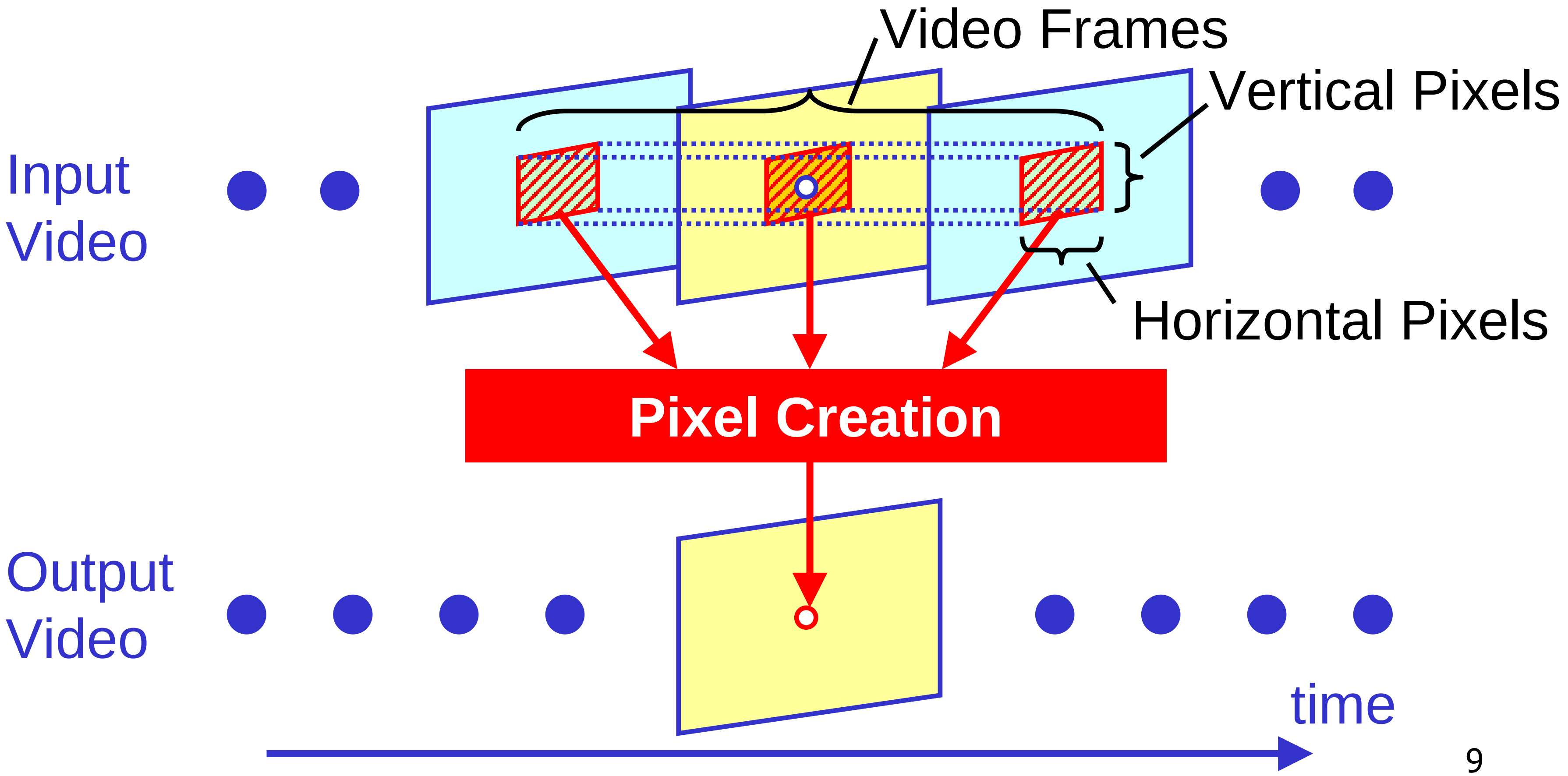
- **Short Turn Around Time** for Estimation
  - SystemC and Behavioral Synthesis
  - Updating FPGA is easy
  - About half as long as without Behavioral Synthesis

- Easy to Implement on SoC
  - Same SystemC, different Behavioral Synthesis

Next: How to Describe **SystemC Description**

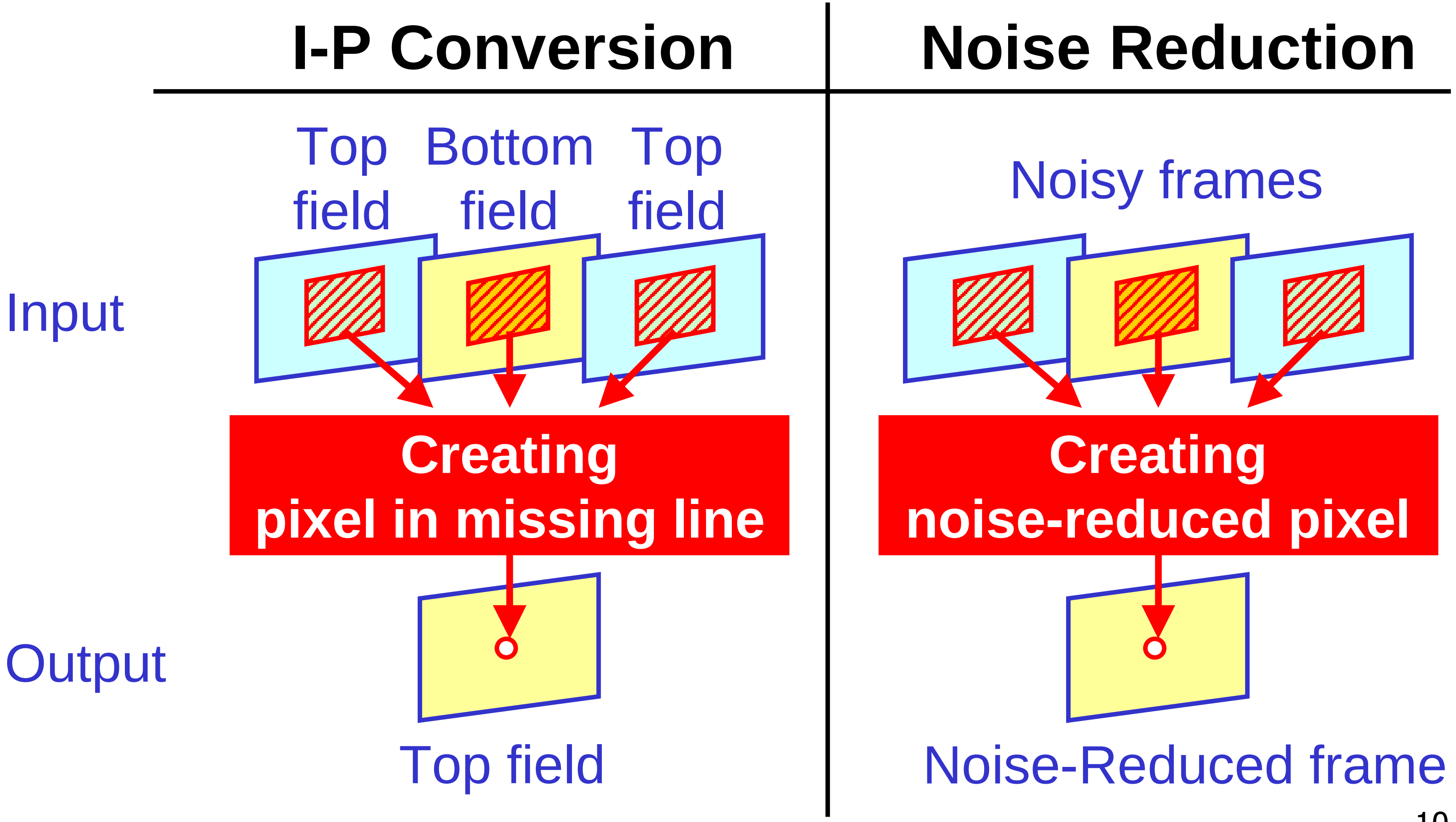
SystemC Description: What kind of Processing?

- For a pixel of Output Video, **Spatiotemporally neighbor** pixels of Input Video are referred.



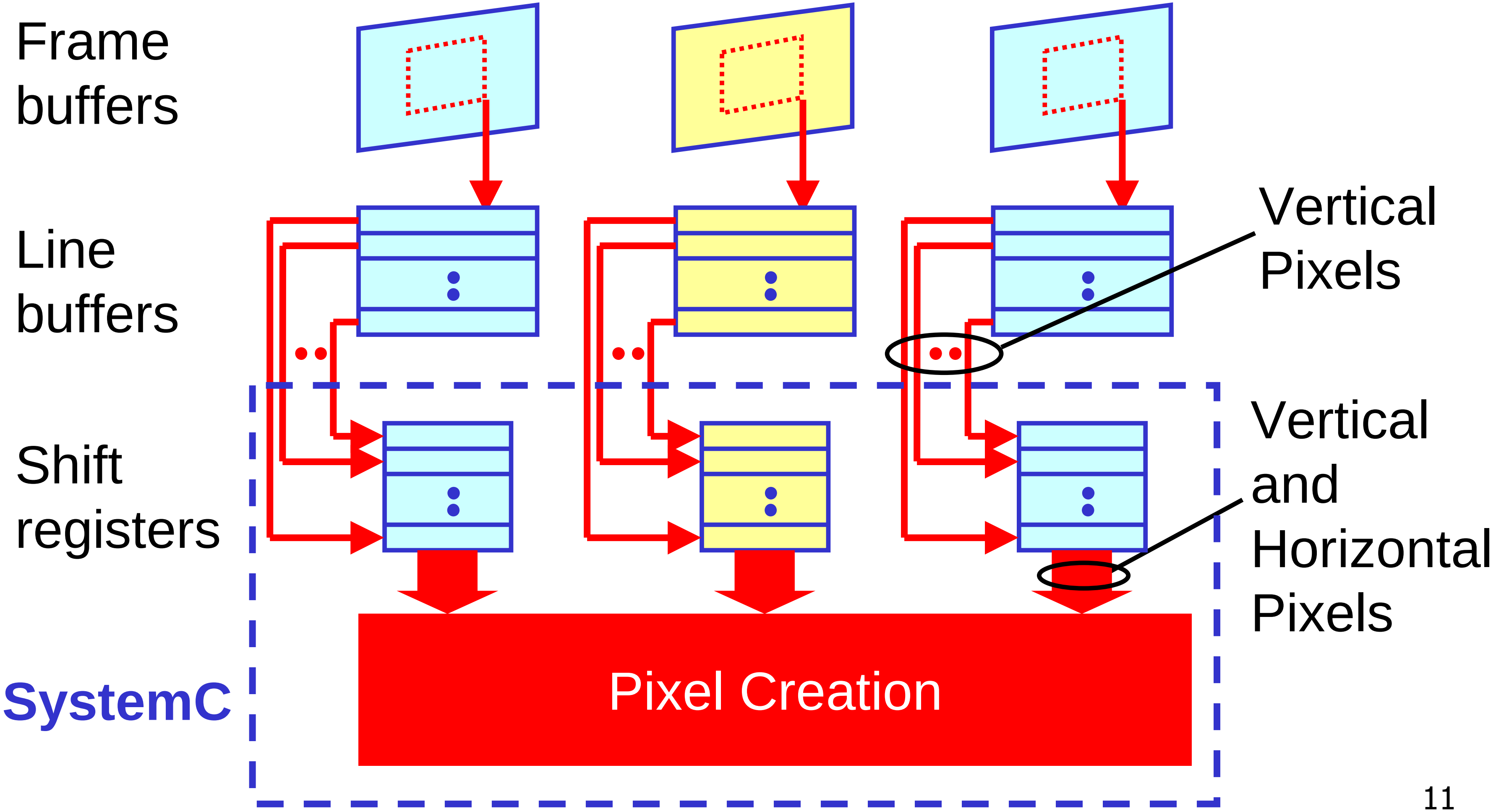
SystemC Description: What kind of Processing?

- Examples: Different Algorithm, Similar Interface



SystemC Description: Data Input

- Raster scan order



SystemC Description : Example

- **Pipeline Synthesis** is available

```
while(1){
    for( f=0; f<3; f++ ){
        for( y=0; y<H; y++ ){
            for( x=W-1; x>0; x-- ){
                shiftreg[f][y][x] = shiftreg[f][y][x-1];
            }
            shiftreg[f][y][0] = indata[f][y].read();
        }
    }
    outsig = output_pixel( shiftreg ); //function
    outdata.write( outsig );
    wait();
}
```

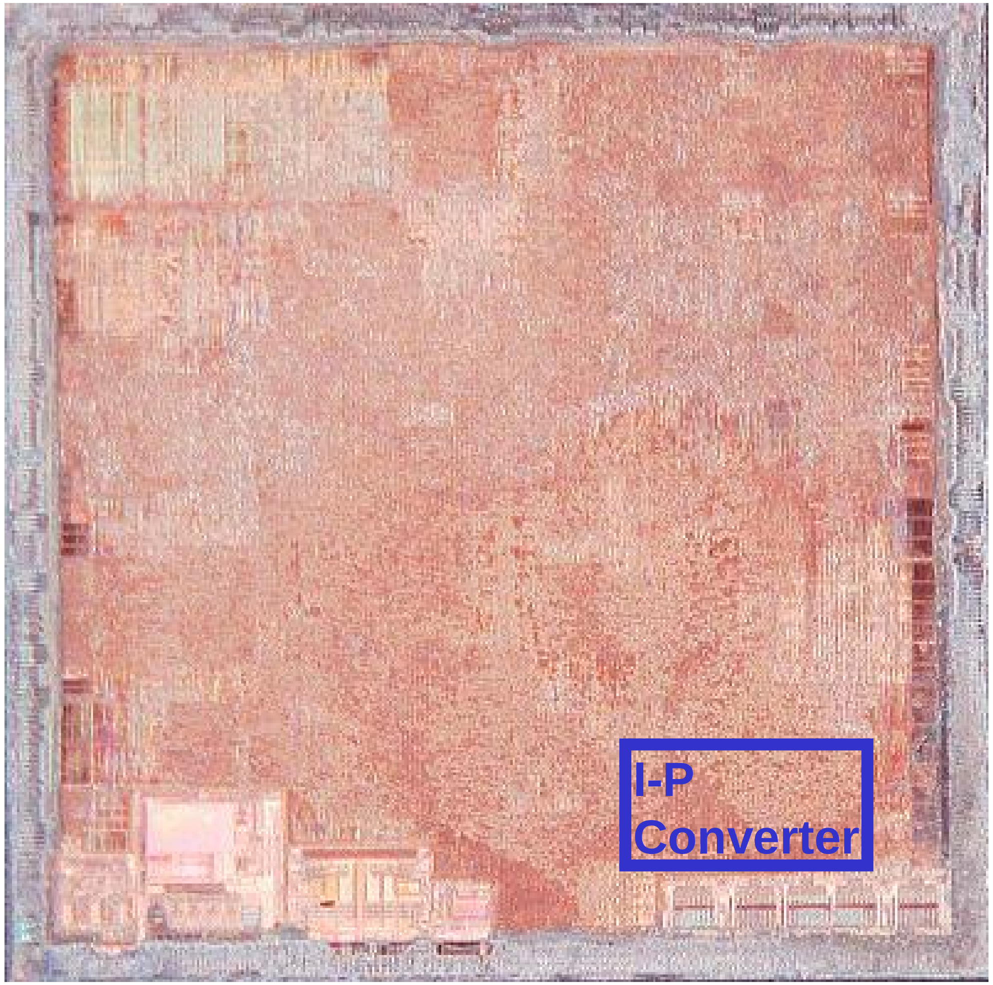
Shift Registers

Main Algorithm (**Pipeline Synthesis**)

1 cycle per pixel

Results of Development: Example of SoC

- Interlace-Progressive Converter on FHD TV SoC



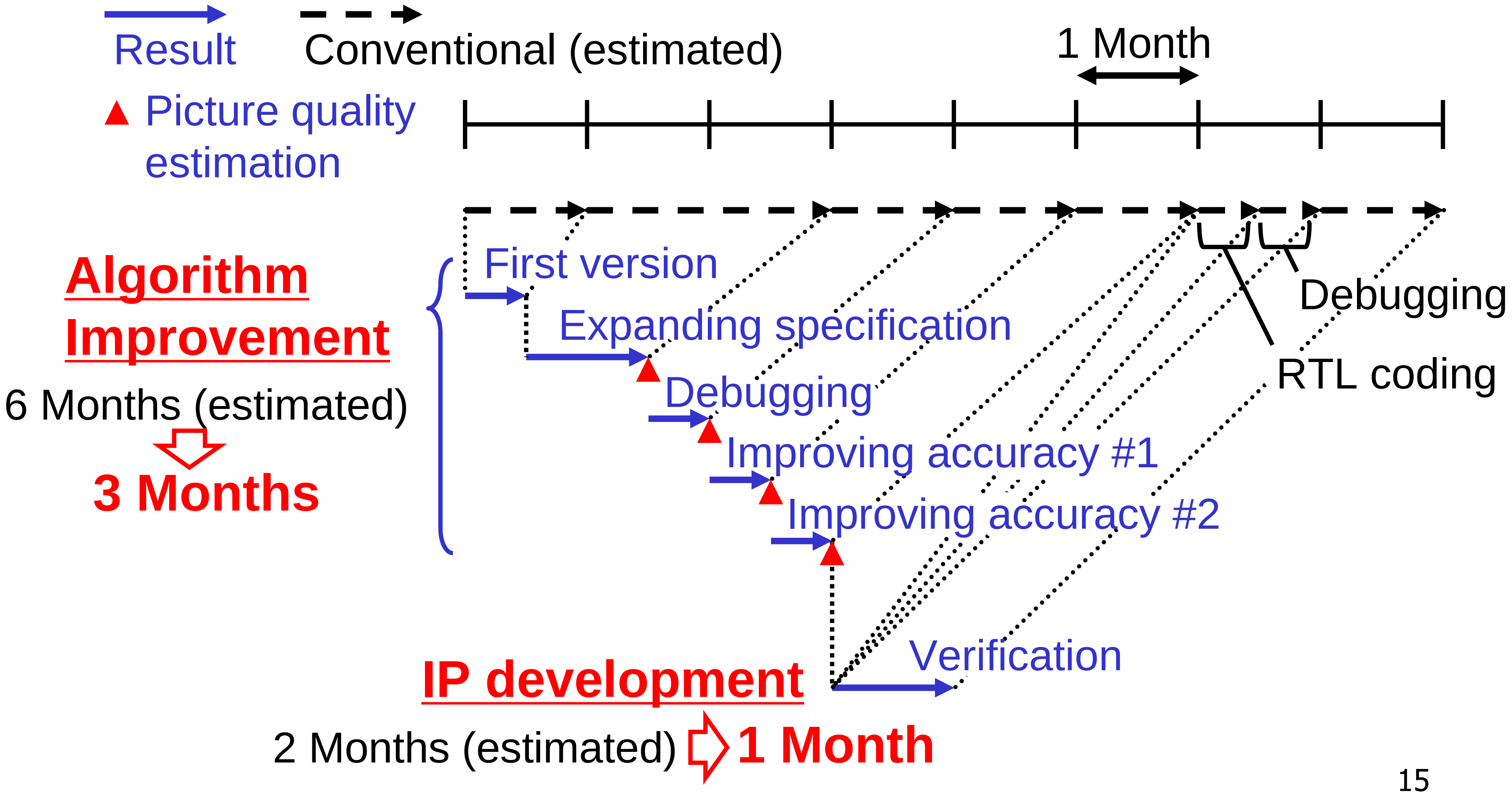
Results of Development: Developed IP lists

- Three designs have been developed

Function	SystemC Code	Development Period		Gate Count	SoC
		Algorithm Improvement	IP Development		
Interlace-Progressive Converter	13.5 klines	3 Months	6 Months	785 kGates	SH-Mobile MT1
Cinema Detection	3.6 klines	3 Months	4 Months	35 kGates	Under development
MPEG Block Boundary Detection	4.1 klines	3 Months	1 Month	135 kGates	Under development

Results of Development: Development Period

- Detail schedule of MPEG block boundary detection



Result

Conventional (estimated)

▲ Picture quality estimation

1 Month

Algorithm Improvement

6 Months (estimated)

3 Months

First version

Expanding specification

Debugging

Improving accuracy #1

Improving accuracy #2

Debugging

RTL coding

Verification

IP development

2 Months (estimated) **1 Month**

Conclusion

- We provide New Design Flow of Video Processing Algorithm using Behavioral Synthesis.

- Turn Around Time is about half as long as that without Behavioral Synthesis

- Three designs have been developed using New Design Flow