An RTL-to-GDS2 Design Methodology for Advanced System LSI

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Contributing to a Bigger Application Ecosystem

What system LSI do we make?

How do we design easily ?

Design Methodology

- What design steps are required?
- What kind of data and design constraints must be created?
- What kind of design information must be verified?
- What kind of information must be passed to next design stage?
- How can manufacturability be assured at the design stage?
- How variations must be taken care?

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Common Design Technology Infrastructure

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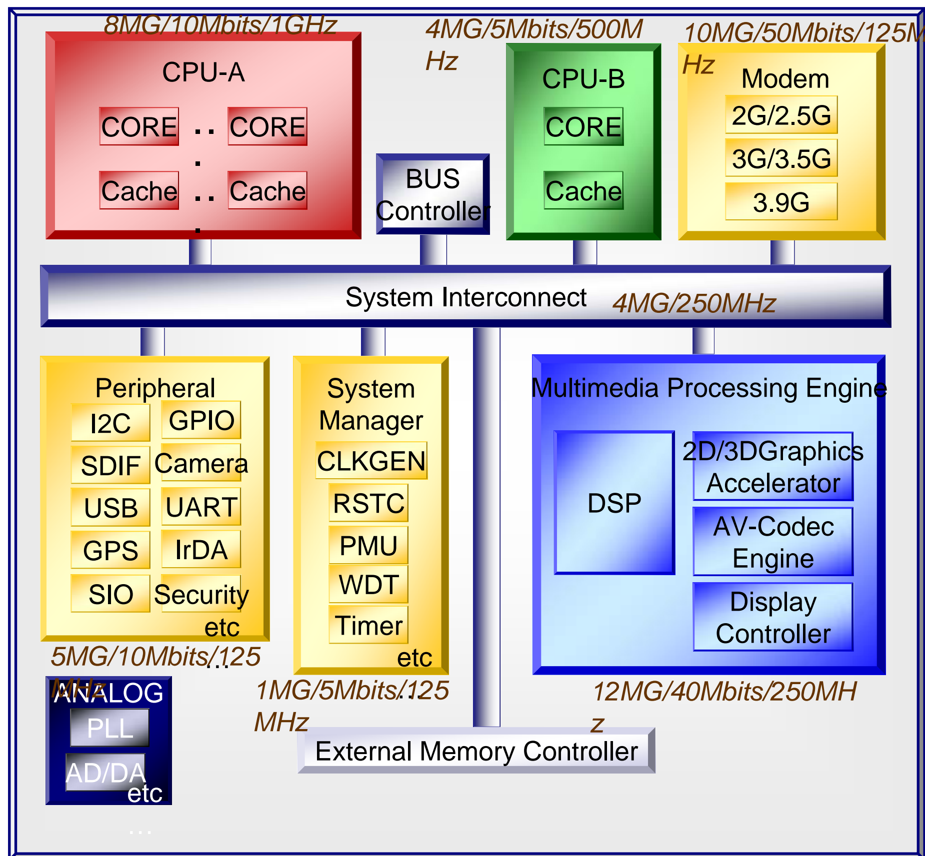
Target System LSI and Design Technology



Target System LSI
(44Mgates, 1GHz, 32nm)

■ Design productivity

- Design and manufacturing aware integrated design flow
- Chip feasibility estimation technology
- Parallel and distributed processing

■ Low power

- Power reduction technology
  - DVFS
  - Efficient Low Power implementation technology
- RTL power estimation and optimization

■ Variation aware

- Variation tolerant clock
- Integrated variation aware analysis
  - Power, Thermal, Noise, Cross talk, Stress/Litho/CMP analysis

■ Manufacturing aware

- Integrated litho, manufacturing defect and dummy fill aware design technology
- Electrical DFM

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Low Power Design

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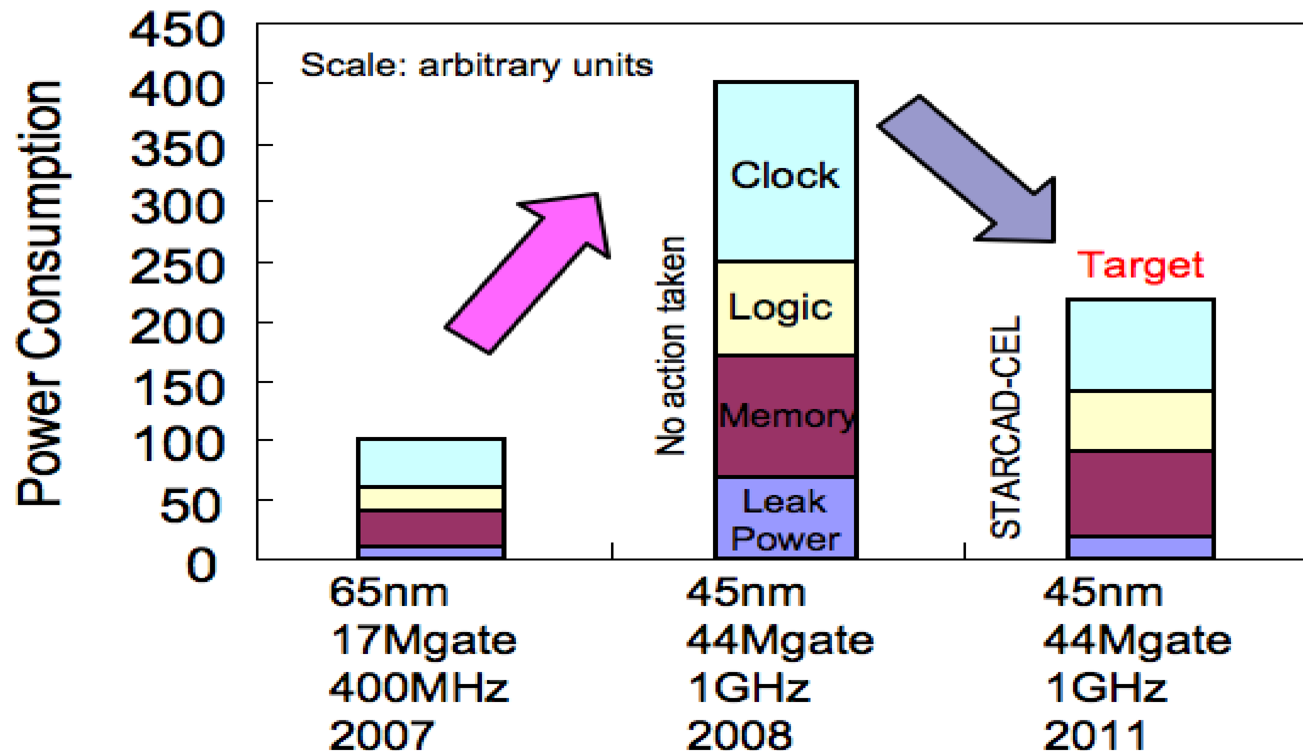
Increasing Power Consumption

- Large Scale and High Speed
- Increasing amounts of embedded memory
- Low Vth due to lower power supply voltages

⇒ increasing dynamic and leakage power



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Types of Low Power Design Techniques

- Various power reduction techniques exist, but they should be combined depending on the specification of the LSI

Low Power Design Technology		Main Power Component Which is Reduced	
		Dynamic Power	Leakage Power
Low Voltage	Multi VDD	○	○
	Power Control（DVFS）	○	○
Switching Reduction	Gated Clock	○	×
Leakage Reduction	Multi Vth	×	○
	VTCMOS (Substrate control)	×	○
	Power Gating	×	○
	MTCMOS (Power gating)	×	○
	Optimization of L	×	○
Other	Low Power Synthesis/P&R	○	○
	Pulsed latch	○	×

The items in pink are areas which STARC has developed

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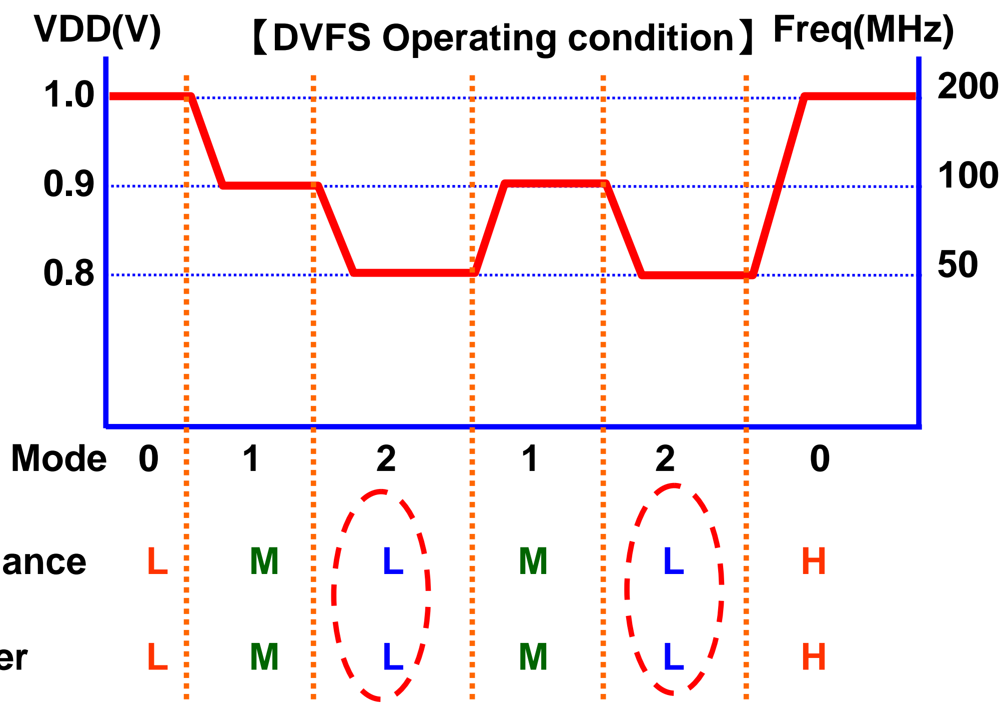
What is DVFS?

DVFS (Dynamic Voltage Frequency Scaling) is a way of reducing power consumption by in a specific block by pre-defining a number of combinations of Voltage and Speed which can selected according to the processing requirements.
This functionality has to be embedded into the chip during the design stage.

Mode	Voltage (V)	Speed (MHz)	Performance	Power
0	1.0	200	H	H
1	0.9	100	M	M
2	0.8	50	L	L



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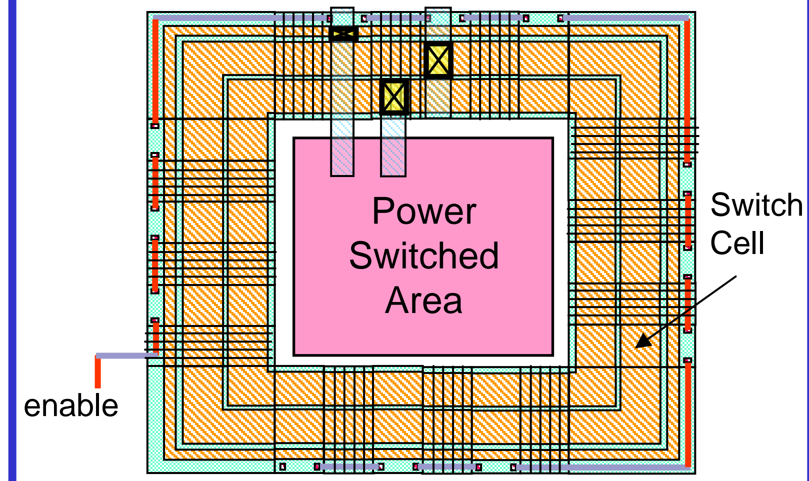
DVFS Implementation

- **Multi Mode Logic Synthesis**
- **Multi mode Multi Corner Clock Synthesis**
- **Ring Style power switch placement**
- **Multi Mode Multi Corner Timing optimization**

Ring Style Power Switch Placement

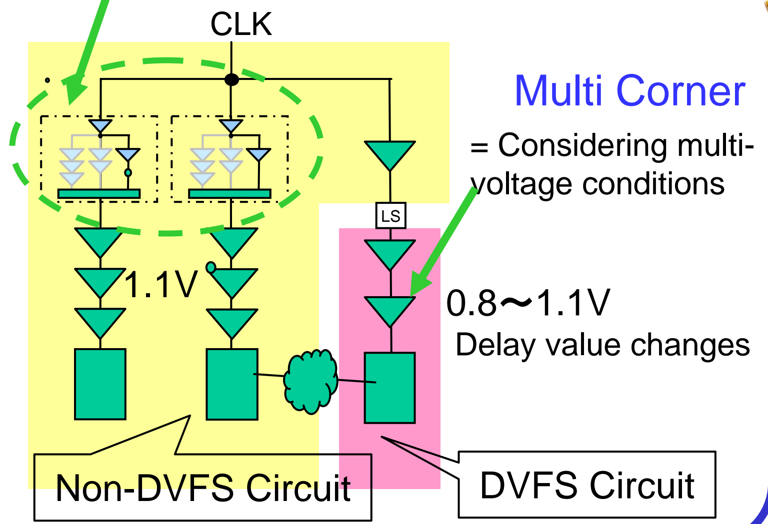


Switch placed around Non-DVFS Circuit

Clock Synthesis

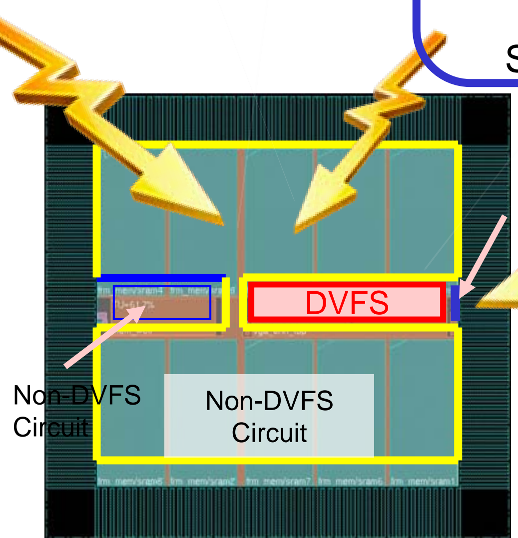
Multi Mode

= voltage and clock path considered for each mode



Multi Corner

= Considering multi-voltage conditions



DVFS Test bench data

Multi-Mode Multi Corner Timing Optimization

Optimization for 30 scenarios

DVFS Operating modes : 5
Sign Off Corners : 6

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Multi power domain timing analysis

Inter power domain (IPD) coefficient method reduced the number of combination for power domains

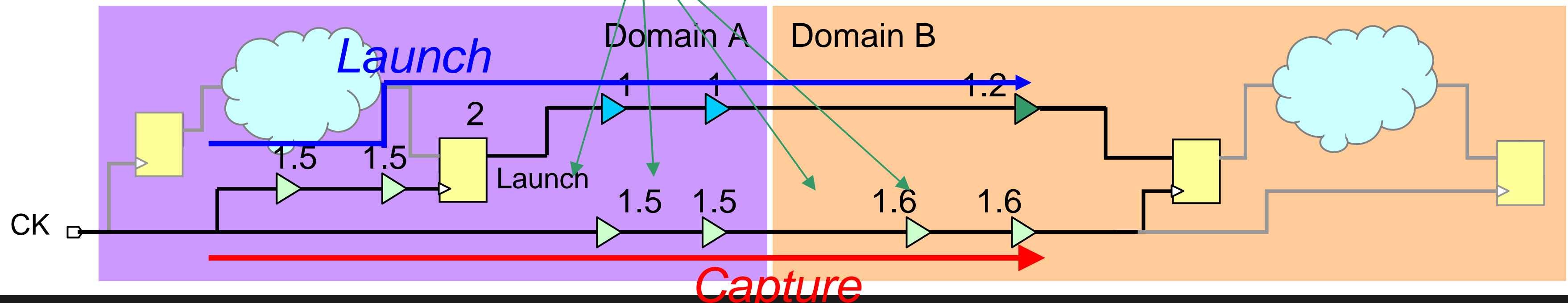
$$m \cdot c \cdot (2^n - 1) \rightarrow m \cdot c$$

(Ex.)
Mode (m)=6,Corner (c)=9、6,Power domain (n) =3 →

CPU-A (Multi-Core)	CPU-B	Multimedia Engine	Peripherals	System Interconnect	Traditional	IPD
DVFS Mesh	DVFS Mesh	Middle Frequency	Low Frequency	Middle Frequency	Number of STA (3 power domain)	Number of STA (3 power domain)
1.1±0.1	1.1±0.1	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
1.1±0.1	1.0±0.1	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
1.1±0.1	0.9±0.05	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
1.0±0.1	1.1±0.1	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
1.0±0.1	1.0±0.1	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
1.0±0.1	0.9±0.05	1.0±0.1	0.9±0.05	1.0±0.1	9×8=72	6×1 =6
				STA	432	36

The number of corner reduction will be explained in the next chapter

An example for high-voltage min (hold check) analysis



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Variation-aware Design and DFM

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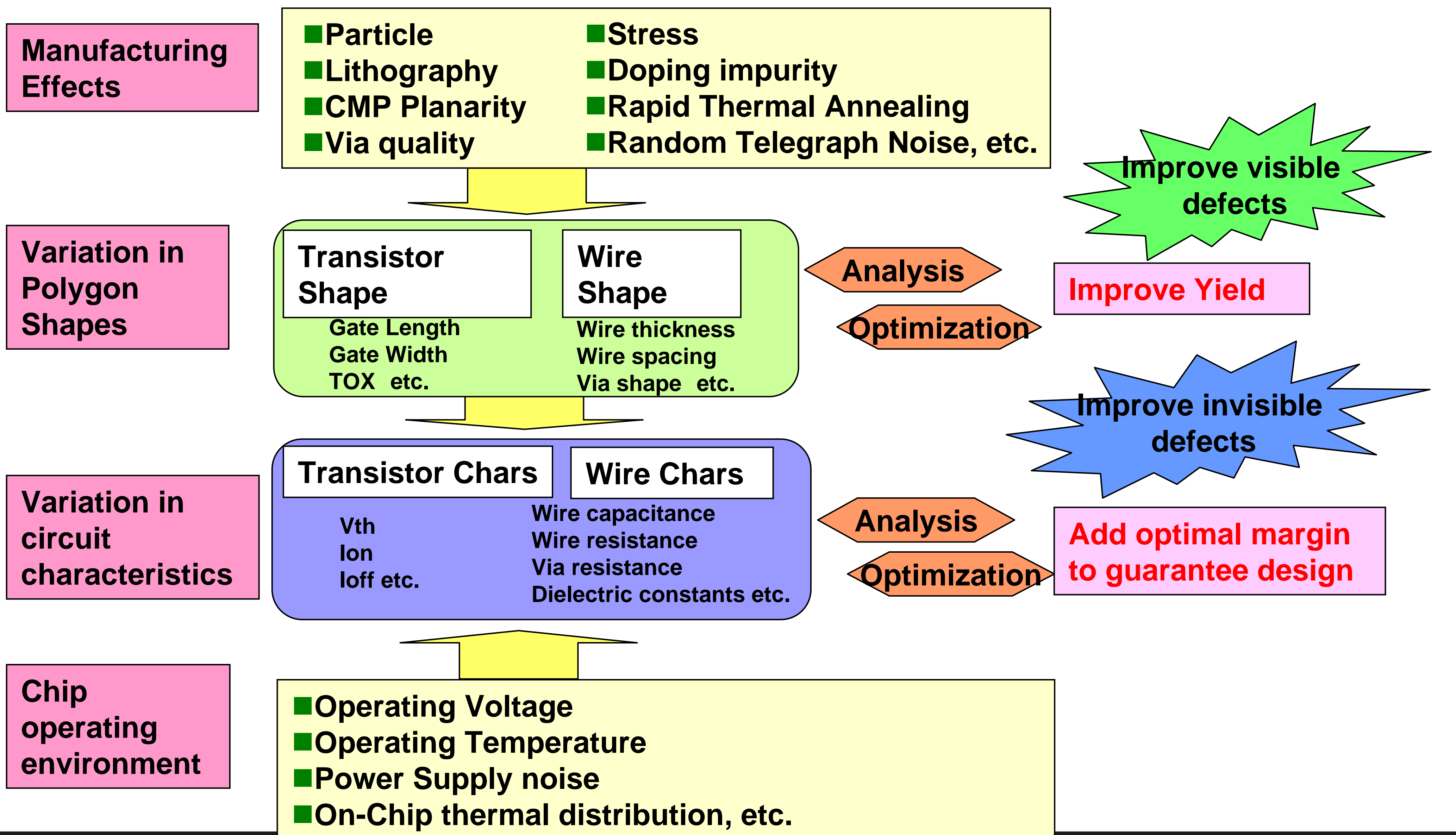
Variation and DFM Aware Design



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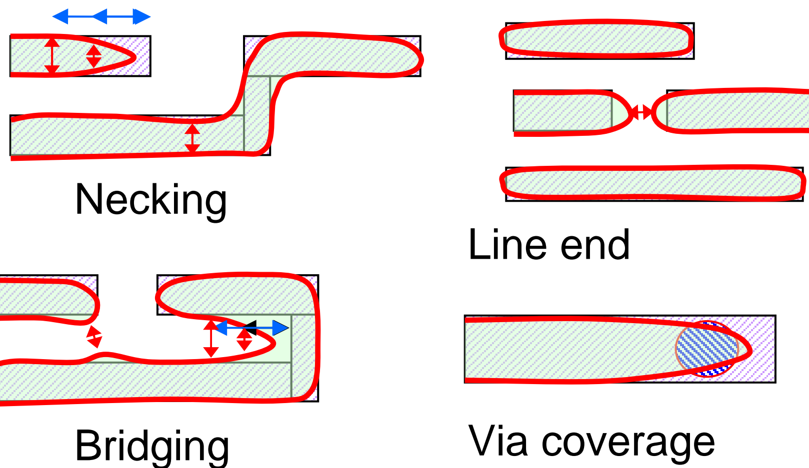
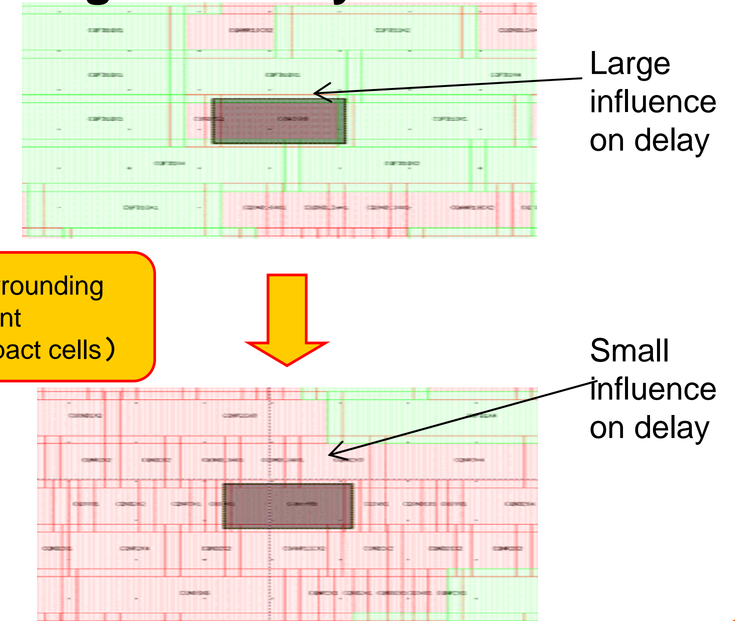
Visible and Invisible Defects

Visible Defects (e.g. litho hotspots)



Invisible Defects (e.g. changes in delay due to STI stress



Prevention (avoiding specific patterns) and routing optimization (fix wiring) -> eliminate litho hotspots

Control delay variation -> improve timing convergence

Moving from visible defects to invisible defects

Electrical DFM

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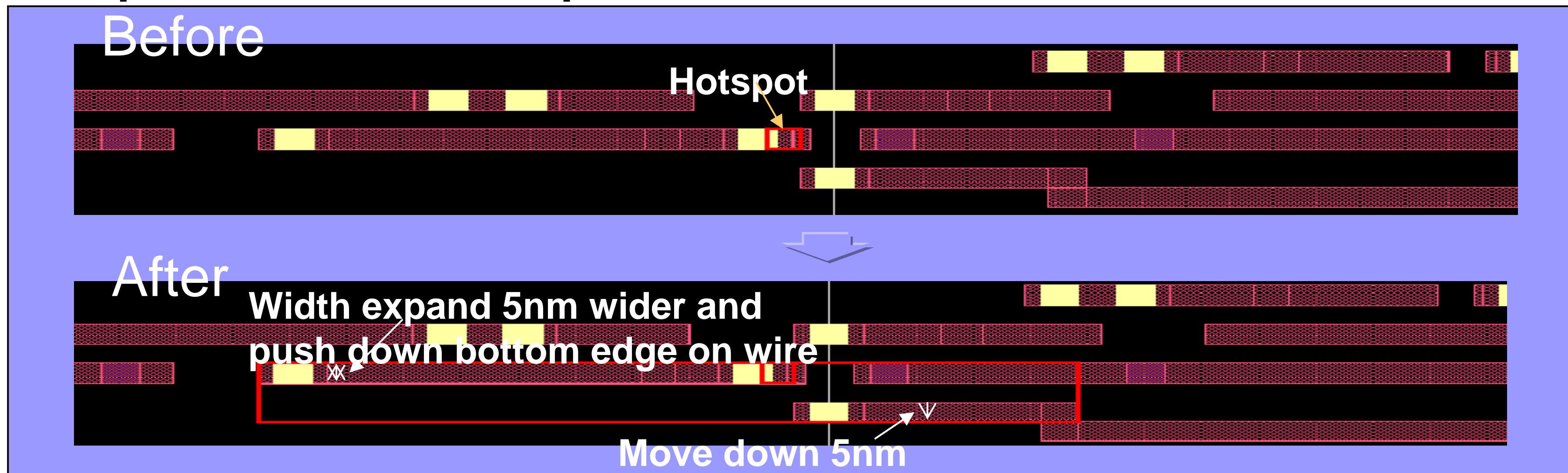
DFM-aware Design Results

	Defect	Countermeasure	Design Index	Design Criteria	Result	
Random	Manufact -uring	Increase Wire Width, Increase Wire Spacing	Critical Area (CA)	Reduce critical area	Critical area	**5.1% Improvement**
	Via	Add double vias	Ratio of defective vias	Ratio of double vias > 80%	Double via ratio	**88.45%**
Systematic	Litho hotspot	Litho Hotspot prevention → Analysis→ fix	Hotspot Error Count	Proportion of Criticality 1 hotspots fixed 100%	Percentage of critical hotspots fixed	**100%**

Litho hotspot correction example



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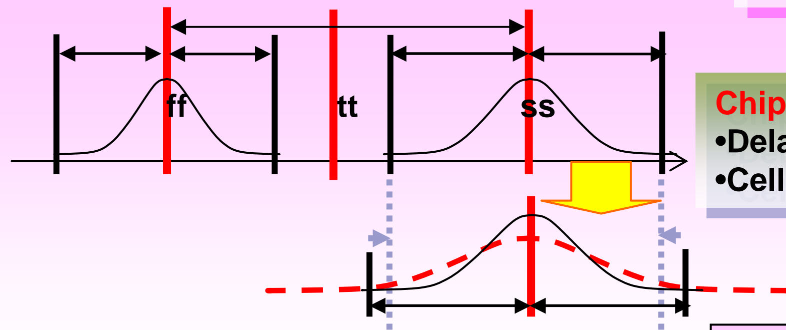
Electrical DFM Design Flow

Goal

Reduce design margin
➔ Shorten design turnaround time
(same design margin
➔ Improve parametric yield loss)

Transistor and wire modeling
Lithography / Etch contour
Stress

Cell characterization
Cell Library



Chip level optimization
- **Delay calculation**
- **Cell placement optimization**

Reduce OCV by 22%

Without DFM → Red dotted line
With DFM → Reducing design margins

E-DFM Usage Model

Litho/Etch aware Phase
- Litho Simulation
- Etch Simulation
- Contour-Base Leff/Weff Extract
- Contour-Base RC Extract
- Leff/Weff Contour-Base RC

Stress aware Phase
- Measurement (LOD/STIW etc)
- Convert (Vth0/U0 etc)
- Δ Vth0/ Δ U0

Library Characterize Phase
- Characterize Tool
- E-DFMed Library

Chip level Phase
- Chip/Block E-DFM Tool
- ・Litho/Etch Analysis (Leff/Weff, Contour-Base RC)
- ・Neighborhood Cell Analysis (Distance・Placement、Cell type)
- SDF+
- Adjusted .lib

STA Phase
- Golden STA/SSTA
- STA Report

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Variation Aware Design Technology

Signoff Corner Reduction Scenario
（Corner Count 9 ⇒ 6⇒ 4）

Signoff Corners：
Combined number of verification conditions needed to guarantee design.

Corner Count
16
14
12
10
8
6
4
2
0
Original Technology
Variation Tolerant Clock
Integrated variation-aware flow
2007(45nm)
2008 (45nm)
2010
2011 (32nm)

Signoff Corners

2H08 45nm 9 Corner

P	V	T	W
FF	1.2	−40	Cmin
FF	1.2	−40	RCmin
FF	1.2	125	Cmax
FF	1.2	125	Cmin
FF	1	125	Cmin
SS	1	−40	Cmax
SS	1	−40	RCmax
SS	1	125	Cmax
SS	1	125	RCmax

1H10 45nm 6 Corner Robust Clock

P	V	T	W
FF	1.2	−40	Cmin
FF	1.2	−40	RCmin
FF	1.2	125	Cmin
SS	1	−40	Cmax
SS	1	125	Cmax
SS	1	125	RCmax

2H10 45nm 4 Corner Variation aware

V	T
1.2	−40
1.2	125
1	−40
1	125

P: Process
V: Voltage
T: Temperature
W: Wiring

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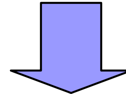
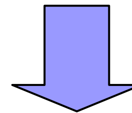
Sign Off Corners and Design Margin

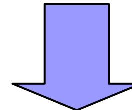
To reduce the number of Signoff corners We should increase the Design margin
（Design margin：guard band used at design time to ensure manufactured chip will work



When the margin is large the design time overhead is high



Need to reduce number of signoff corners without increasing design margin



Solution: variation tolerant clocks and integrated variation aware design flow

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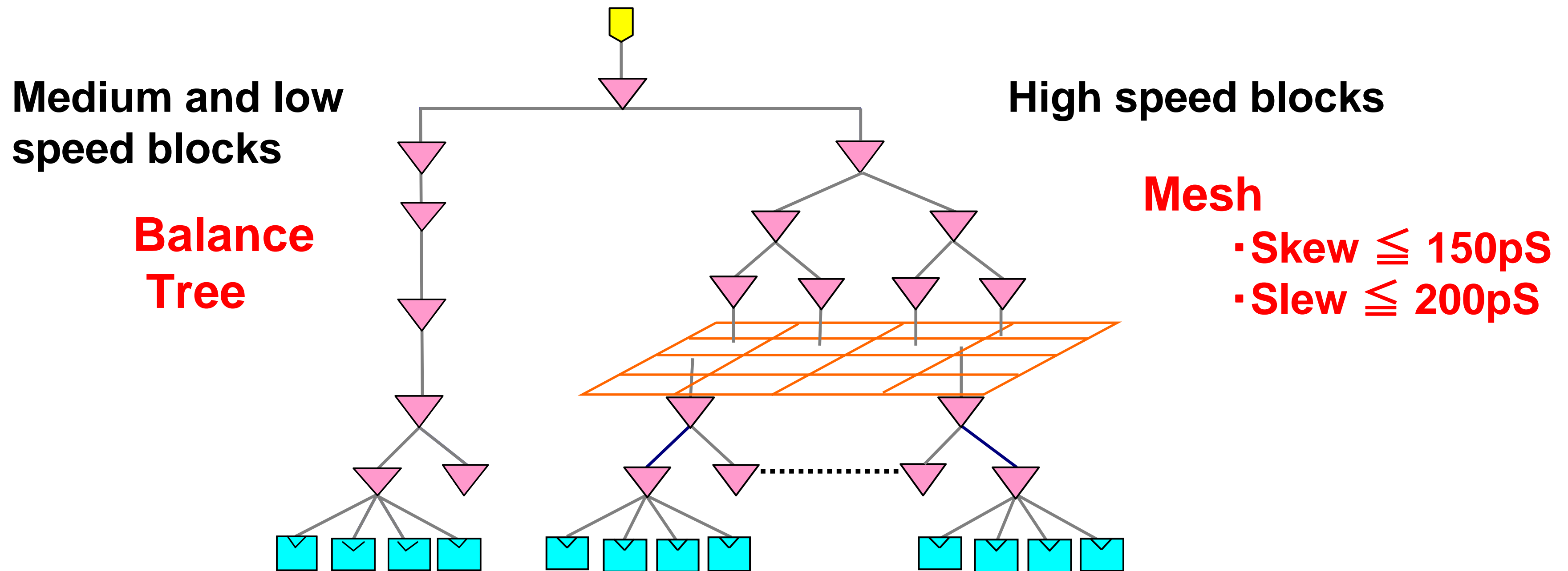
Variation Aware Design Technology

Variation Tolerant Robust Clocks



6 sign-off corners

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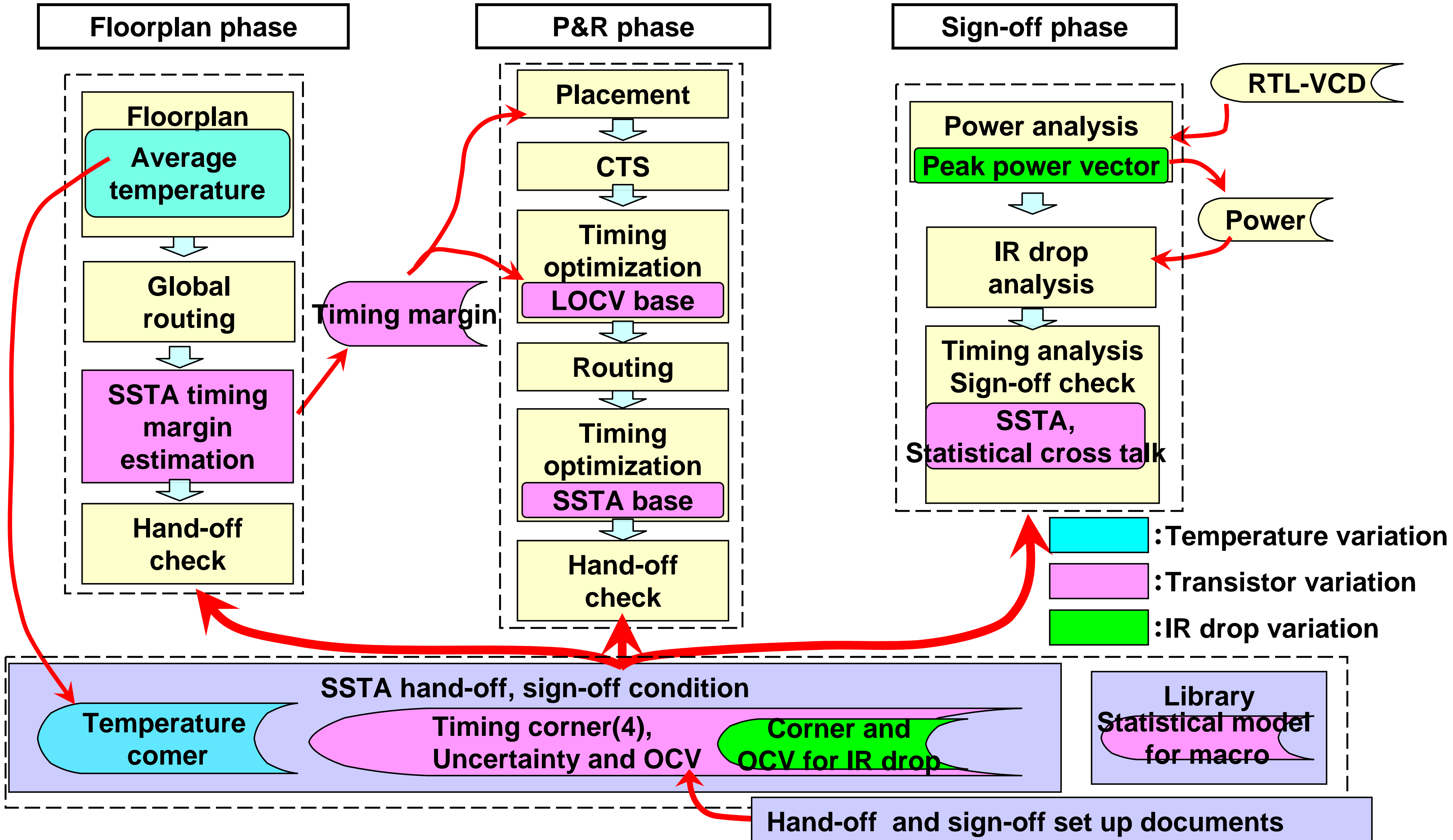
Integrated Variation Aware Design Flow



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Relationship between Technologies and Results

Shrinking Process

Low Cost
Business Profits

Optimize variation
through analysis of
physical effects

Variation aware
Design Technology

Manufacturing aware
design technology

Improved Yield

Low Power Consumption

Use variation aware design and optimize
·Design margin
·Signoff corners

Increased design complexity
due to manufacturing aware
design

Low Power
Design Technology

Design technology to
improve design productivity

High Design
Productivity

Increased design
complexity due to
low power design

Low Cost
Time to Market

Low Power LSI

Eco Society

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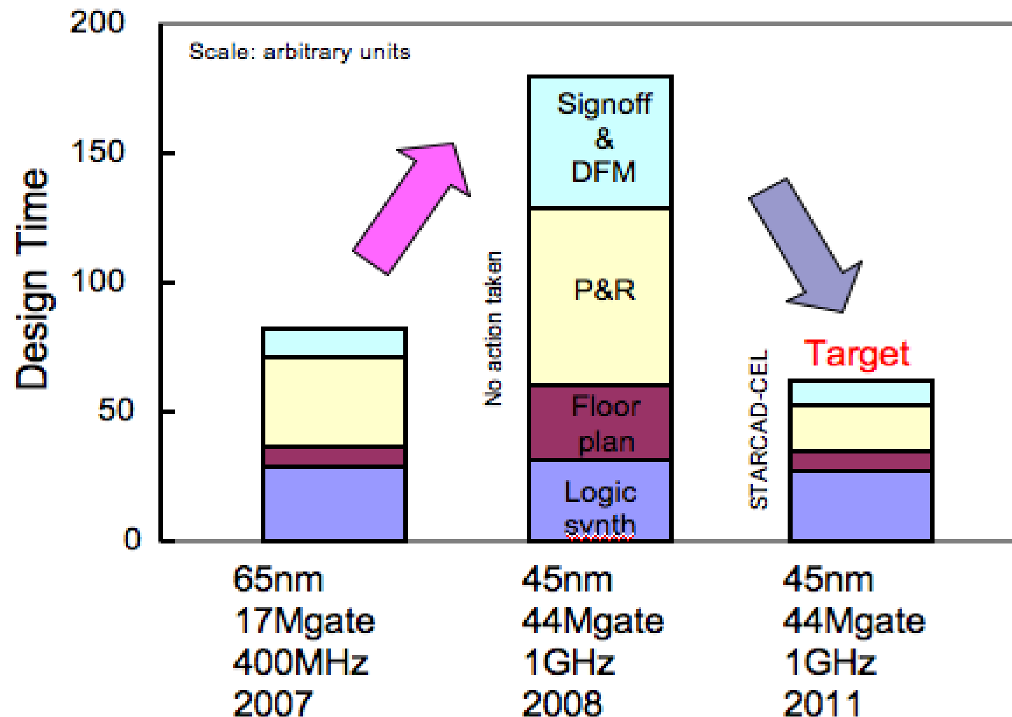
Increase in TAT due to Scaling

- Number and types of blocks included on chip increasing
- Number of power and clock domains increasing
  => Floorplanning becomes more complex, number of iterations increase
- Large scale, high speed, shrinking process nodes
  => Complexity of P&R, Sign off Verification, DFM get higher and TAT longer



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Design Methodology for Increased Productivity

Integrated design flow

Phase 0

Inputs: CPF/UPF, RTL, SDC, VCD

- Power Format check
- Low Power Sim
- RTL power opt.
- RTL DFT
- RTL prototyping
- RTL Power/ Timing/SDC checks
- FP aware Synthesis
- Handoff Check

Outputs: CPF/UPF, SDC, TGLFile, Netlist, FP-DEF

Phase 1

Inputs: CPF/UPF, SDC, TGLFile, Netlist, FP-DEF

- Detailed Floorplan
- Create Hierarchy
- Handoff Check

Outputs: CPF/ UPF, SDC, TGLFile, Netlist, FloorPlanデータ

Phase 2

Inputs: Netlist, FloorPlan data, SDC, CPF/ UPF, TGLFile

- Detailed Routing
- CTS, Clock Mesh
- Timing／Power Optimization
- Global/Detailed Routing
- Timing w/Xtalk Power Optimization
- Timin Analysis

Outputs: Netlist, Routing Data, CPF/UPF, SDC

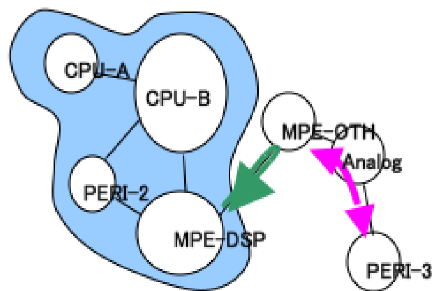
Phase 3

Inputs: Netlist, Routing data, SDC, CPF/ UPF, TGLFile

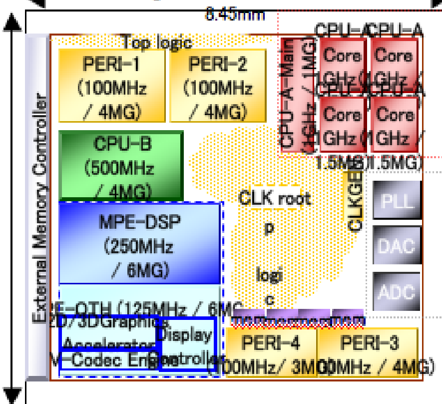
- DFM
- Signal-EM
- Static IR-Drop
- Dynamic IR-Drop
- Decap Insertion
- Rush Current Wake Up
- Timing Analysis
- Signoff Check

Output: GDSII

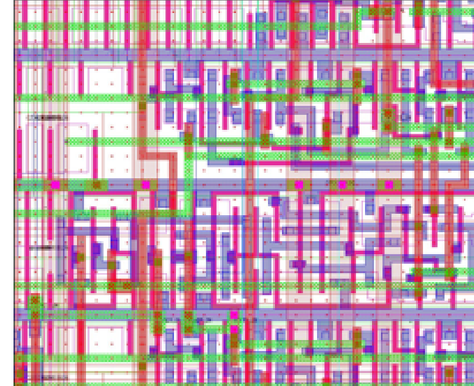
RTL Analysis



Floorplan



Place and Route



Signoff Checks

- Timing
- Signal Integrity
- IR Drop
- Dynamic Power
- Leak Power
- Design Rules
- Equivalence checks
- Litho Hotspots
- Density Rules

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Summary

- Increasing complexity and lengthening design times
  - Large Scale, High Speed, smaller feature size increase need for low power, variability and manufacturability aware design and in response to that design times are lengthening.
- Make design easier means identifying and using best design practices
  - Low power design technologies
  - Manufacturing aware and variability aware design
    - Move from invisible defects to visible defects
    - Sign off corners and design margins
    - Reduce number of signoff corners
  - Improve design productivity

Develop and promote a good design methodology！

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