Fault Simulation and Test Generation for Clock Delay Faults

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Outline

- Introduction
- Purpose
- Clock delay fault model
- Fault simulation results
- Test generation method
- Experimental results
- Conclusion

Introduction

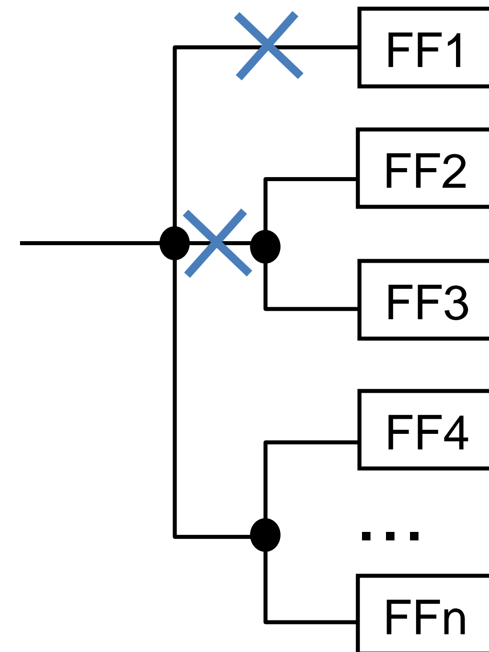
- Delay faults
  - Must be considered in testing of recent high-speed LSIs.
  - Logic gates and signal lines are considered.
- Clock lines
  - The number of FFs is increasing.
  - Defects on clock lines must be detected.

Purpose

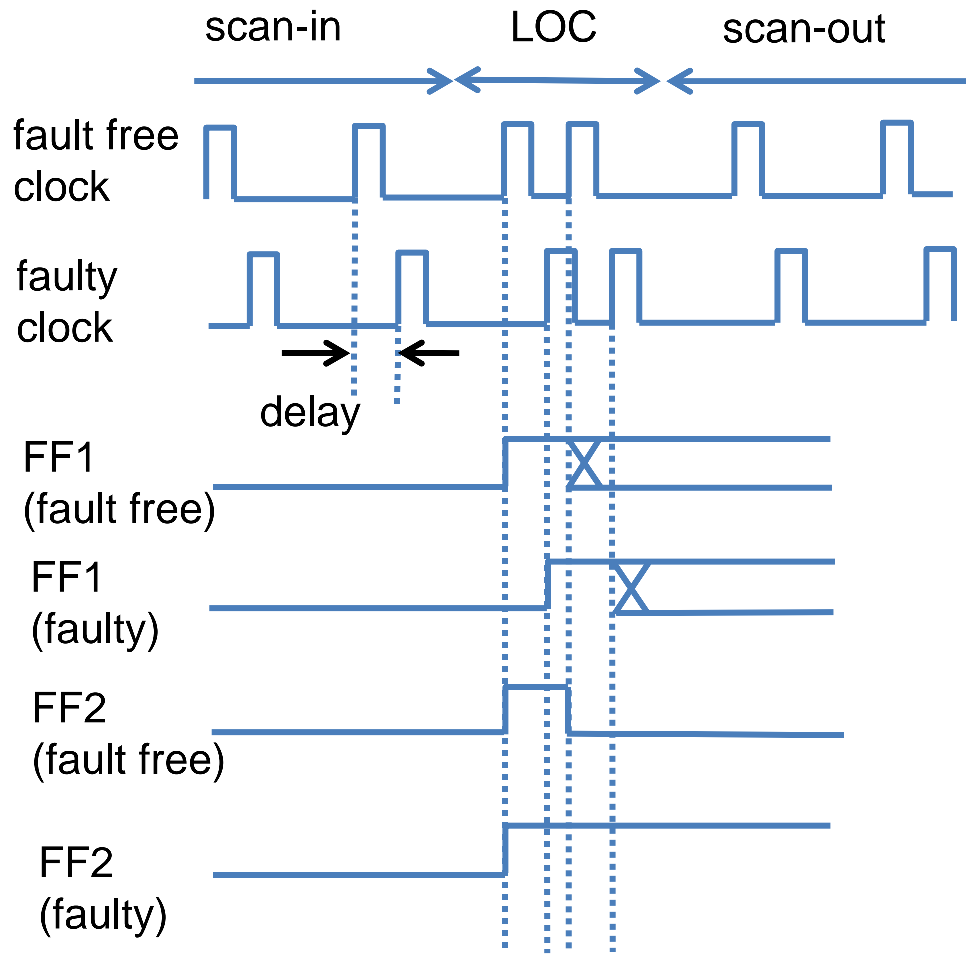
- Investigate effects of delay faults on clock lines
- Show fault simulation results
- Propose a test generation method
- Assumptions
  - Launch-on-capture test is applied.
  - One or two FFs are affected.
  - The delay faults affect FFs during the system clock cycle

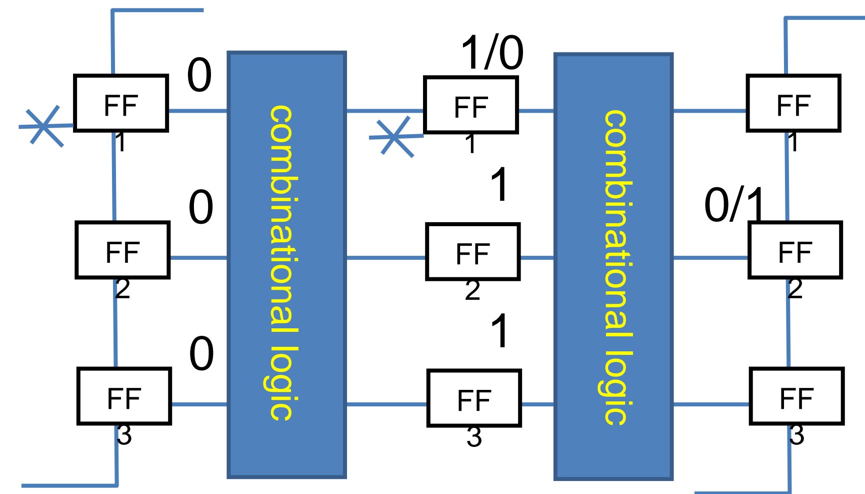
Clock tree

- Clock signals are distributed by the clock tree.
- We consider the case in which one or two FFs are affected.
- The case in which many FF FFs are affected is easy to test.



Launch-on-capture (LOC) test





Clock delay fault model

- In the scan-shift mode, faulty FFs capture correct values.
- In the LOC mode, scan-in values are launched because faulty FFs fail to capture the functional value.

Fault simulation

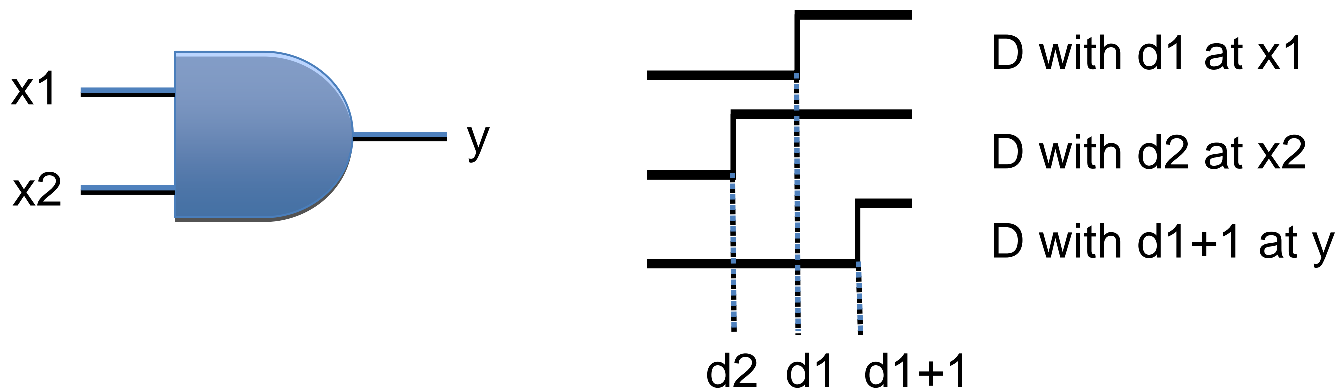
- The relation between the amount of delay and the fault detection is investigated.
- Seven logic values are used. [Takahashi, ATS '95]
  - D (0 -> 1)
  - $\overline{D}$ (1 -> 0)
  - B (0 -> 1 propagated from the fault site)
  - $\overline{B}$ (1 -> 0 propagated from the fault site)

AND operation using 7 logic values

	0	1	D	$\overline{D}$	B	$\overline{B}$	X
0	0	0	0	0	0	0	0
1	0	1	D	$\overline{D}$	B	$\overline{B}$	X
D	0	D	D	0	D	0	X
$\overline{D}$	0	$\overline{D}$	$\overline{D}$	$\overline{D}$	$\overline{D}$	$\overline{B}$	X
B	0	B	B	0	B	0	X
$\overline{B}$	0	$\overline{B}$	$\overline{B}$	$\overline{D}$	$\overline{B}$	$\overline{B}$	X
X	0	X	X	X	X	X	X

Fault simulation

- Latest transition time is calculated.
- Unit-delay is assumed at every gate.



Latest transition time on AND gate

	0	1	D	$\overline{D}$	B	$\overline{B}$	X
0	0	0	0	0	0	0	0
1	0	0	d2+1	d2+1	d2+1	d2+1	0
D	0	d1+1	d1+1	0	d1+1	0	0
$\overline{D}$	0	d1+1	d1+1	d2+1	d1+1	d2+1	0
B	0	d1+1	d1+1	0	d1+1	0	0
$\overline{B}$	0	d1+1	d1+1	d2+1	d1+1	d2+1	0
X	0	0	0	0	0	0	0

d1 is later than d2

Results on FF-186 in s13207

- Experiment for s13207
- Test vectors generated for gate-transition-faults were applied.
- The amount of clock delay was varied.
- One FF (FF-186) was affected.
- System clock cycle was set to 60.
- The number of detecting test vectors was investigated.

delay	38	39	40	41	42	43	44	45	46	47	48	49
vectors	1	2	6	8	9	10	12	14	18	22	27	41

- ◆Minimum delay was 38.
- ◆Maximum delay was 49.

Delay and the number of detected faults in s13207

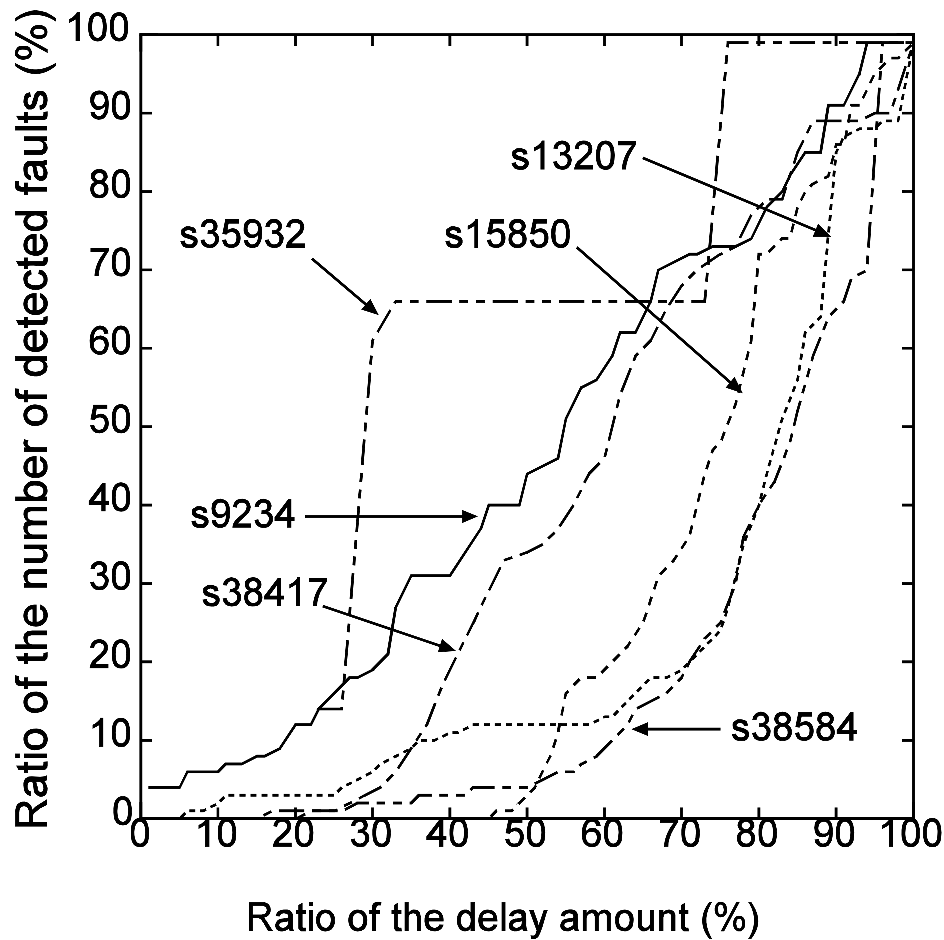
delay	1-5	6-10	11-15	16-20	21-25	26-30	31-35	36-40	41-45	46-50	51-55	56-60
min	9	8	1	23	16	3	1	28	27	134	174	37
max	0	0	0	3	12	5	4	23	4	132	209	88
median	0	0	9	15	13	7	8	18	20	145	188	57

"minimum delay" means the amount of delay such that a target fault is detected by at least one test vector.

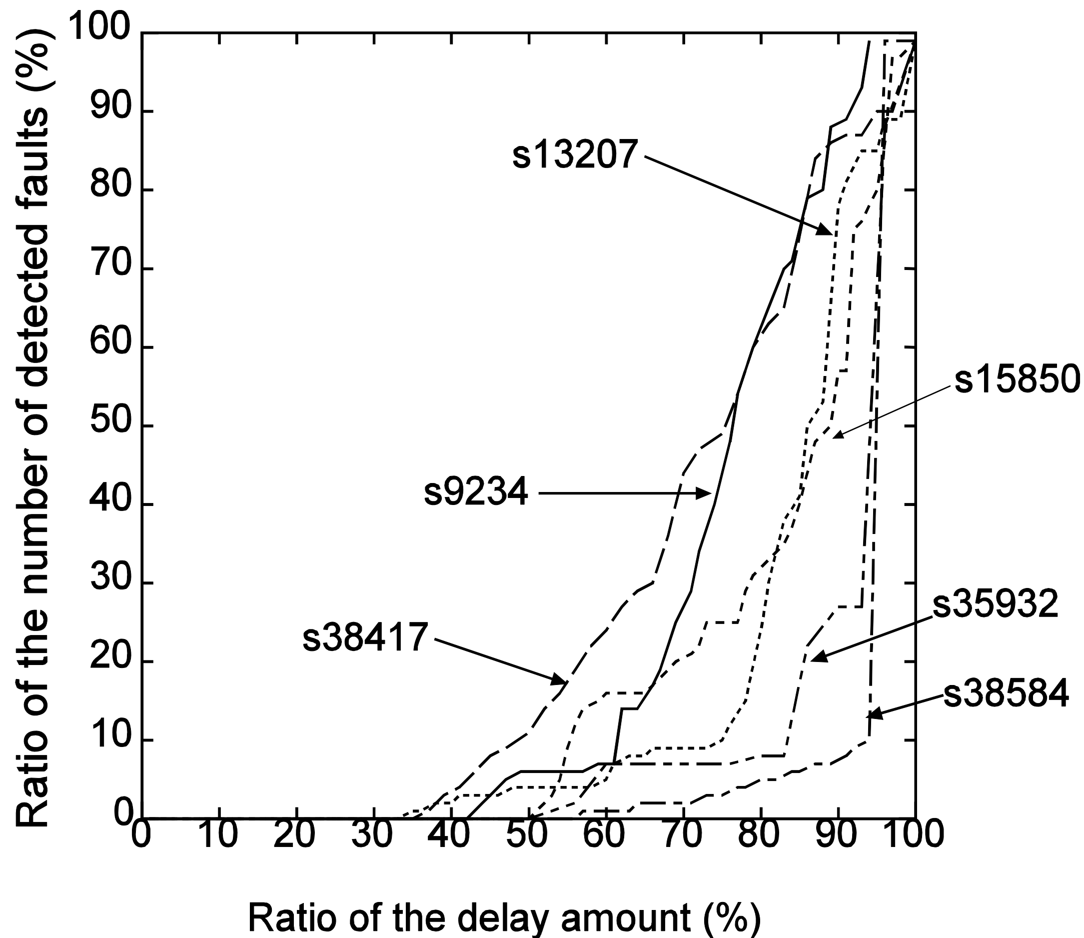
Ex) There are 9 faults whose minimum delay was 1 to 5.

"maximum delay" means the amount of delay such that a target fault is detected by all the detecting test vectors.

Results on minimum delay



Results on maximum delay

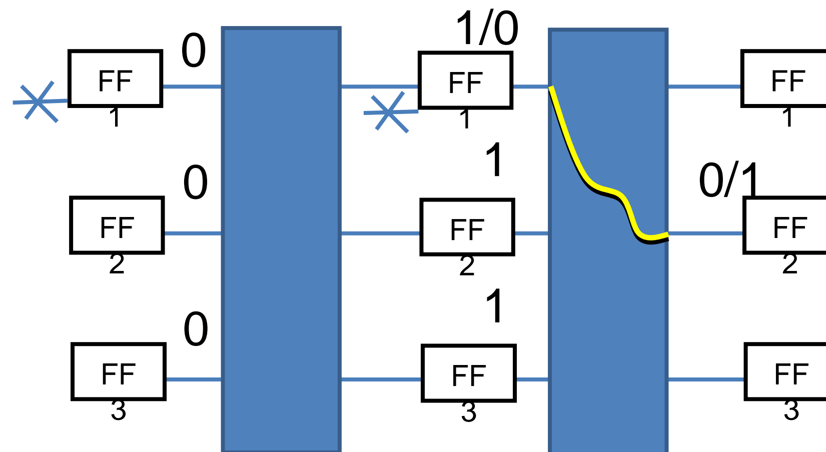


Test generation for clock delay

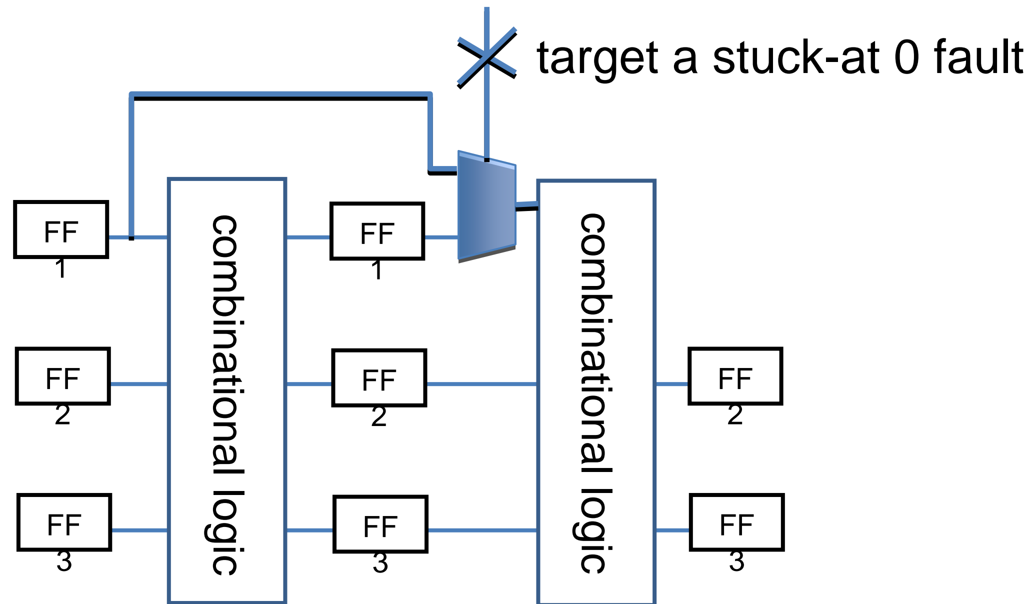
- Two cases are considered
  - The case of a single FF affected by a clock delay
  - The case of two FFs affected by a clock delay
- Approach
  - Use of a standard stuck-at ATPG tool
  - Some extra gates are added during the ATPG process

A single FF affected by a clock delay

- Conditions for detecting such a clock delay
  - The scan-in value is different from the functional one at the faulty FF
  - One sensitized path exists from the faulty FF to another FF or a PO in the LOC mode



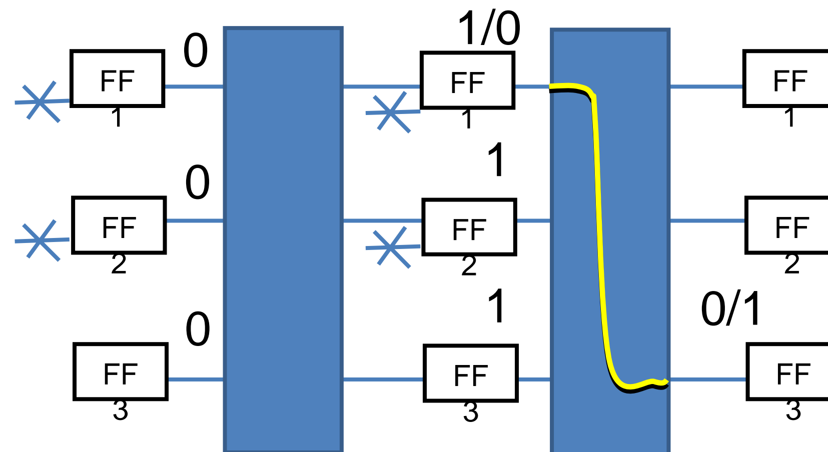
Circuit modification



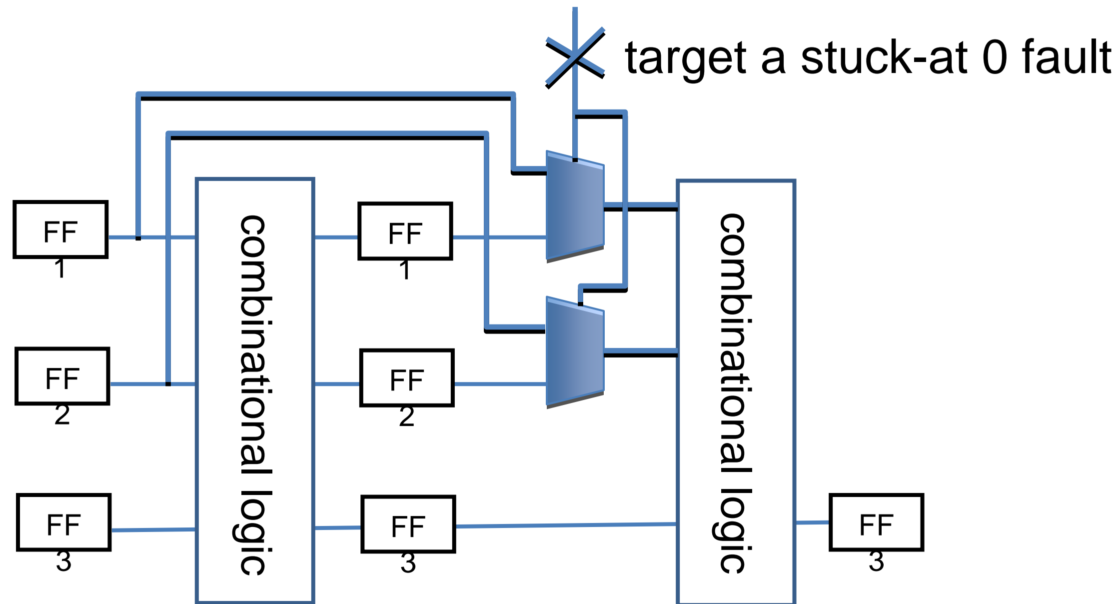
- FF1 is affected by a clock delay fault.
- The conditions for detecting a clock delay is converted into those for a stuck-at fault.

Two FFs affected by a clock delay

- Conditions for detecting such a clock delay
  - The scan-in value is different from the functional one at either one or both of the faulty FFs
  - One sensitized path exists from either one faulty FF to another FF or a PO in the LOC mode



Circuit modification



- FF1 and FF2 are affected by a clock delay fault.
- The conditions for detecting a clock delay is converted into those for a stuck-at fault.

Results for the case of a single affected FF

circuit	target	detect1	detect2	redun-dant	effi-ciency	vector1	vector2	CPU(s)
s9234	224	146	17	61	100	194	16	5.7
s13207	663	481	69	113	100	127	42	11.3
s15850	588	429	36	123	100	144	23	33
s35932	1728	1728	0	0	100	54	0	0.4
s38417	1627	1466	156	5	100	139	119	2203
s38584	1451	1388	8	55	100	258	8	9.9

detect1: the number of faults detected by transition test vectors
detect2: the number of faults detected by the proposed test generation
vector1: the number of test vectors for gate transition faults
vector2: the number of test vectors generated by the proposed method

Results for the case of two affected FFs

circuit	target	detect1	detect2	redun-dant	effi-ciency	vector1	vector2	CPU(s)
s9234	1000	865	55	80	100	194	16	434
s13207	1000	922	45	33	100	127	21	503
s15850	1000	934	32	34	100	144	20	1258
s35932	1000	1000	0	0	100	54	0	0.25
s38417	1000	993	7	0	100	139	7	91.1
s38584	1000	999	0	1	100	258	0	2.4

detect1: the number of faults detected by transition test vectors
detect2: the number of faults detected by the proposed test generation
vector1: the number of test vectors for gate transition faults
vector2: the number of test vectors generated by the proposed method

Conclusion

- Investigate the effects of clock delay faults
- Show fault simulation results
- Propose a test generation method
- Future works
  - propose a diagnosis method
  - investigate the effects of clock delay faults on detection of other faults