Compression-Aware Capture Power Reduction for At-Speed Testing

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Test Power Problems

Test Power

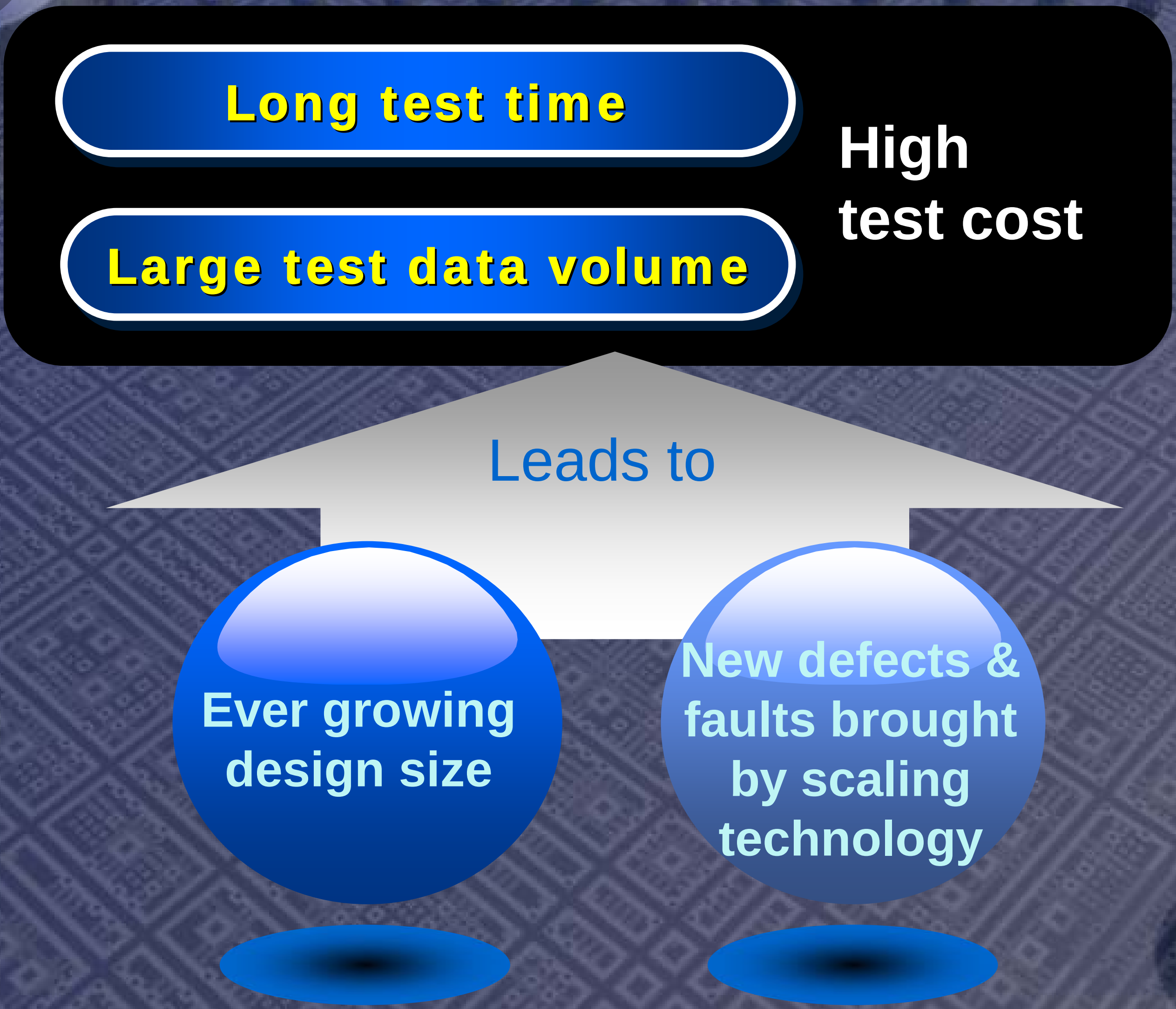
Shift Power:

Duration: long
Clock: scan
Impact: thermal
Solution: DFT-based

Capture Power:

Duration: short
Clock: scan/functional
Impact: yield
Solution: Vector-based

Test Compression Becomes Mandatory



Long test time

Large test data volume

High test cost

Leads to

Ever growing design size

New defects & faults brought by scaling technology

Test Compression Techniques

Test compression techniques

Nonlinear code-based

- Efficiently exploit the correlation among specific bits
- No ATPG constraints

Linear decompression-based

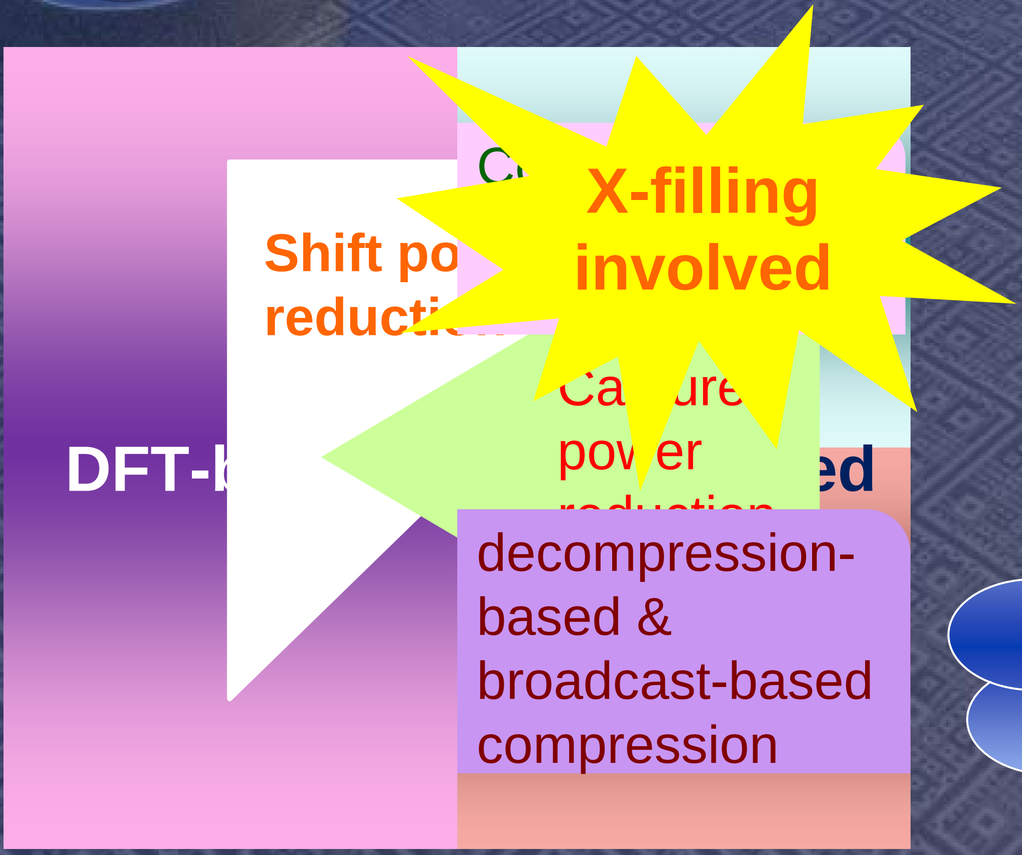
- High test compression ratio
- Integrated into ATPG

Broadcast-based

- High test compression ratio
- Strict ATPG constraints

Approach: Utilize X-bits in test vectors

Impact of X-filling



Objective:
Solve the contradiction caused by X-filling->

Reduce capture power for code-based test compression in at-speed scan testing

Contents

Code-based Test Data Compression

- **Fixed-symbol-length Schemes**
  - Test cubes segmented into fixed-length symbols
  - Dictionary-based, Selective Encoding…
- **Variable-symbol-length Schemes**
  - Test cubes segmented into variable-length symbols
  - Run-length-based, VIHC, …
- **Test Compression Ratio (TCR)**
  - Related to **entropy*** of the test cubes to be encoded:

*The minimum average number of bits required for each code-word

$$H = -\sum_{i=1}^{n} p_i \times \log p_i$$

p_i: the probability of occurrence of symbol x_i in the test cubes

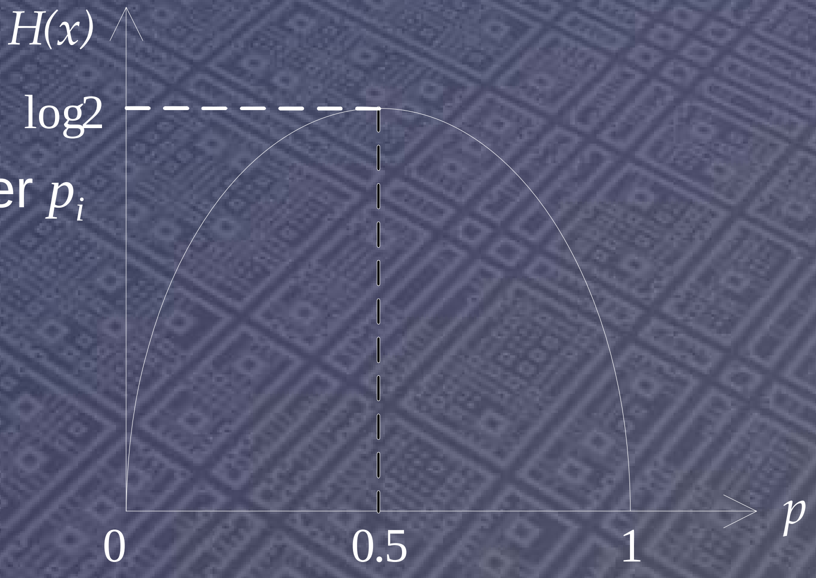
n: the total number of unique symbols

$$H \uparrow, TCR \downarrow$$

Improve *TCR* by X-filling

- **TCR ↑ → H ↓ → more skewed p_i distribution**
- **Fill X-bits to obtain:**
  - Fewer types of symbols
  - More code-words can be represented by symbols with higher p_i
- **Existing solution**
  - Fixed-symbol-length schemes: Alternative Fill [Balakrishnan07]
  - Variable-symbol-length schemes: still an open problem

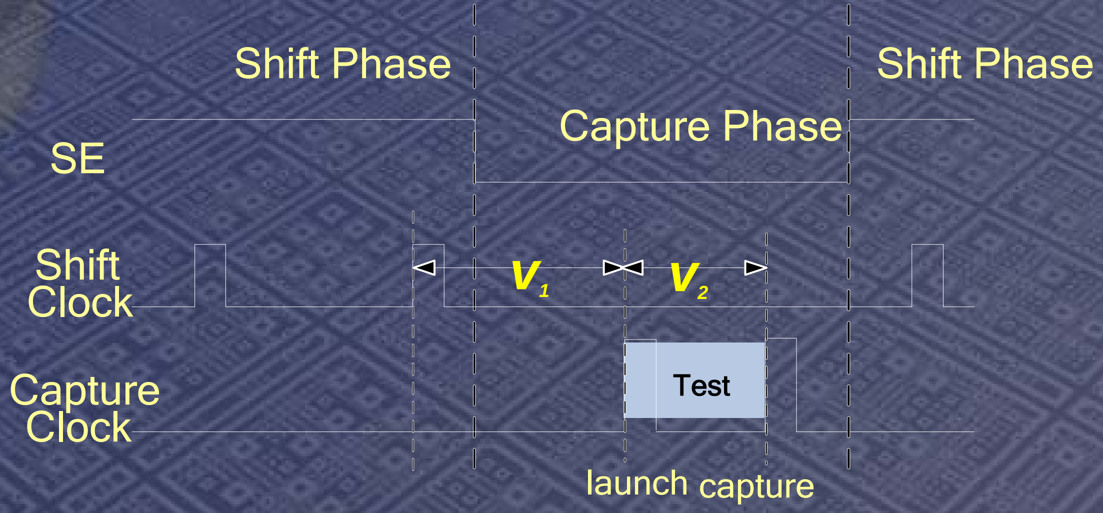
2 symbol example:



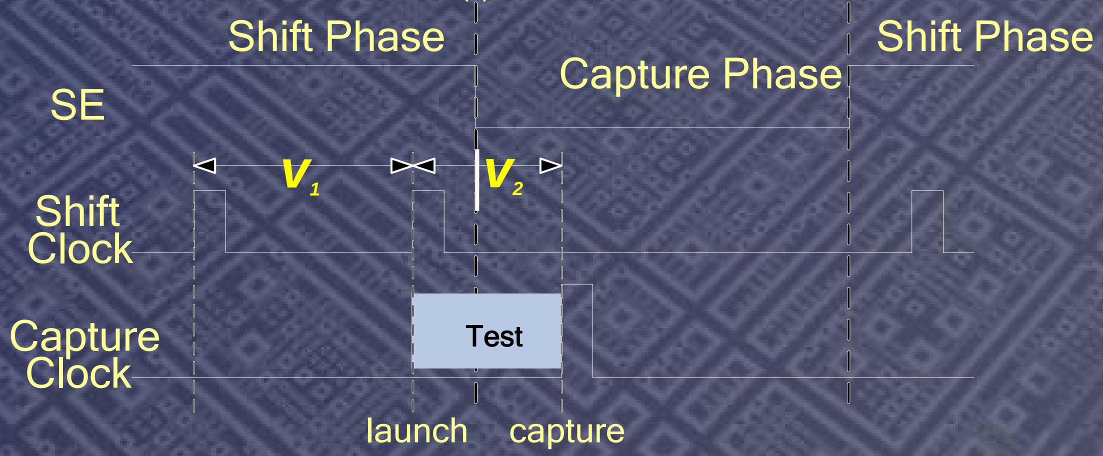
[Balakrishnan07] K. J. Balakrishnan and N. A. Touba. Relationship Between Entropy and Test Data Compression. *IEEE Transactions on Computer-Aided Design*, 26(2):386–395, Feb 2007.

Capture Power in At-speed Testing

(a) LoC Scheme



(b) LoS Scheme



Test Power Reduction with X-filling

- **Objective:**
  - Keep the capture power
  - in at-speed scan testing
  - under the safety limit
- **Approach:**
  - Selectively fill the X-bits
  - in certain order
  - to reduce Hamming distance between v_1 and v_2
  - so that the capture transition in the entire CUT can be reduced under the safety limit

Problem Formulation

- X-filling can facilitate either test compression ratio enhancement or test power reduction, but not both.
  - Different objectives and approaches
  - →test sets with high TCR usually cause high capture power, or test sets with low capture power can not be compressed efficiently
- There is requirement to apply them simultaneously in at-speed testing
- Problem: Propose a compression-aware capture power reduction X-filling framework for at-speed scan testing

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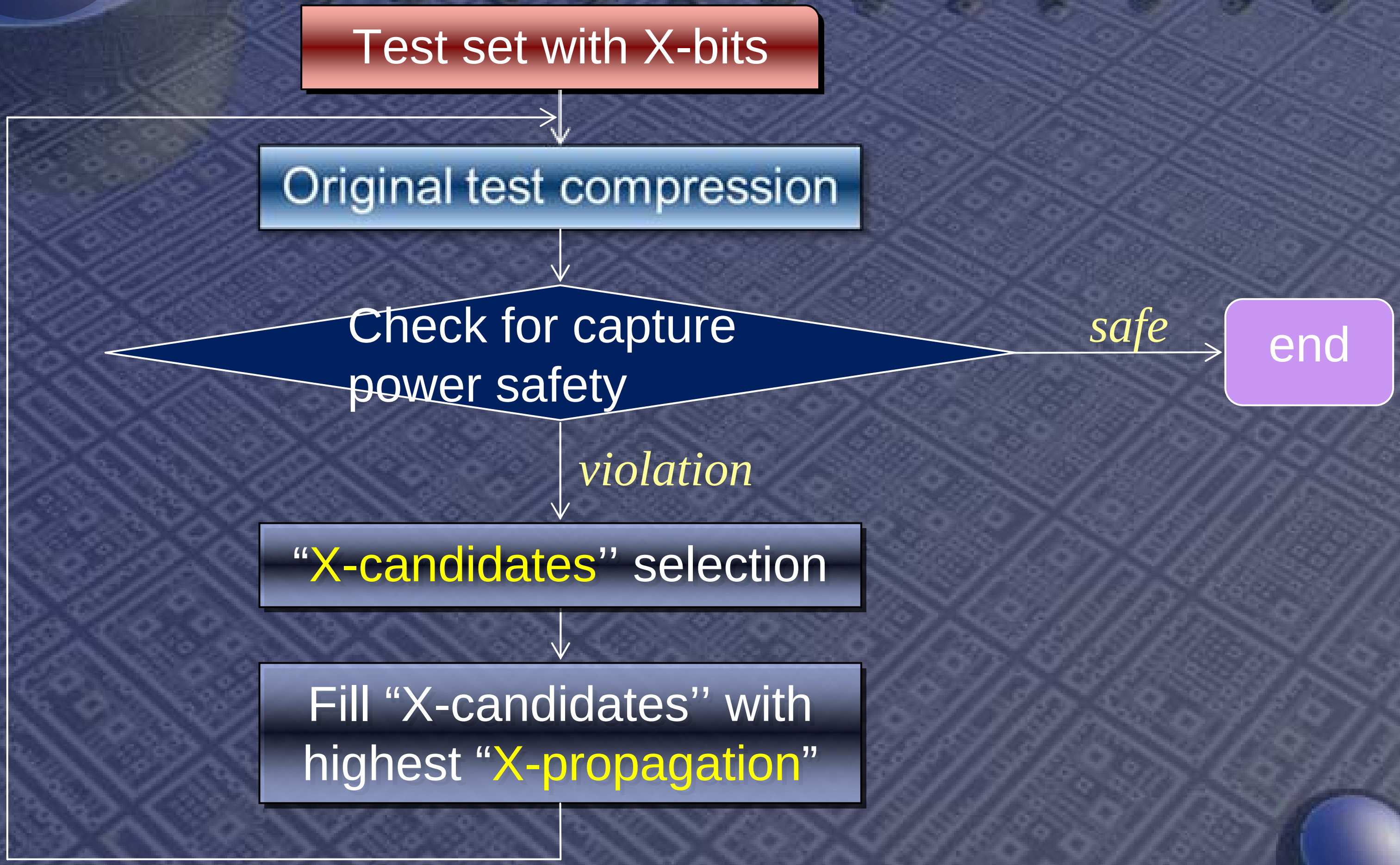
1. Introduction
2. Background
3. Proposed Framework
4. Experimental Results
5. Conclusion

Contributions highlight

- Prior works:
  - X-bits are usually selected and filled without considering their impact on test compression
  - Considered only LoC at-speed testing
  - Applicable to target special test compression scheme only
- Proposed work:
  - proposes to identify "*X-candidate*" that can be filled with low test compression ratio loss
  - proposed "*X-propagation*" metric to evaluate the impact of the X-bits on capture power of both LoC and LoS at-speed testing.
  - general applicability of the proposed framework in different X-filling and test compression strategies.

Overall flow



Test set with X-bits

Original test compression

Check for capture power safety

safe

end

violation

"X-candidates" selection

Fill "X-candidates" with highest "X-propagation"

“X-candidates” Selection (1)

In Fixed-symbol-length schemes

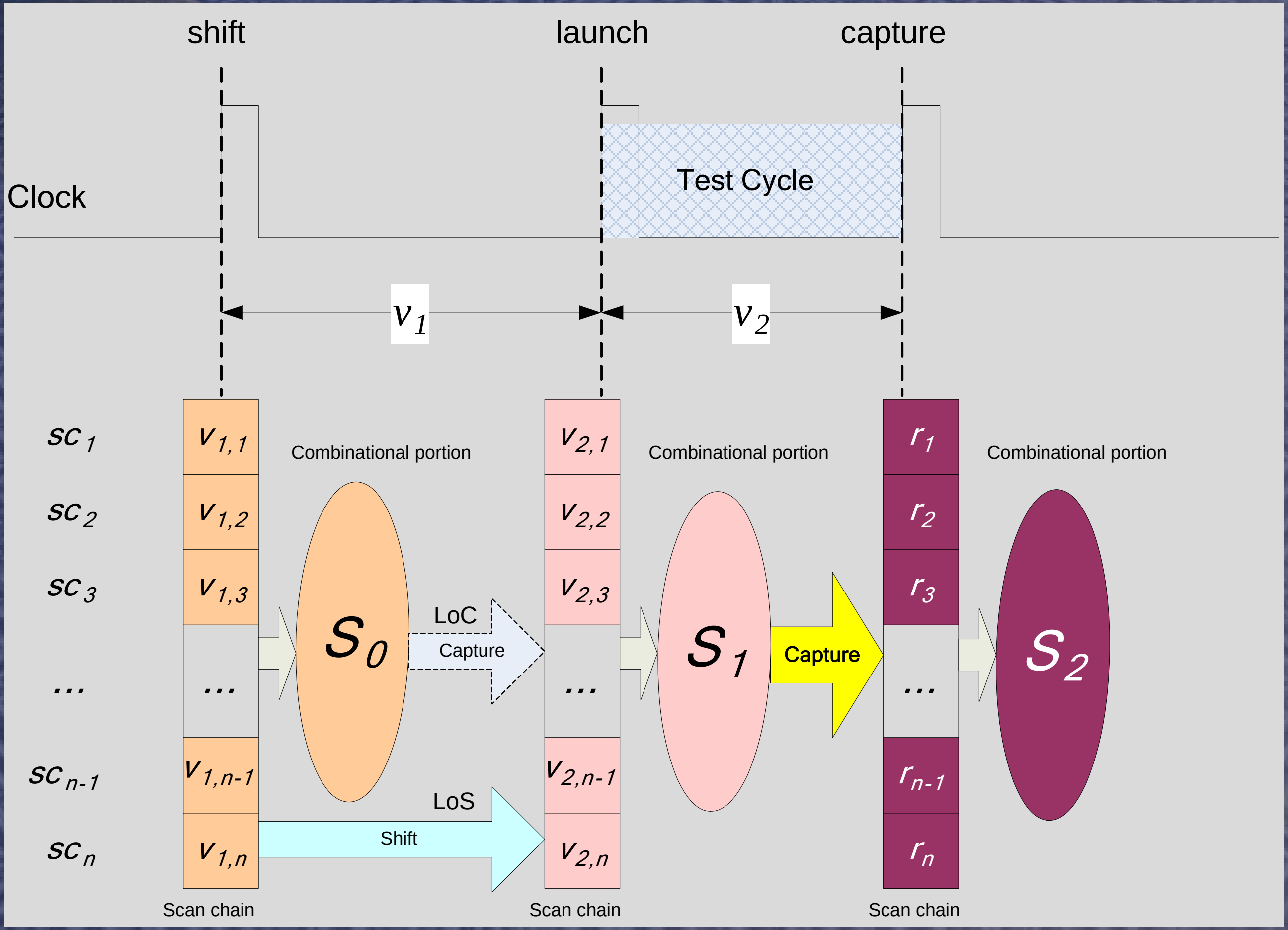
Vector1	111X	XX01	001X	X000	110X	011X
Vector2	X000	001X	X001	011X	01X0	X000
Vector3	X001	011X	011X	110X	110X	X000
Vector4	001X	X000	X000	01X0	110X	011X

- **Symbol set: {X000, 011X, 110X, 001X, X001, 01X0, 111X}**
  - X-bits in the representing symbols can be filled without affecting the distribution of the symbols
  - X-bits in the corresponding code-words are selected as “X-candidates”

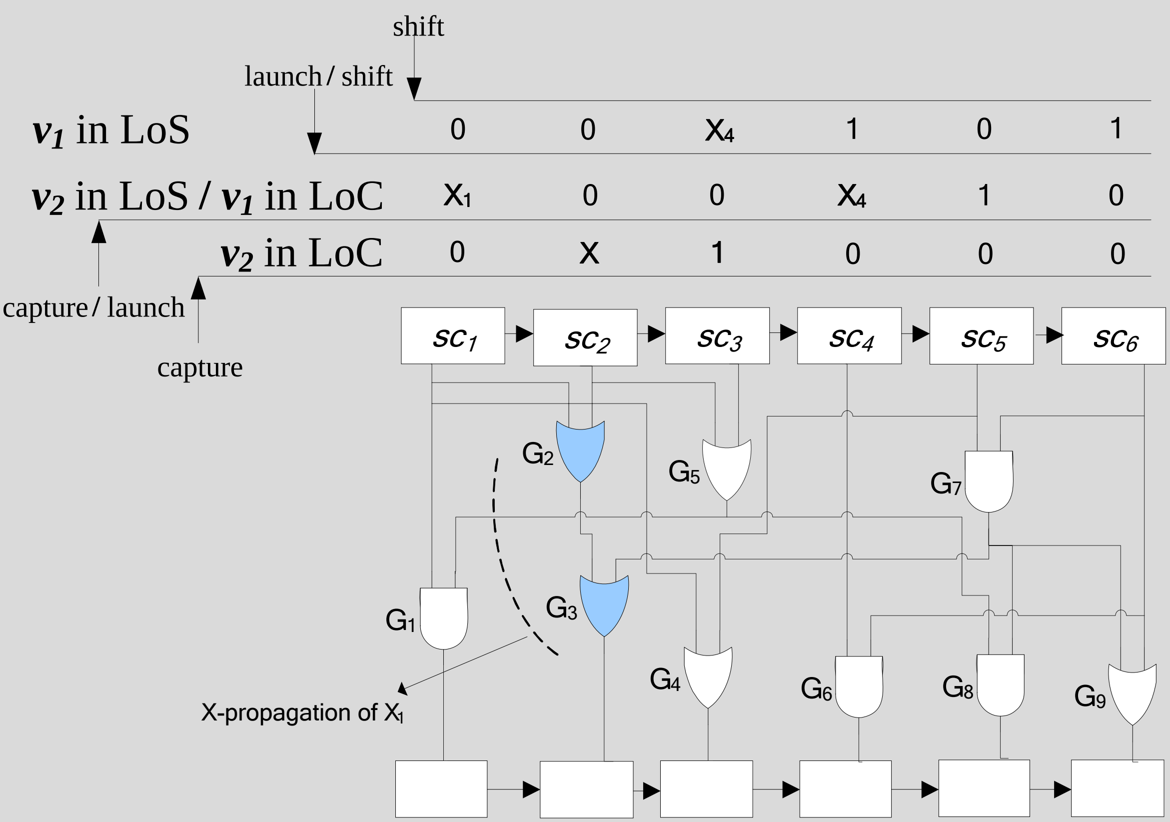
“X-candidates” Selection (2)

- **In Variable-symbol-length schemes**
  - Existing solutions fill the X-bits with logic value that will not break the run, e.g.,
  - 000X0X0X 001X10X1→00000000 00101001
  - Maximum run-length (L_{max}): 8
  - 4 code-words: 00000000, 001, 01, 001
  - Or: 00000001, 001, 01, 001
  - →the last bit in the code-word with the maximum run-length can be filled with 0 or 1.→chosen as “X-candidates”

Cause of capture power in at-speed scan testing: LoC/LoS scheme



“X-propagation” calculation



	sc_1	sc_2	sc_3	sc_4	sc_5	sc_6
v_1 in LoS	0	0	X_4	1	0	1
v_2 in LoS / v_1 in LoC	X_1	0	0	X_4	1	0
v_2 in LoC	0	X	1	0	0	0

$$P_i = \sum_{G_k \text{ driven by } X_i} \frac{1}{N_{X-\text{input}_k}}$$

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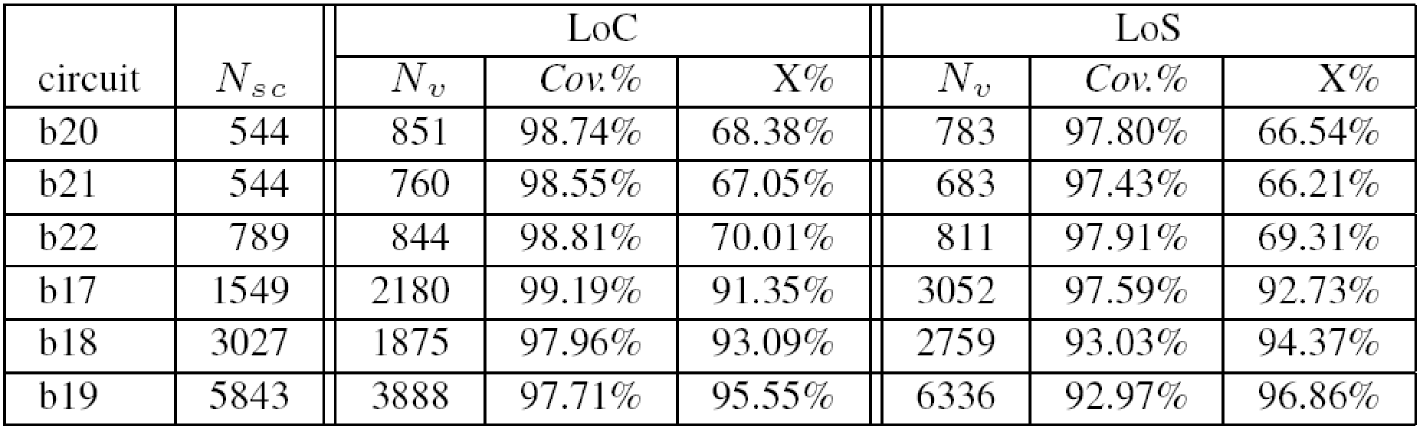
Experimental setting



circuit	N_{sc}	LoC			LoS		
		N_v	Cov.%	X%	N_v	Cov.%	X%
b20	544	851	98.74%	68.38%	783	97.80%	66.54%
b21	544	760	98.55%	67.05%	683	97.43%	66.21%
b22	789	844	98.81%	70.01%	811	97.91%	69.31%
b17	1549	2180	99.19%	91.35%	3052	97.59%	92.73%
b18	3027	1875	97.96%	93.09%	2759	93.03%	94.37%
b19	5843	3888	97.71%	95.55%	6336	92.97%	96.86%

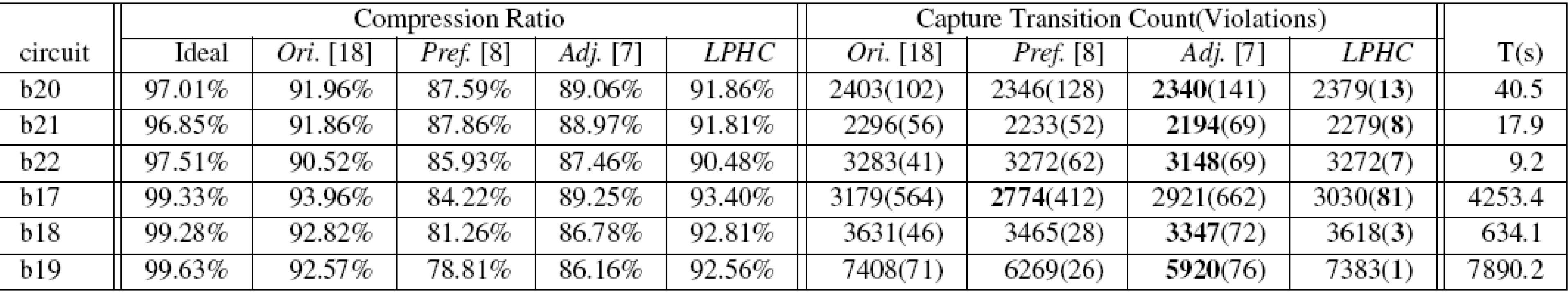
- **Test compression schemes:**
  - Fixed-symbol-length scheme: dictionary-based [Wurtenberger04]
  - Variable-symbol-length scheme: VIHC [Gonciari03]
- **At-speed scan testing schemes:**
  - LoC & LoS

[Wurtenberger04] A. Wurtenberger, C. S. Tautermann, and S. Hellebrand. Data Compression for Multiple Scan Chains using Dictionaries with Corrections. In *Proceedings IEEE International Test Conference (ITC)*, pages 926–935, October 2004.

[Gonciari03] P. T. Gonciari, B. M. Al-Hashimi, and N. Nicolici. Variable-length input Huffman coding fo system-on-a-chip test. *IEEE Transactions on Computer-Aided Design*, 22(6):783–796, June 2003.

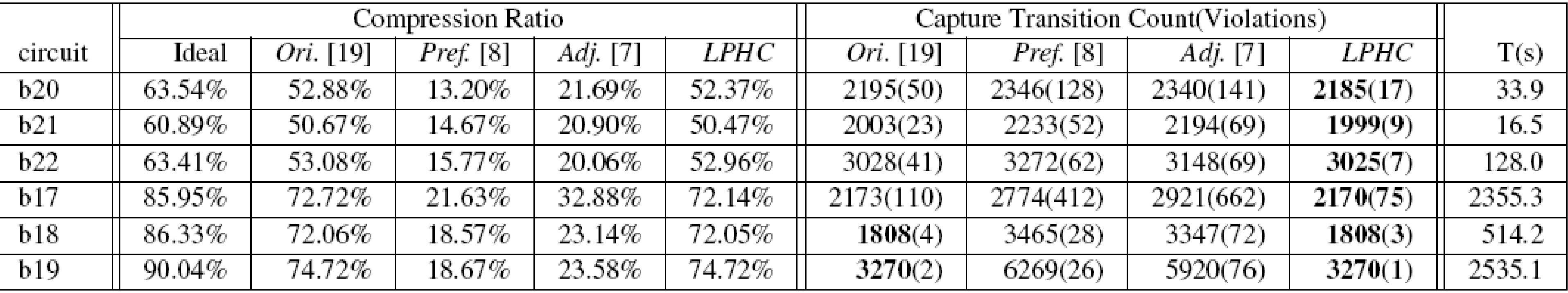
In LoC at-speed testing

- For dictionary-based test compression



circuit	Compression Ratio					Capture Transition Count(Violations)				T(s)
	Ideal	*Ori.* [18]	*Pref.* [8]	*Adj.* [7]	*LPHC*	*Ori.* [18]	*Pref.* [8]	*Adj.* [7]	*LPHC*	
b20	97.01%	91.96%	87.59%	89.06%	91.86%	2403(102)	2346(128)	**2340**(141)	2379(**13**)	40.5
b21	96.85%	91.86%	87.86%	88.97%	91.81%	2296(56)	2233(52)	**2194**(69)	2279(**8**)	17.9
b22	97.51%	90.52%	85.93%	87.46%	90.48%	3283(41)	3272(62)	**3148**(69)	3272(**7**)	9.2
b17	99.33%	93.96%	84.22%	89.25%	93.40%	3179(564)	**2774**(412)	2921(662)	3030(**81**)	4253.4
b18	99.28%	92.82%	81.26%	86.78%	92.81%	3631(46)	3465(28)	**3347**(72)	3618(**3**)	634.1
b19	99.63%	92.57%	78.81%	86.16%	92.56%	7408(71)	6269(26)	**5920**(76)	7383(**1**)	7890.2

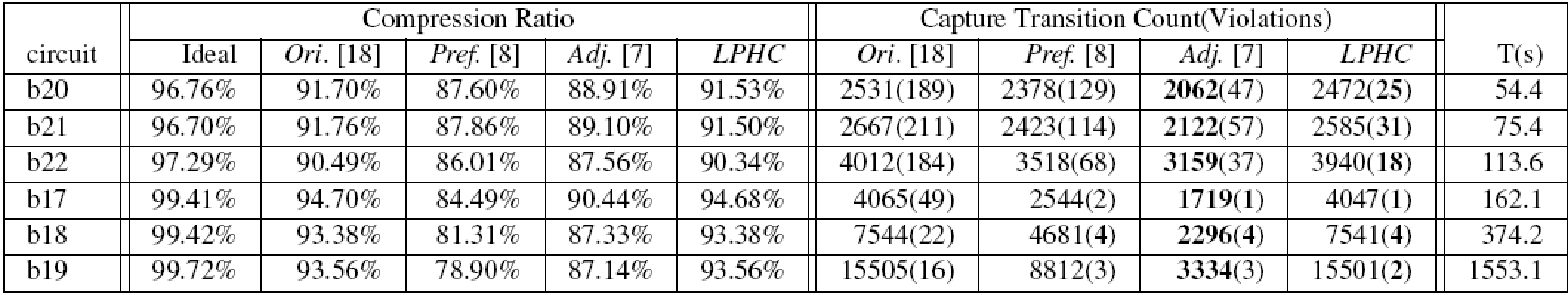
- For VIHC



circuit	Compression Ratio					Capture Transition Count(Violations)				T(s)
	Ideal	*Ori.* [19]	*Pref.* [8]	*Adj.* [7]	*LPHC*	*Ori.* [19]	*Pref.* [8]	*Adj.* [7]	*LPHC*	
b20	63.54%	52.88%	13.20%	21.69%	52.37%	2195(50)	2346(128)	2340(141)	**2185**(**17**)	33.9
b21	60.89%	50.67%	14.67%	20.90%	50.47%	2003(23)	2233(52)	2194(69)	**1999**(**9**)	16.5
b22	63.41%	53.08%	15.77%	20.06%	52.96%	3028(41)	3272(62)	3148(69)	**3025**(**7**)	128.0
b17	85.95%	72.72%	21.63%	32.88%	72.14%	2173(110)	2774(412)	2921(662)	**2170**(**75**)	2355.3
b18	86.33%	72.06%	18.57%	23.14%	72.05%	**1808**(4)	3465(28)	3347(72)	**1808**(**3**)	514.2
b19	90.04%	74.72%	18.67%	23.58%	74.72%	**3270**(2)	6269(26)	5920(76)	**3270**(**1**)	2535.1

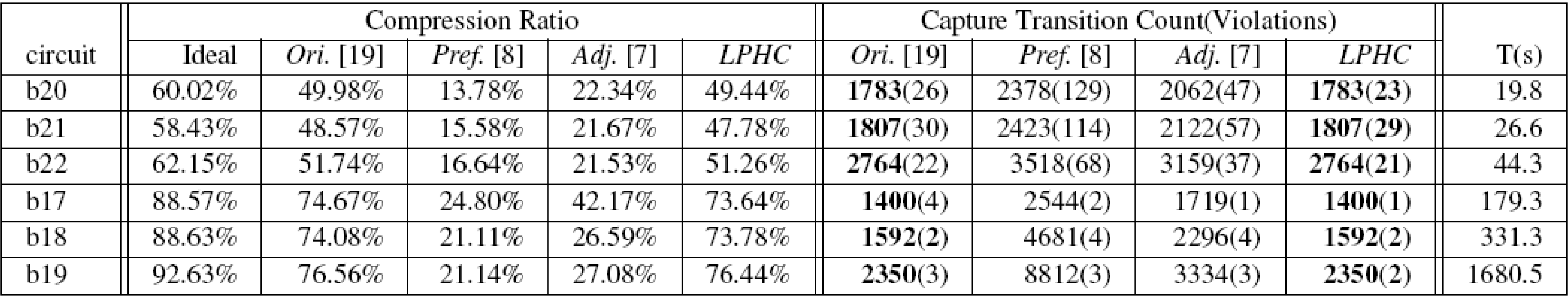
In LoS at-speed testing

❖ For dictionary-based test compression



circuit	Compression Ratio					Capture Transition Count(Violations)				T(s)
	Ideal	*Ori*. [18]	*Pref.* [8]	*Adj.* [7]	*LPHC*	*Ori*. [18]	*Pref.* [8]	*Adj.* [7]	*LPHC*	
b20	96.76%	91.70%	87.60%	88.91%	91.53%	2531(189)	2378(129)	**2062**(47)	2472(**25**)	54.4
b21	96.70%	91.76%	87.86%	89.10%	91.50%	2667(211)	2423(114)	**2122**(57)	2585(**31**)	75.4
b22	97.29%	90.49%	86.01%	87.56%	90.34%	4012(184)	3518(68)	**3159**(37)	3940(**18**)	113.6
b17	99.41%	94.70%	84.49%	90.44%	94.68%	4065(49)	2544(2)	**1719**(**1**)	4047(**1**)	162.1
b18	99.42%	93.38%	81.31%	87.33%	93.38%	7544(22)	4681(**4**)	**2296**(**4**)	7541(**4**)	374.2
b19	99.72%	93.56%	78.90%	87.14%	93.56%	15505(16)	8812(3)	**3334**(3)	15501(**2**)	1553.1

❖ For VIHC



circuit	Compression Ratio					Capture Transition Count(Violations)				T(s)
	Ideal	*Ori*. [19]	*Pref.* [8]	*Adj.* [7]	*LPHC*	*Ori*. [19]	*Pref.* [8]	*Adj.* [7]	*LPHC*	
b20	60.02%	49.98%	13.78%	22.34%	49.44%	**1783**(26)	2378(129)	2062(47)	**1783**(23)	19.8
b21	58.43%	48.57%	15.58%	21.67%	47.78%	**1807**(30)	2423(114)	2122(57)	**1807**(**29**)	26.6
b22	62.15%	51.74%	16.64%	21.53%	51.26%	**2764**(22)	3518(68)	3159(37)	**2764**(**21**)	44.3
b17	88.57%	74.67%	24.80%	42.17%	73.64%	**1400**(4)	2544(2)	1719(1)	**1400**(1)	179.3
b18	88.63%	74.08%	21.11%	26.59%	73.78%	**1592**(2)	4681(4)	2296(4)	**1592**(2)	331.3
b19	92.63%	76.56%	21.14%	27.08%	76.44%	**2350**(3)	8812(3)	3334(3)	**2350**(2)	1680.5

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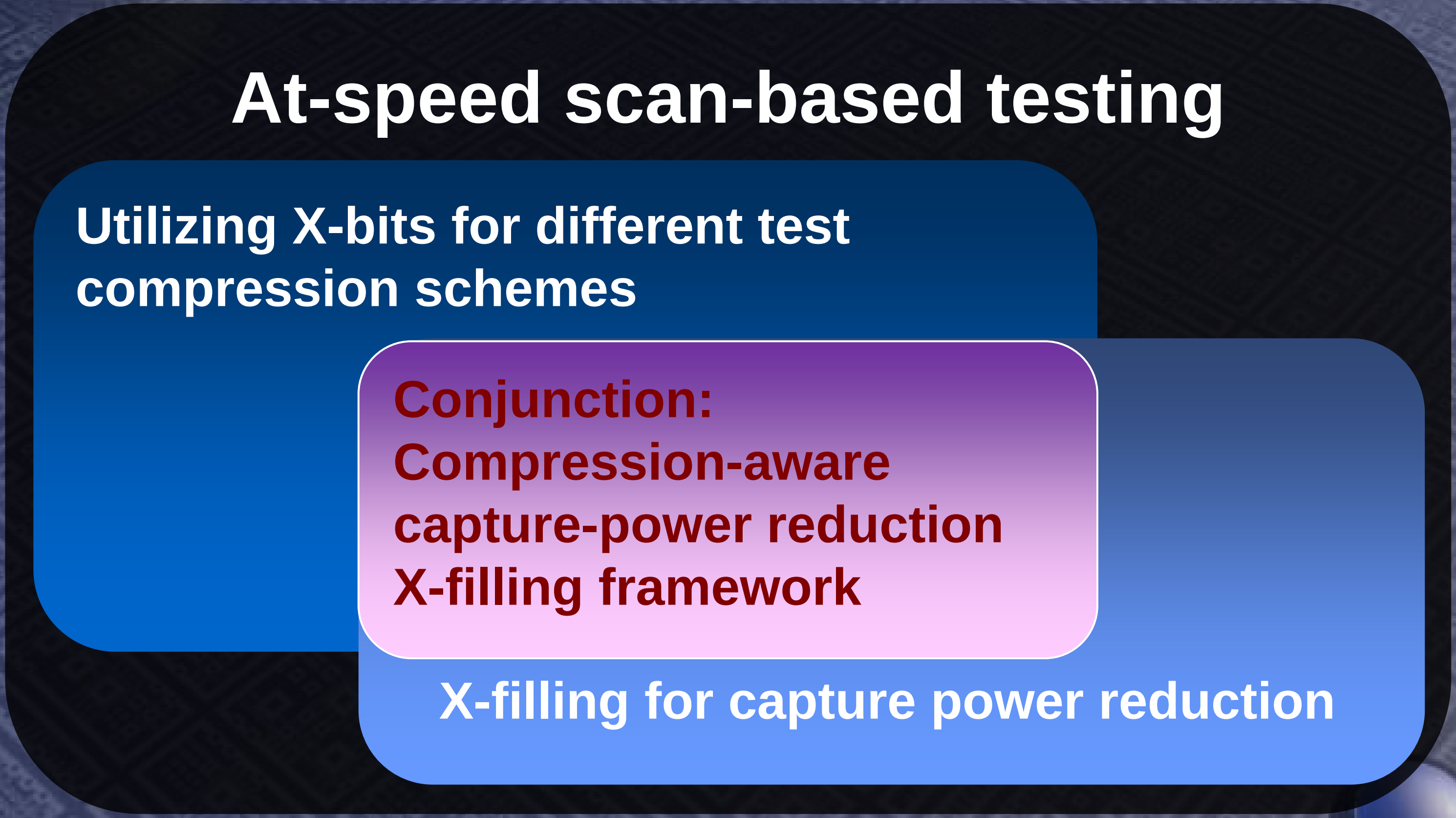
Conclusion



At-speed scan-based testing

Utilizing X-bits for different test compression schemes

Conjunction:
Compression-aware capture-power reduction X-filling framework

X-filling for capture power reduction

Thank You!
Questions/Comments?