# 16th Asia and South Pacific Design Automation Conference

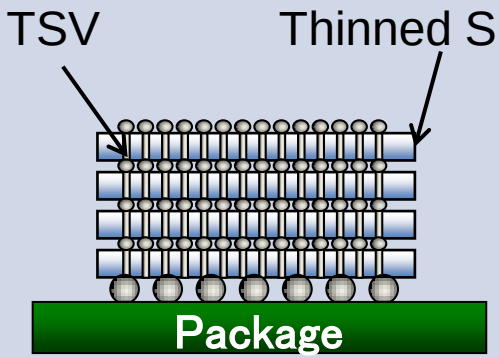
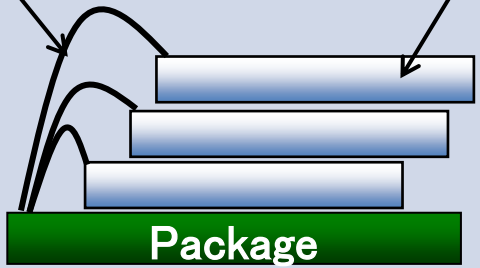
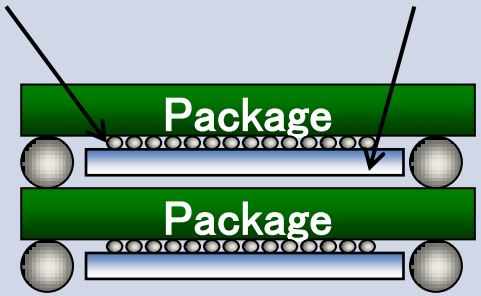
**Session 9D: Friday, January 28, 16:00-18:00 @ Room 416+417**
**Panel Discussion: Advanced packaging and 3D Technologies**

3D packaging is a key technology to satisfy a growing demand to realize highly integrated system and memory.
The panel session explores the technologies of three dimensional stacked chips and discusses the challenges to design and test of such integrated chips.

# Time table

| Plan | Contents | | Speaker |
|---|---|---|---|
| 5 min | Introductory talk | - Basic 3D integraion | Moderator |
| 15 min | Position talk | -3D technology<br>-Situation in Europe | Dr. Plas<br>Imec |
| 15 min | Position talk | -3D technology<br>-Situation in Asia | Dr. Ezawa<br>Toshiba |
| 15 min | Position talk | -3D technology<br>-Situation in U.S.A | Dr. Orii<br>IBM |
| 15 min | Position talk | -Package technology for 3D integration | Dr. Hiruta<br>J-DEVICES |
| 15 min | Position talk | -EDA technology for 3D integration | Dr. Cheung<br>Cadence |
| 35min | Discussion | | All |
| 5 min | Summary | | Moderator |

# 3D vertical integration

| TSV (Through-Silicon-Via) | Wire bond | PoP (Package-on-Package) |
|---|---|---|
|  |  |  |







## ◆ Benefits

- Small size / High density
- High bandwidth
- Heterogeneous-chip combination
- Low power
- Short time to market

## ◆ Applications

- DRAM, Flash, FPGA
- CPU + Memory
- Sensor + DSP

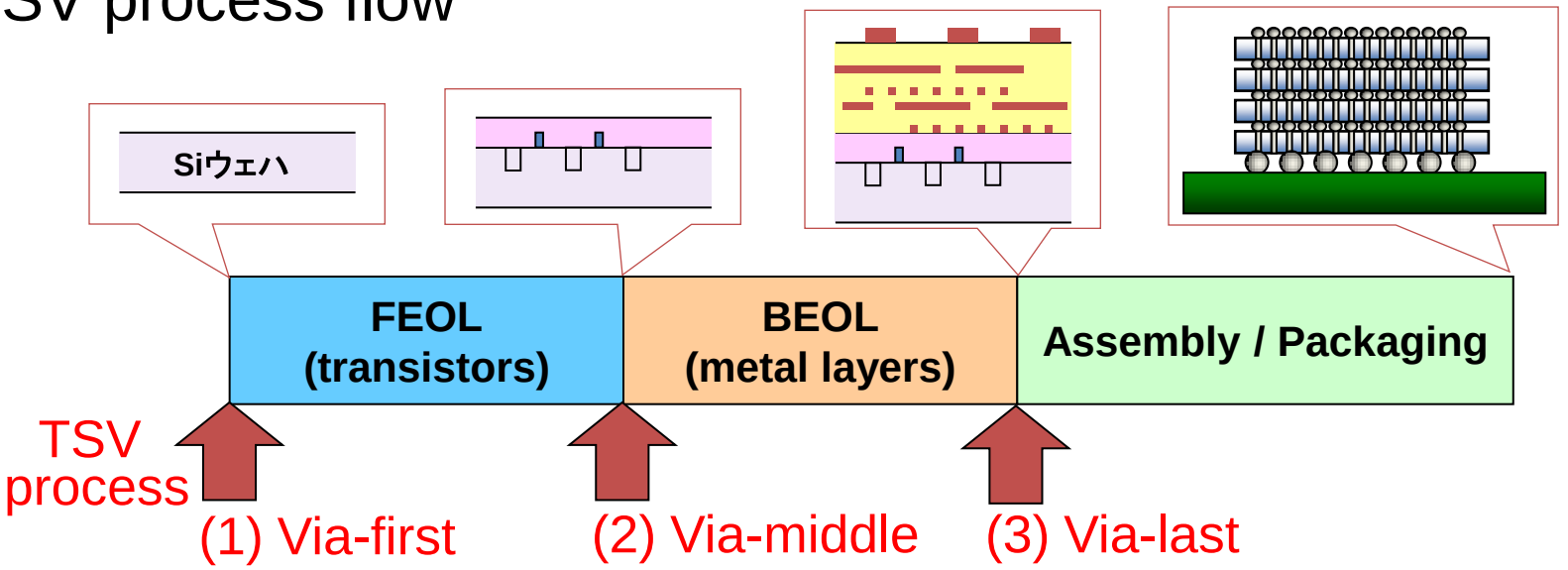
Questions

Where the market is for 3D ICs with TSVs?

When the 3D-TSV production starts on a large scale ?

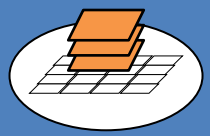
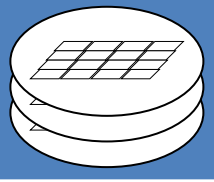
# 3D integration process options using TSV

◆ TSV process flow



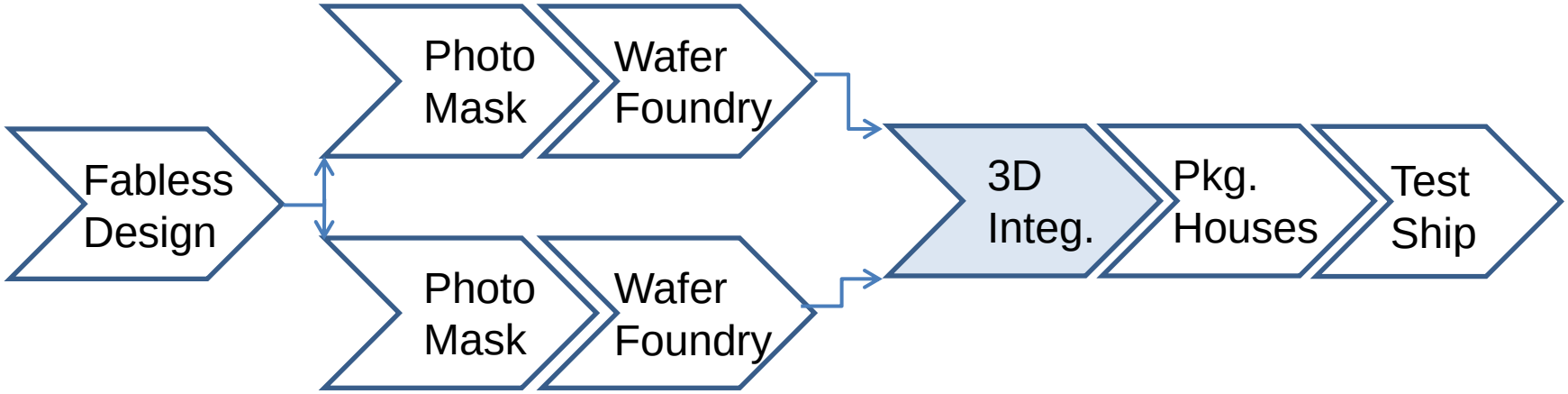

◆ TSV interconnect methods

KGD: known good die

| | (1) C2C: chip-to-chip  | (2) C2W: chip-to-wafer  | (3) W2W: wafer-to-wafer  |
|---|---|---|---|
| Pros | Flexible<br>Use of KGD | Flexible<br>Use of KGD | High throughput |
| Cons | Handling, Bonding | Handling, Bonding | Same chip size, Yield |

# Supply chain for 3D integration

◆ 3D IC integration process needs various expertise techniques.
=> To make 3D ICs widely used, new supply chain infrastructure must be built.




Example of supply chain for heterogeneous chips using wafer-to-wafer stacking

◆ Supply chain depends on
- TSV process flow, (via first, middle, last)
- Interconnect methods (wafer to wafer, wafer to chip, chip to chip)

◆ Supply chain needs EDA and test

Question
Who leads the supply chain to be built for 3D TSV production?
IDM(Integrated Device Manufacturer)? foundry? packaging house?
OSAT(Outsourced Semiconductor Assembly and Test)? EDA vender?

# 3D-INTEGRATION: STATUS, CHALLENGES AND OPPORTUNITIES

**Geert Van der Plas, Paul Marchal**

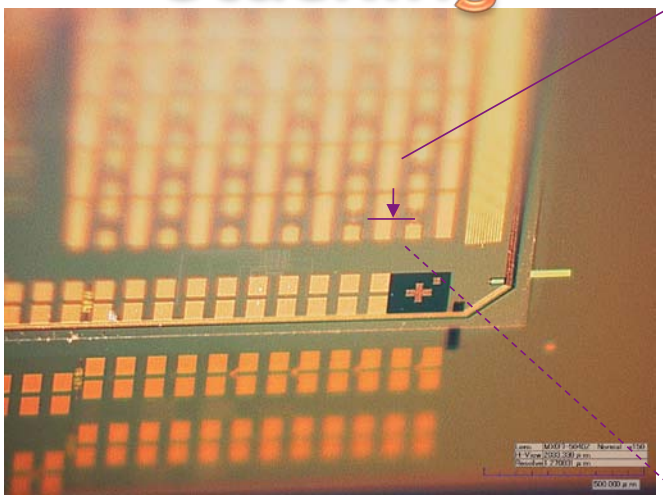
**3D Program IMEC**

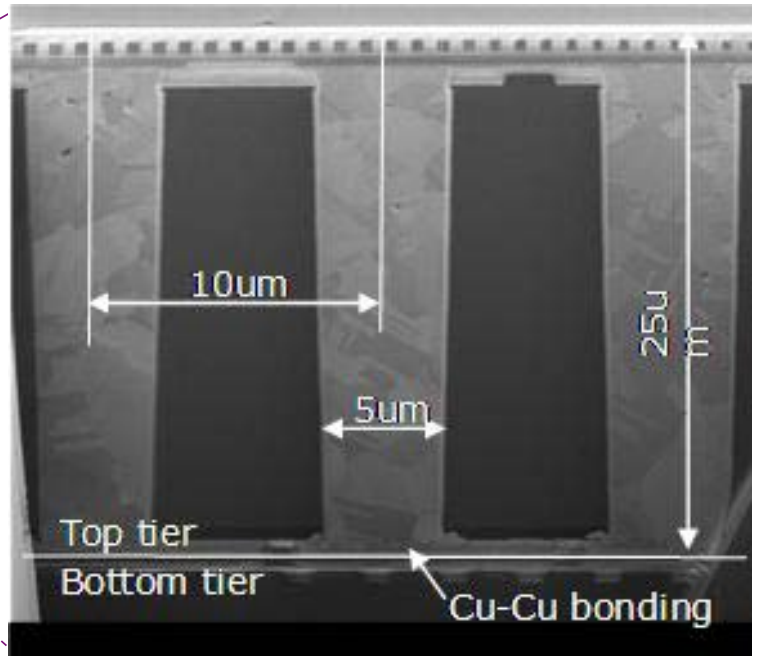
**IMEC, Kapeldreef 75, B-3001, Leuven, Belgium**

# TECHNOLOGY STAUTS: 3D'S COMING SOON

TSV

Stacking





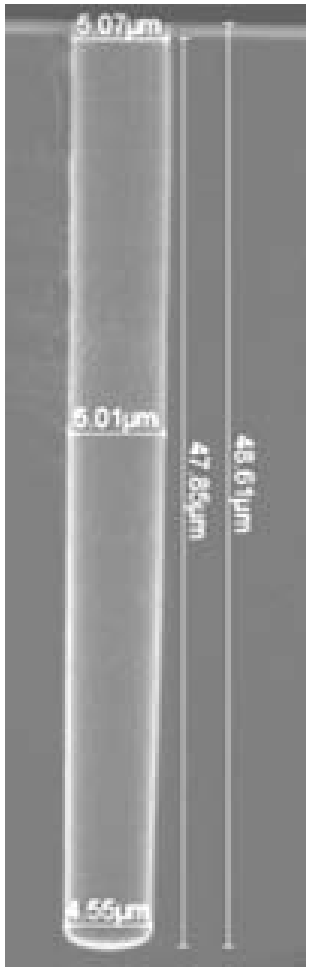

## Key features

- TSV Via middle
- CuSn & CuCu bonding

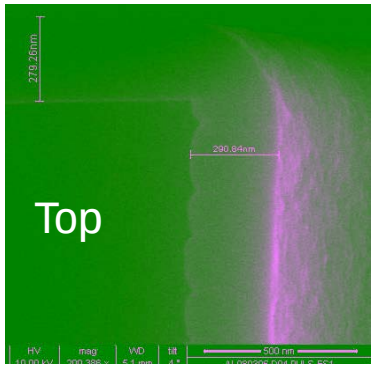
| | CuCu | CuSn |
|---|---|---|
| Wafer Ø | 200mm | 300mm |
| Cu TSV Ø Si Via | 5µm | 5µm |
| Height | 25µm | 50µm |
| TSV pitch | 10µm | 40µm → 20µm |

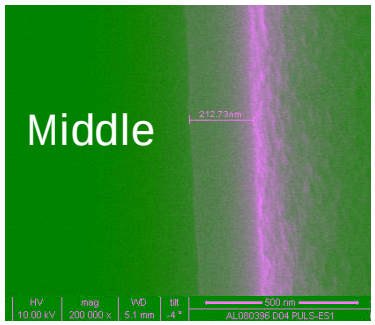
# HIGH ASPECT RATIO TSVS on 300mm

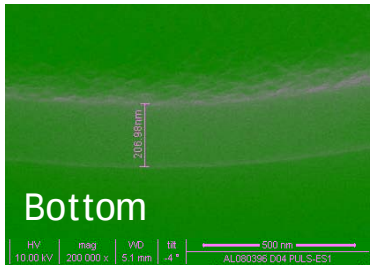
**via etch**



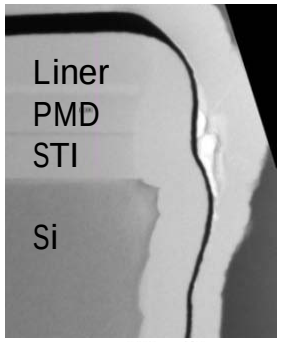

**oxide liner**

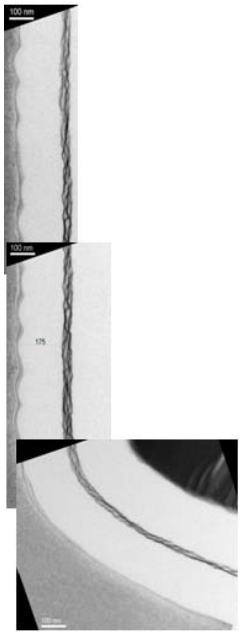


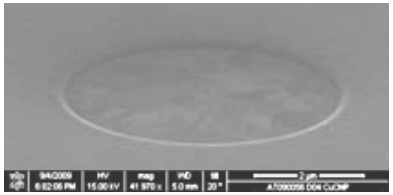

**barrier seed**



**Cu ECD Fill**

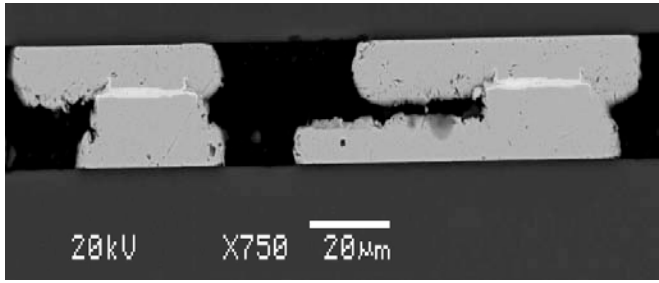

**TSV anneal & CMP**

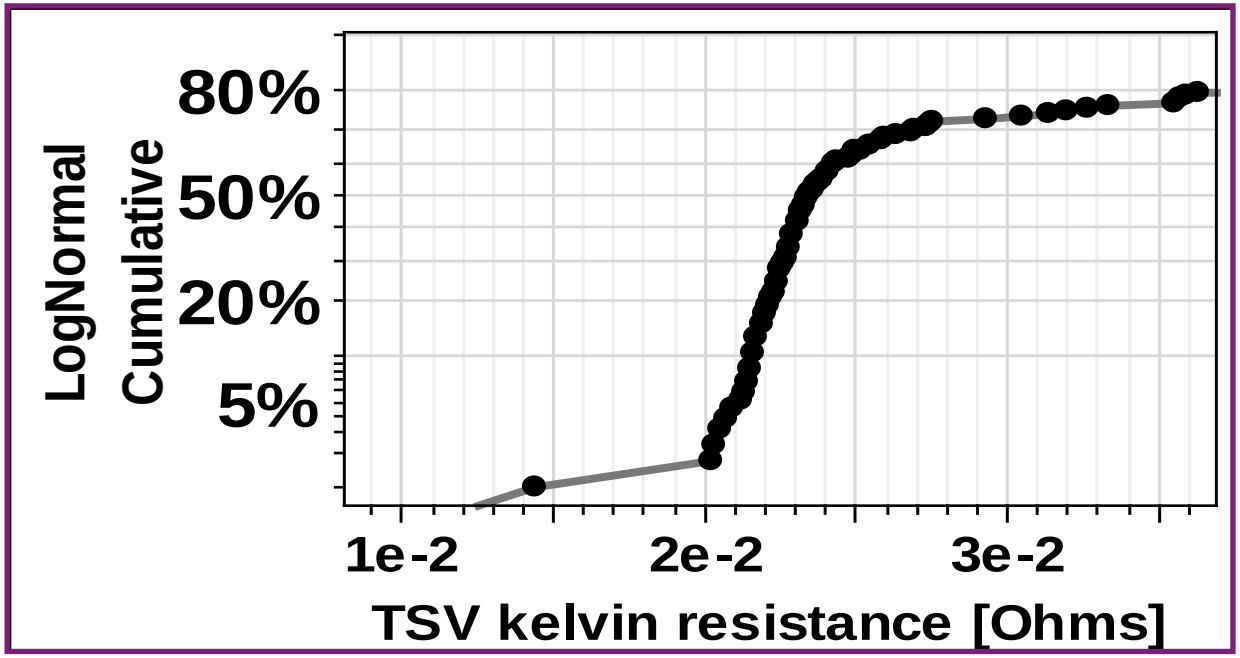


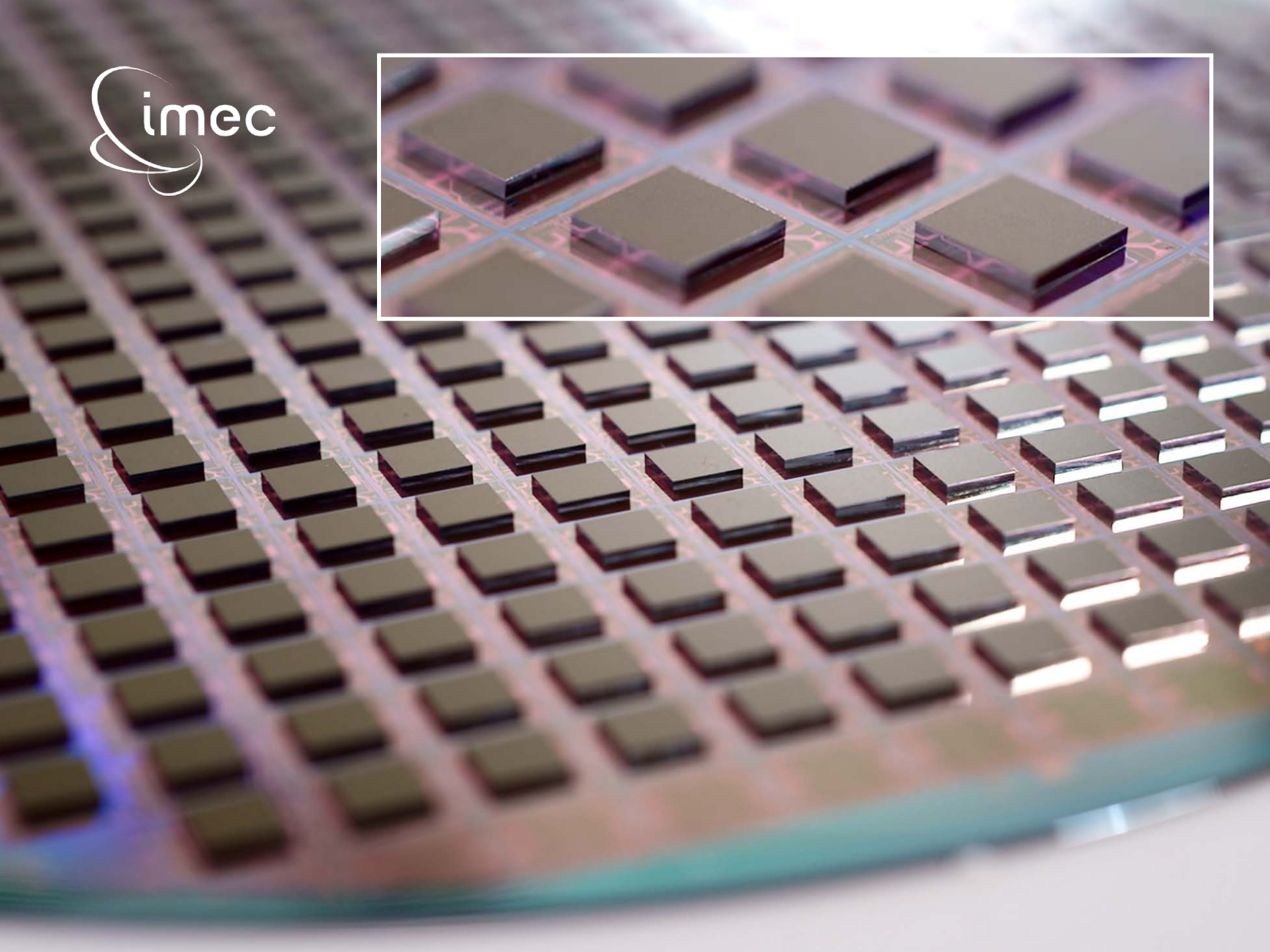
# 3D STACKING APPROACHES

**Die-to-wafer bonding approach: "fast" and accurate pick-and-place step, followed by collective bonding.**

- Process of Record: Cu/Sn
  - Scaling : 40→20µm
  - Cu/Sn Transient-Liquid-Phase, TLP, (250° C)
  - Diffusion bonding (150° C)


imec

# CHALLENGES & OPPORTUNITIES ?

# ELECTRICAL, THERMAL & THERMO-MECHANICAL CHALLENGES FOR 3D INTEGRATION

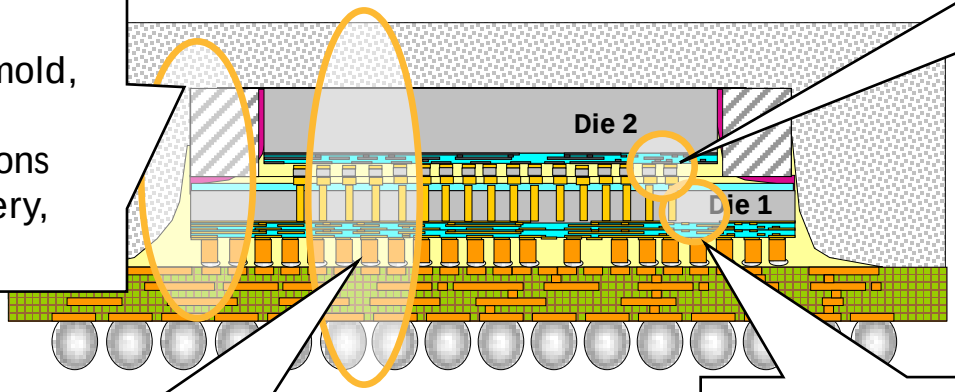
Reliability

**Impact of Flip Chip Package on 3D chip-stack (CPI)**
- Stress induced by Cu-pillars on low-K
- Stress induced by overmold, laminates CTE mismatch
- Thermal: cooling solutions
- Electrical: power delivery, EMI, …

CPI

**Heat dissipation & DRAM operation :**
Affected by packaging, mbump placement, underfill, …

Thermal

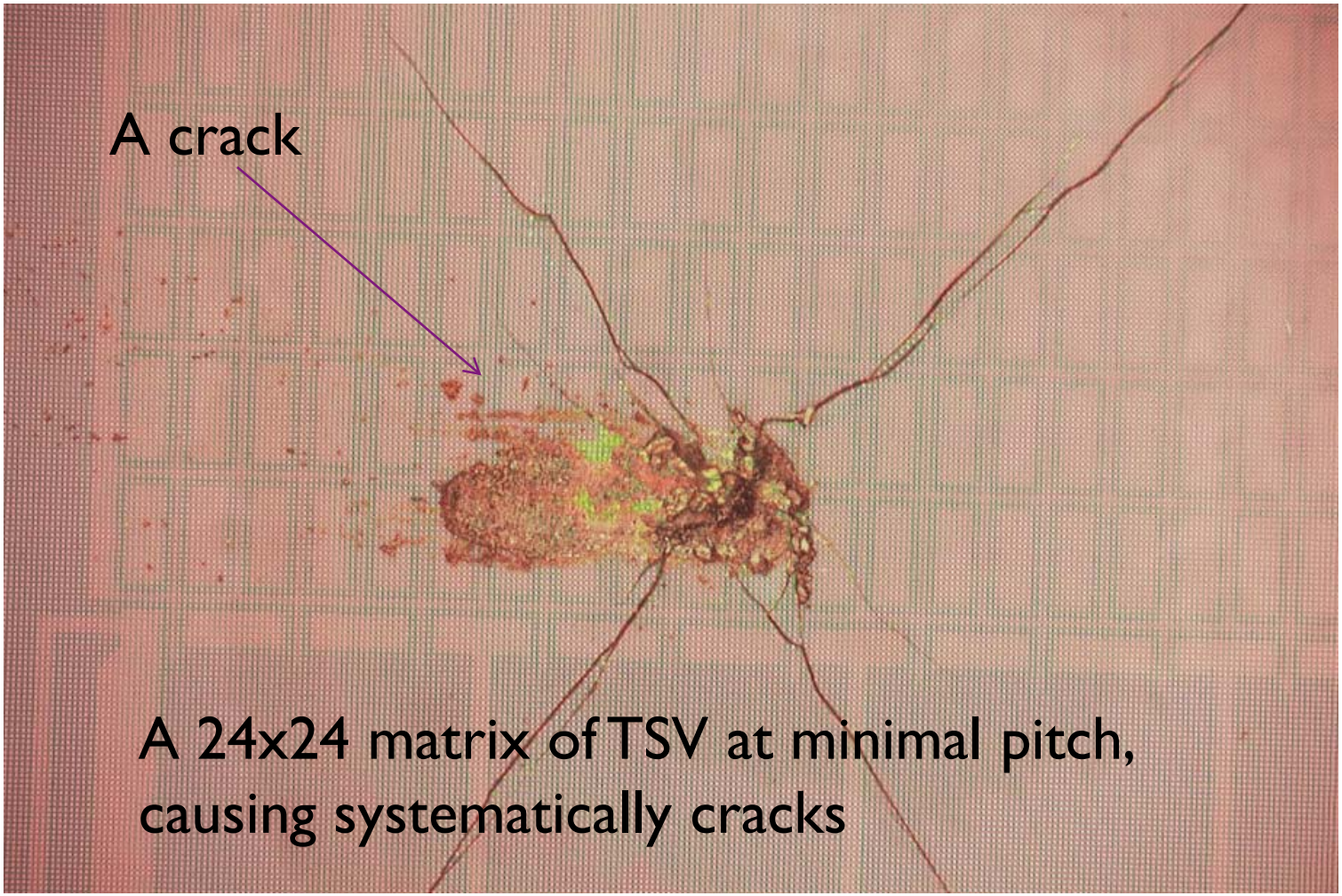



**3D Test**
- system testability
- KGD testing, physical probing

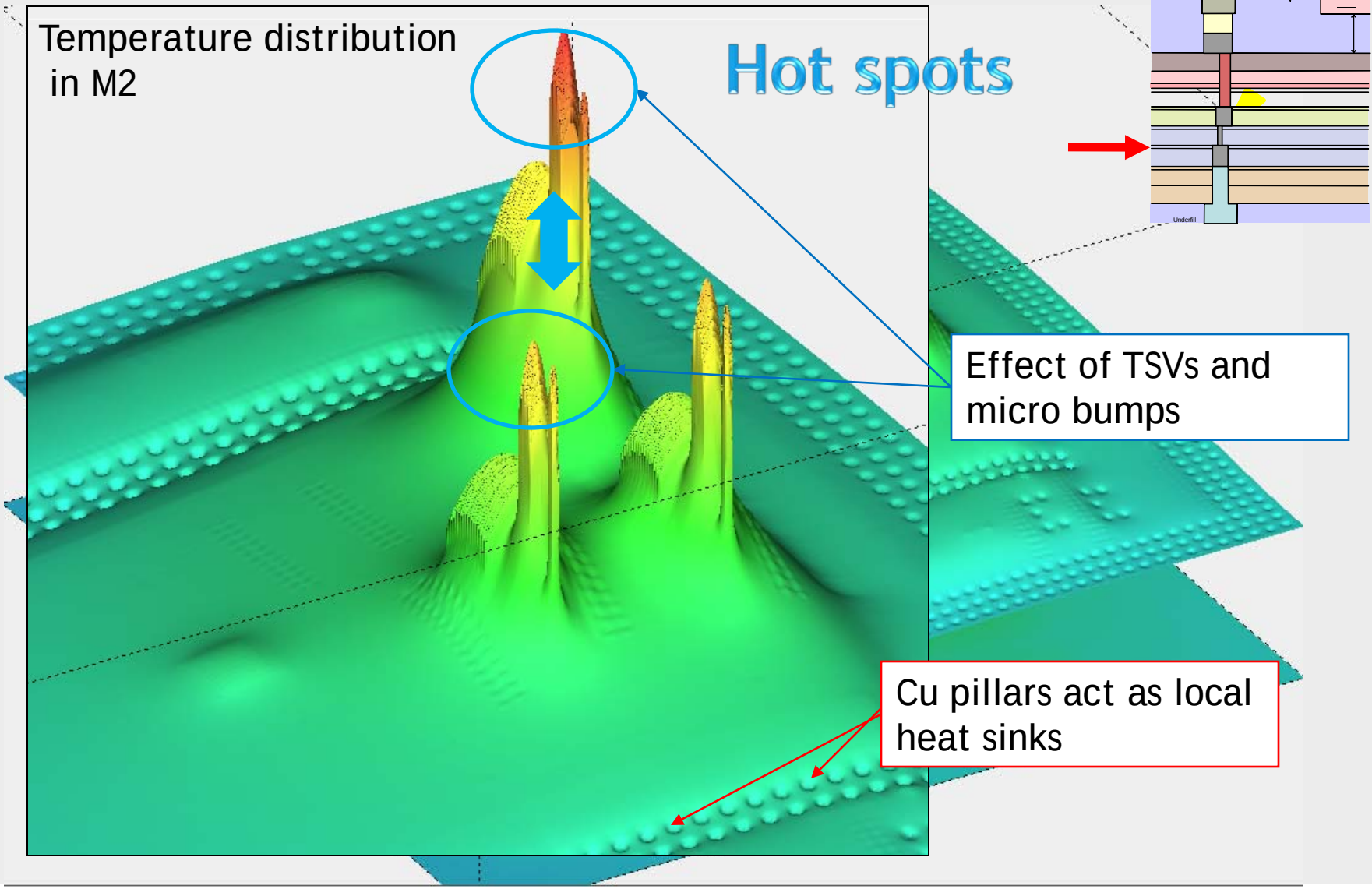
Test

**Impact of TSV on dies**
- Built-in stress
- Stress varies as function of temperature
- …

# TSV INDUCED STRESS – LIMITING RELIABILITY



# DRAM ON LOGIC: THERMAL SIMULATION RESULTS



# PATHFINDING FLOW: ELECTRICAL, MECHANICAL AND THERMAL AWARE HIGH-LEVEL DESIGN TOOL

PathFinding

Front Design
•Digital
•Analog

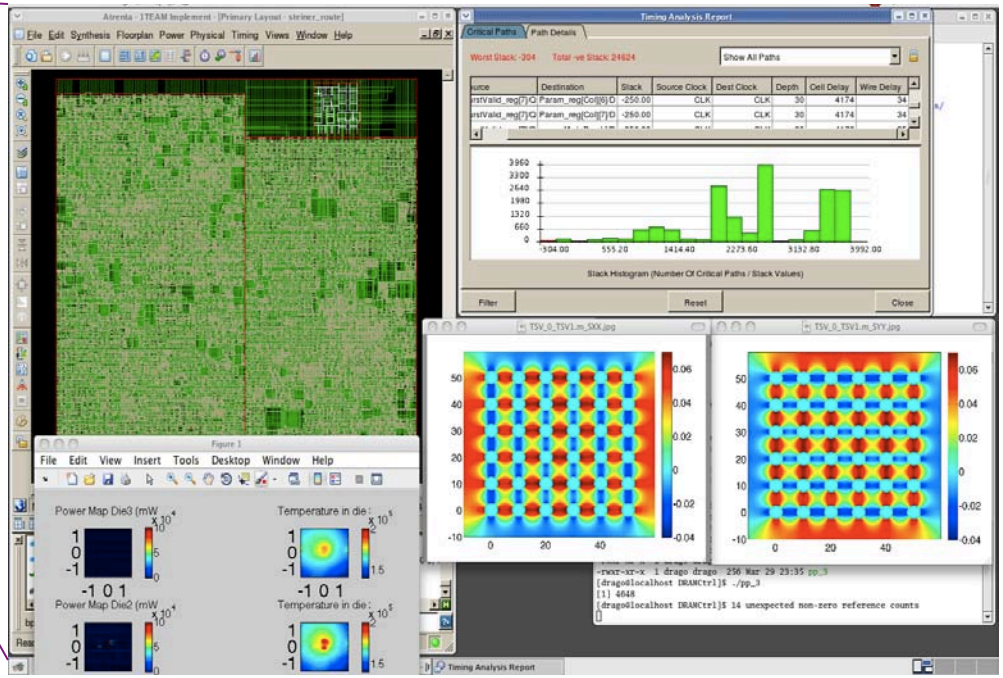
Physical Design

Extraction

Verification

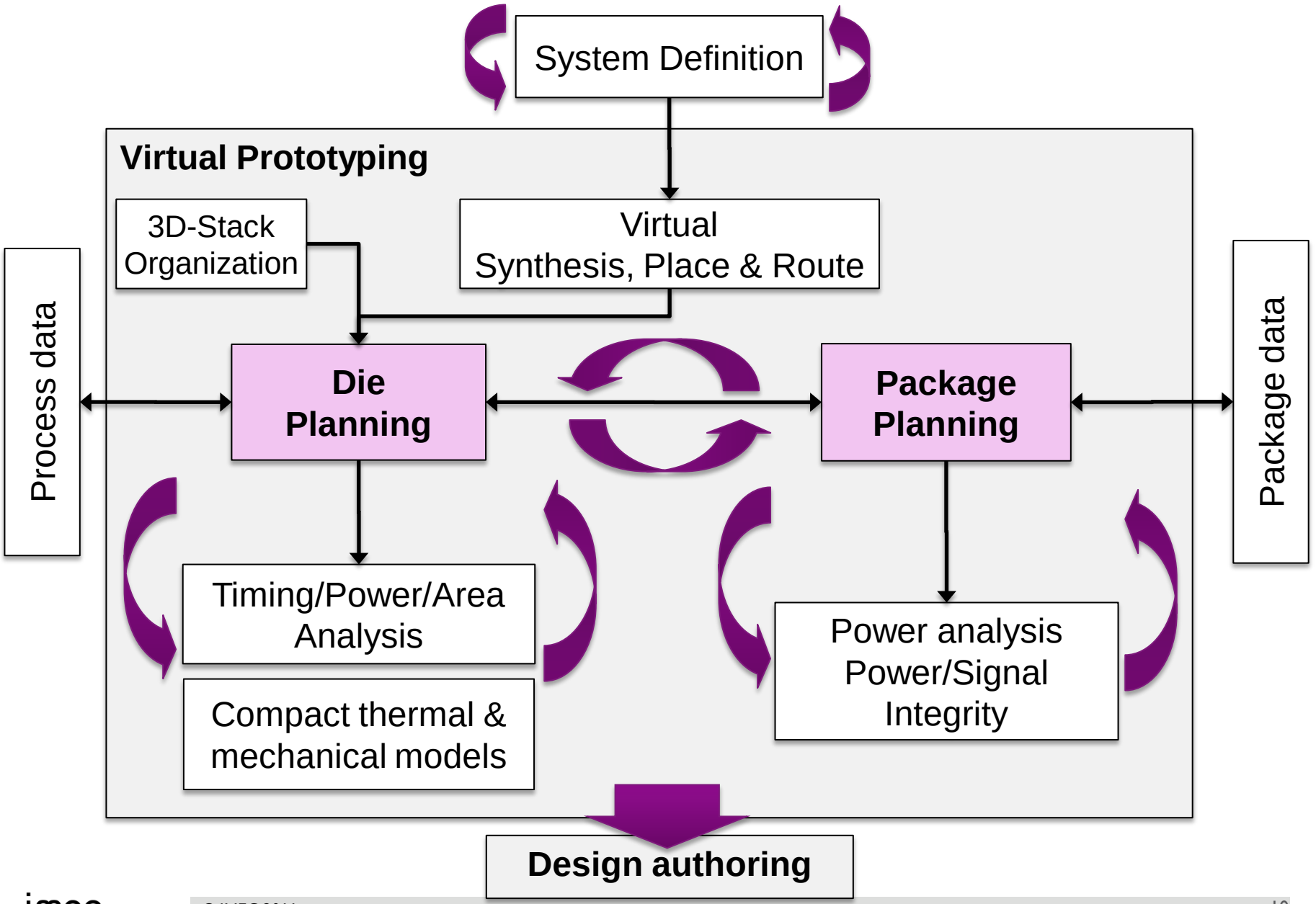
Stack
Sign-off

DFT for 3D




- Quick and dirty design flow" providing early assessment of timing/power/area/cost of 3D product ideas

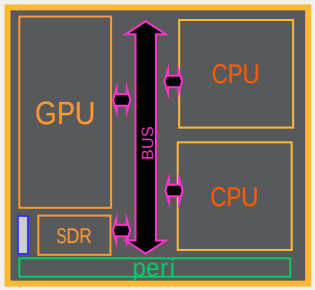
# Current status of the PathFinding Flow



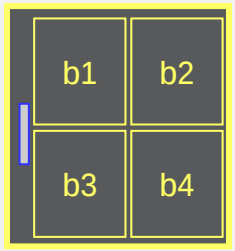
# Die Planning — Illustration

## System Definition

Logic




Memory

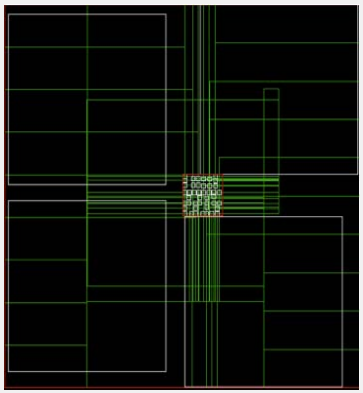



## Virtual prototype — after virtual synthesis, place & route

ATRENTA

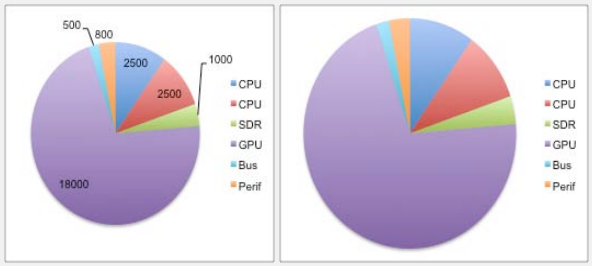
Bottom tier

Top tier

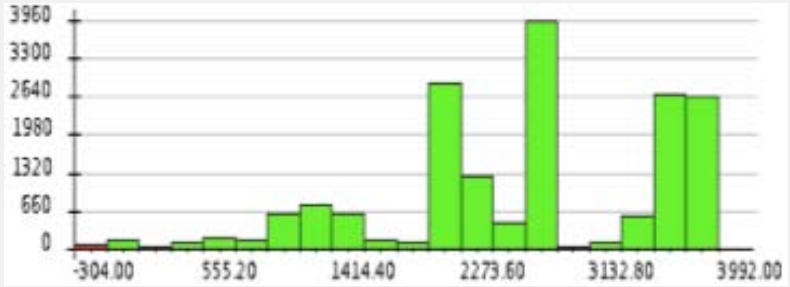


## Figures of Merit

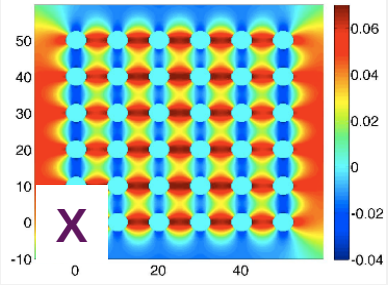
1. Area/power

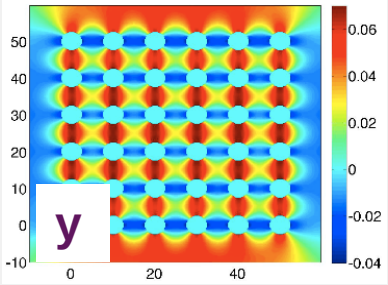



2. Timing analysis

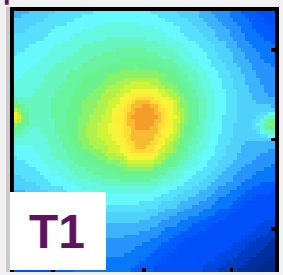


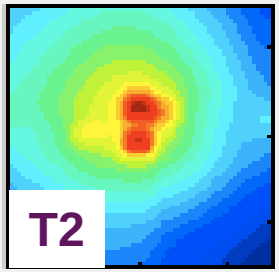

3. TSV displacement maps




4. Thermal maps



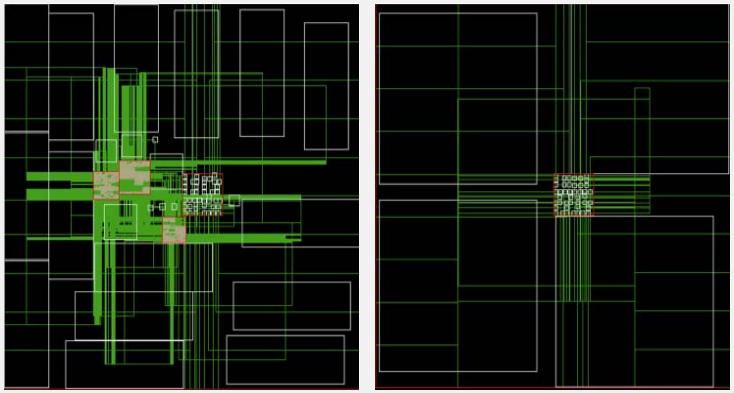




5. Cost

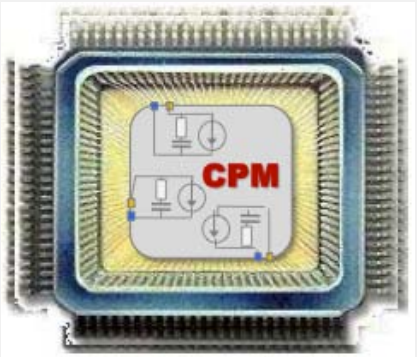
Constraints

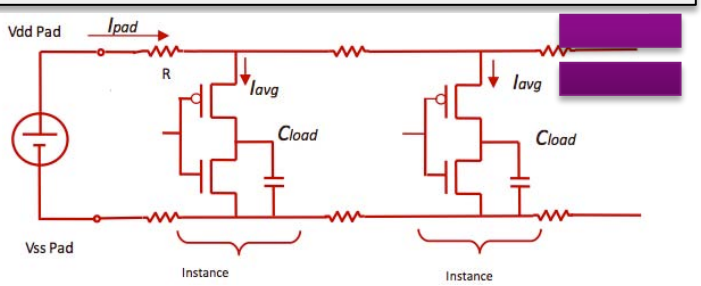
# Package Planning — Illustration

## Virtual die prototype



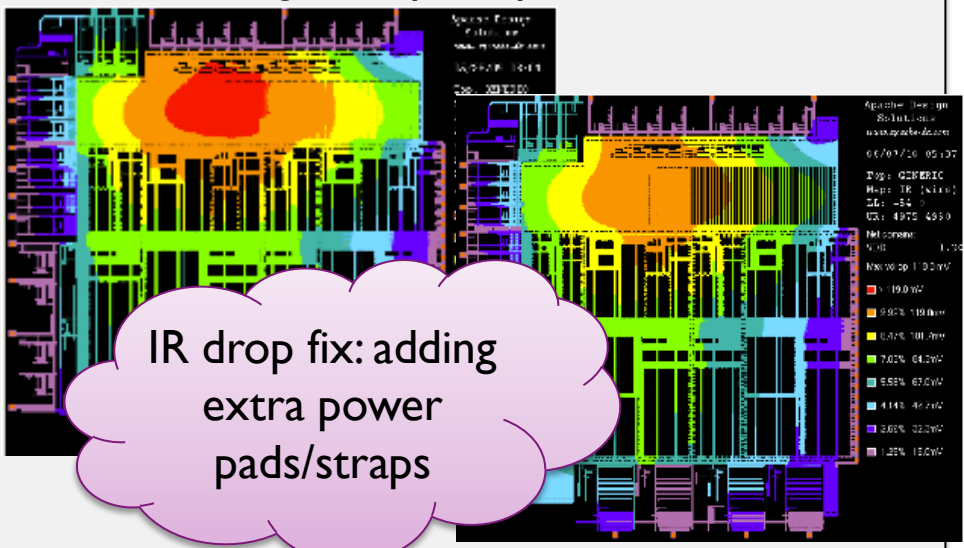
## Virtual package prototype




## Figures of Merit

Static voltage drop map

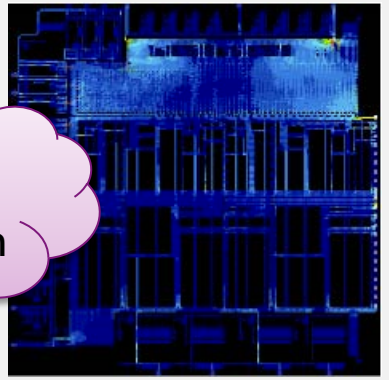


IR drop fix: adding extra power pads/straps

Wire/via currents

Better via distribution

Electro-migration



# SSG ON 3D-TEST

## Charter

- Inventorize need for and timeliness of standards in 3D test and DfT
- If appropriate, formulate Project Authorization Requests (PARs) for starting up an IEEE Standard Development Working Group (SDWG)

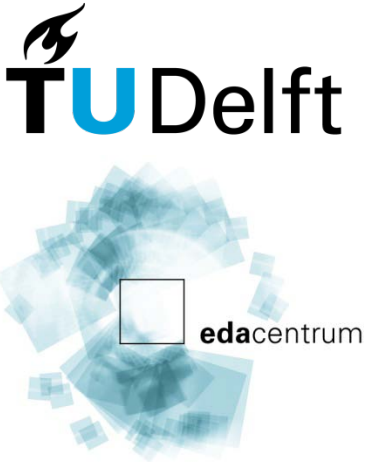
- **Organization & Participation**
  - Sponsored by IEEE Test Technology Standards Committee (TTSC)
  - 54 participants from companies/institutes around the globe
  - Chair: Erik Jan Marinissen (IMEC)
- **Activities to date**
  - Active per January 2010
  - Web site and e-mail reflector for internal communication
  - Weekly WebEx conference calls (provided by Cisco Systems)
  - First formal report due at TTSC meeting at VTS'10, April 20

## I. IEEE STANDARDIZATION STUDY GROUP ON 3D-TEST

# PARTICIPATING COMPANIES

I. IEEE STANDARDIZATION STUDY GROUP ON 3D-TEST

# INSTITUTES, UNIVERSITIES, AND CONSULTANTS









ITRI
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Research Institute






# IDENTIFIED STANDARDIZATION NEEDS

During the SSG discussions,

the following standardization needs were identified:

- **Die and Stack Test**
  1. DfT test access architecture
  2. Wafer probe interface
- **Access for Board-Level Users**
  3. Board-level interconnect test
  4. Access to embedded instruments
- **Test Data Formats**
  5. Wafer map and device tracking
  6. Standard Test Data Format (STDF)

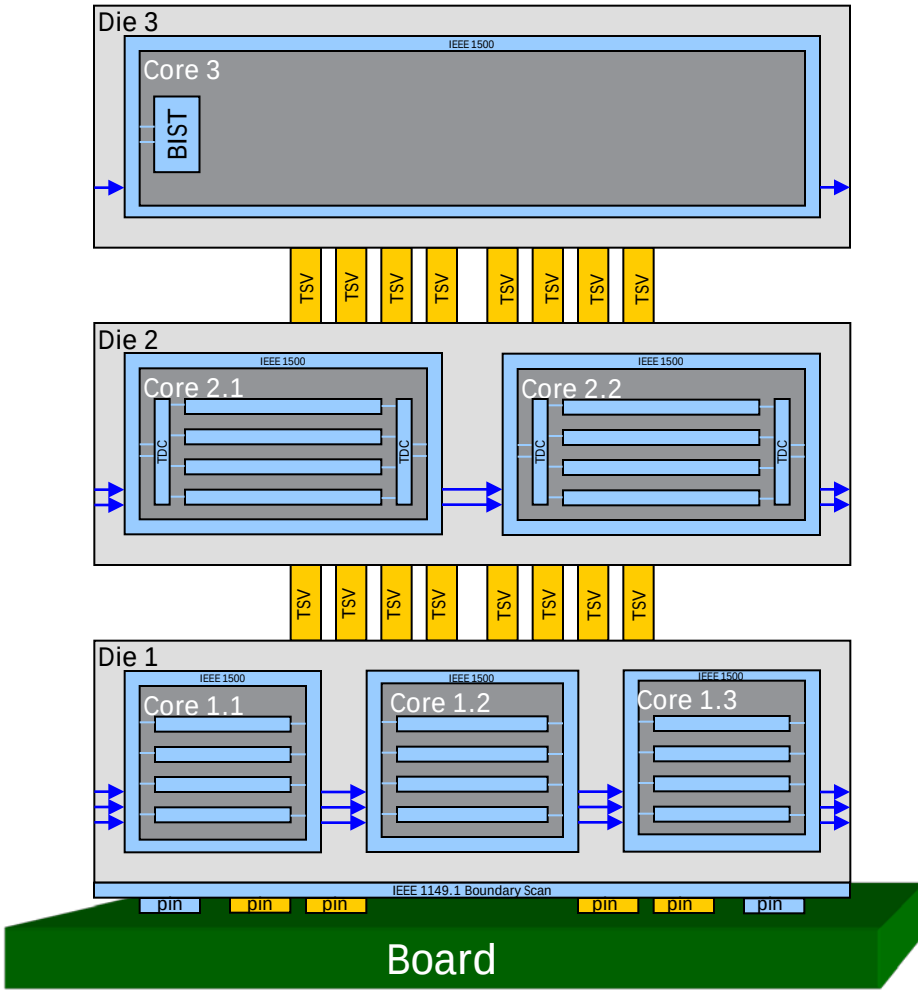
# LEVERAGING EXISTING DESIGN-FOR-TEST

## Functional Design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

## Existing Design-for-Test

- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1



# 3D DFT ARCHITECTURE – OVERVIEW

## Functional Design

- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

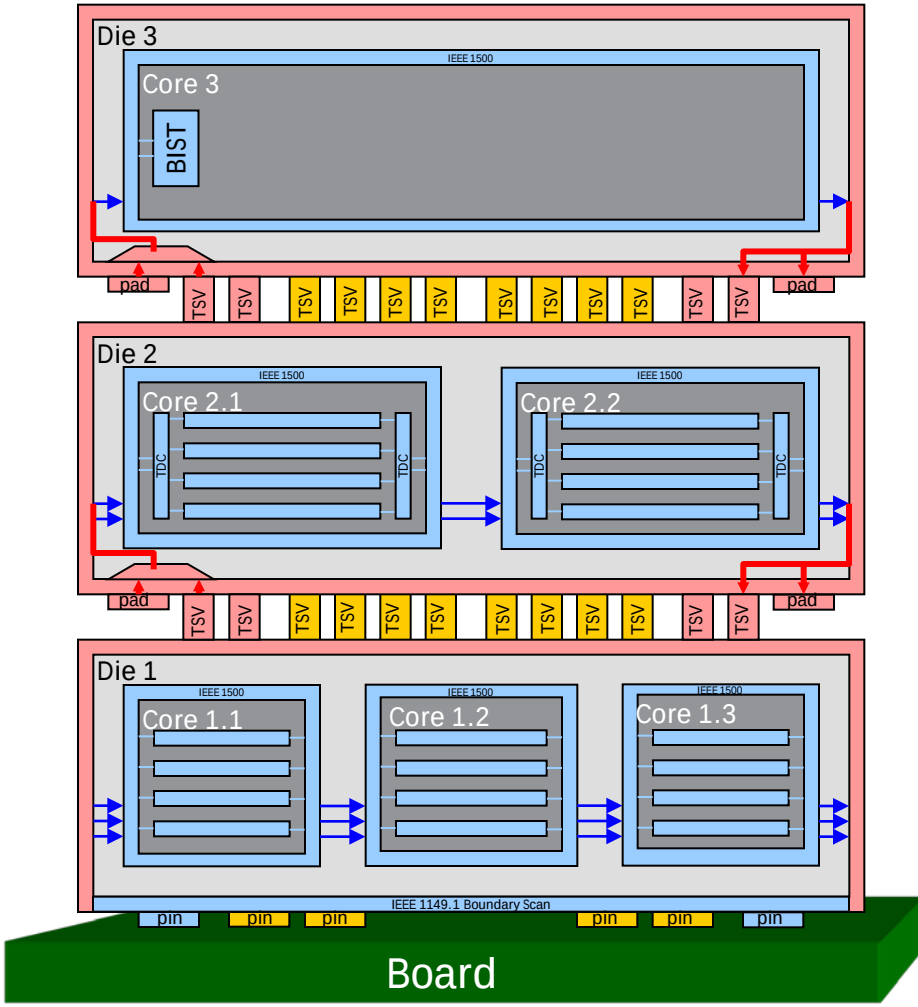
## Existing Design-for-Test

- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1

## 3D DfT Architecture

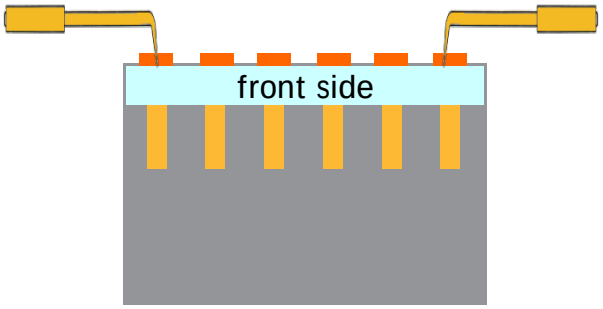
Test wrapper per die

- Based on IEEE Std 1500
- Two entry/exit points per die:
  1. Pre-bond : extra probe pads
  2. Post-bond : extra TSVs



# FRONT-SIDE vs. BACK-SIDE PROBING

## Front-Side of Thick Wafer



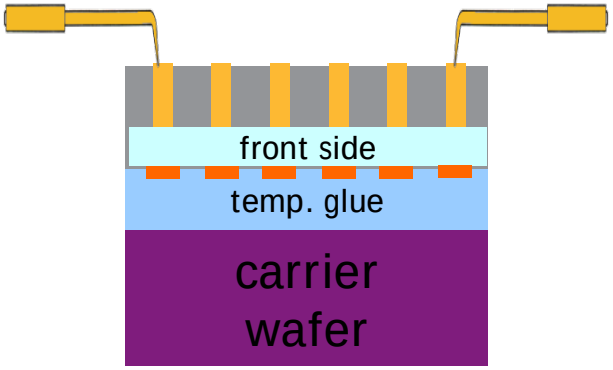

*Benefits*

- Handling full-thickness wafer easier

*Drawbacks*

- Defects due to thinning not covered
- TSVs not exposed yet; testing them requires expensive DfT / test time

## Back-Side of Thinned Wafer




*Benefits*

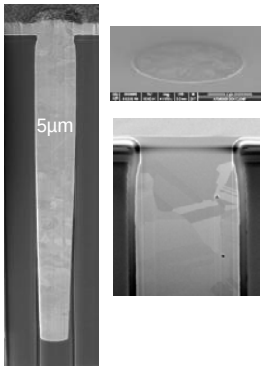
- Test can also cover thinning defects
- Dual-side access on subset of TSVs

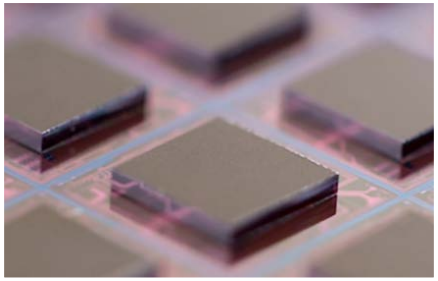
*Drawbacks*

- Thinned wafer on carrier: no front-side access
- Probe force might damage intra-die circuitry

# SUMMARY

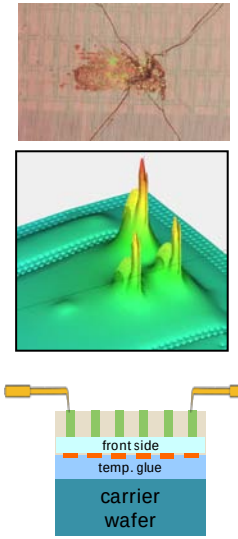
- Status
  - 3D-SIC TSVs mature
  - Stacking solutions available



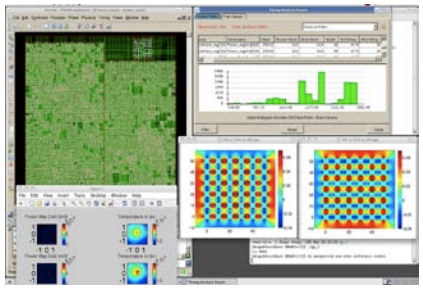
Challenges

- Reliability
- CPI
- Thermal
- Test




Opportunities for EDA

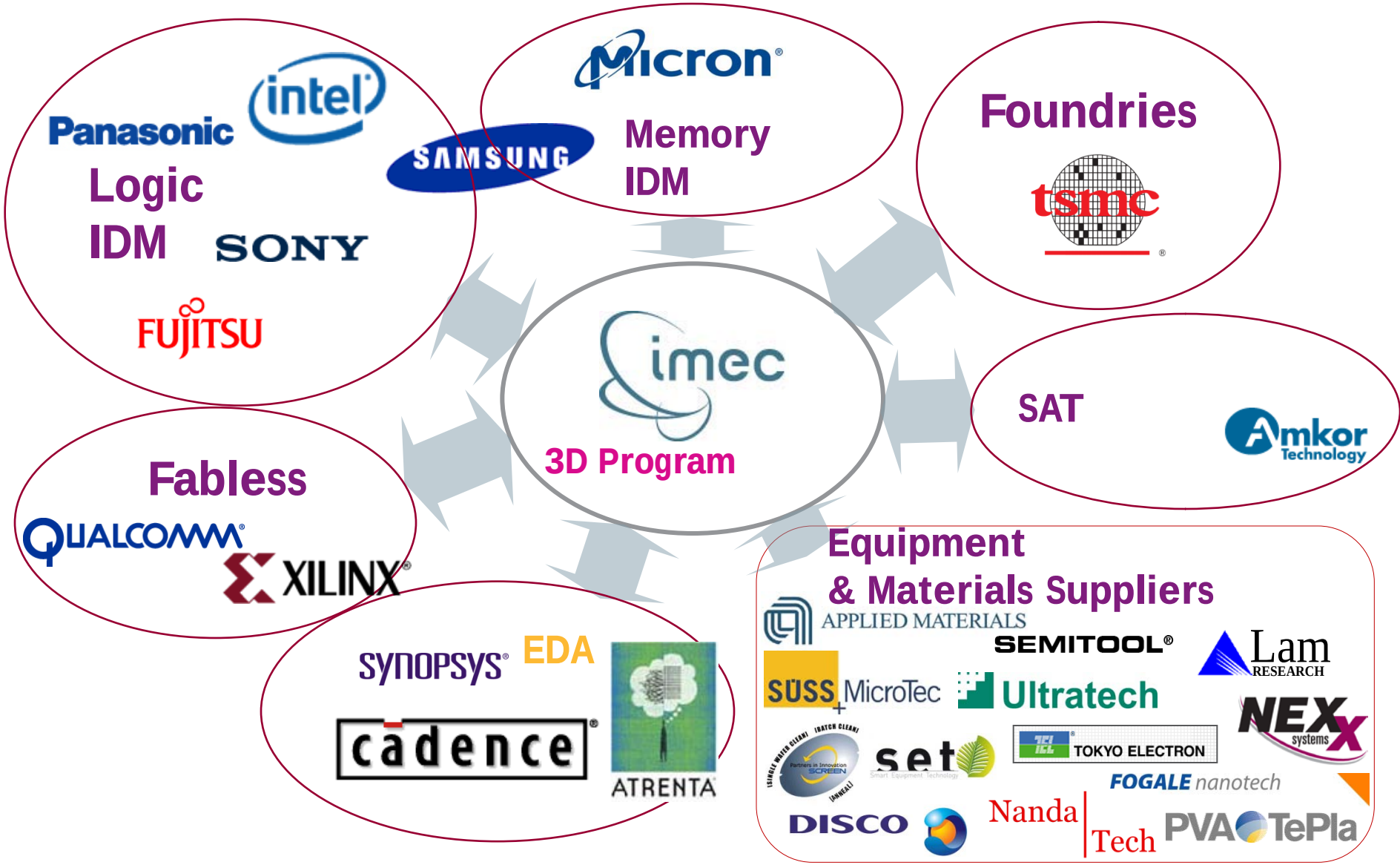
- Pathfinding flow



- DfT & infrastructure

TTSC Standardization Study Group on 3D Test

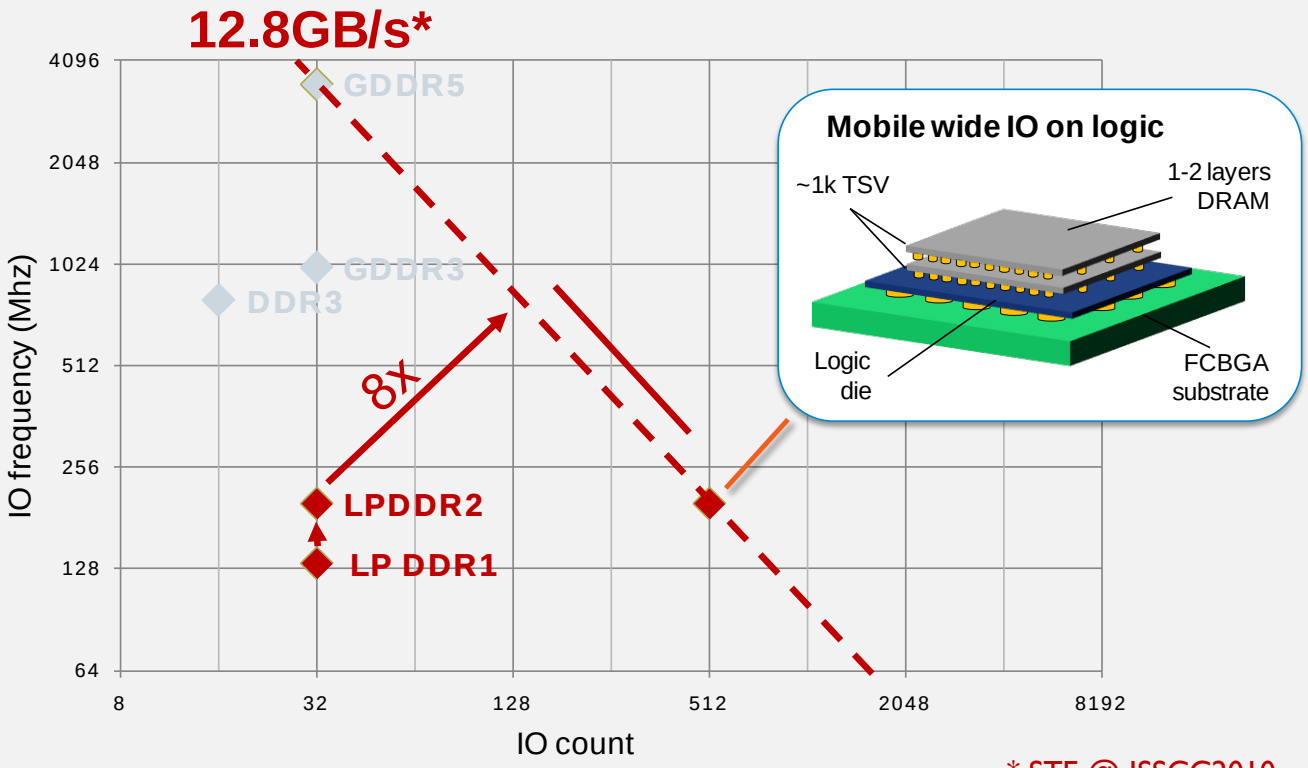
# 3D ecosystem at imec



# TECHNOLOGICAL RULE CHANGING - 3D & MOBILE VIDEO SERVICES

HD mobile video

E.g, full HD lifecast
(lifecast.com, utube, ...)




* STE @ ISSCC2010

*With an expected ~130% CAGR,*
*Service Providers would commit murder for this technology!!!*

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# ASP-DAC 2011 Panel discussion: Advanced Packaging and 3D Technologies

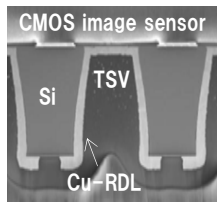
## “Packaging trends towards 3D integration and synergies between wafer process and packaging”

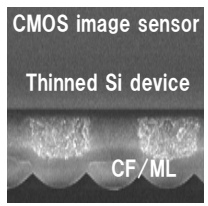
Hirokazu Ezawa
Advanced Packaging Engineering Dept.
Toshiba Corporation Semiconductor Company
2011,January 28th

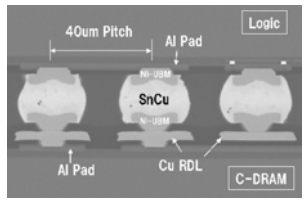
# Current technology platforms for chip-stacking

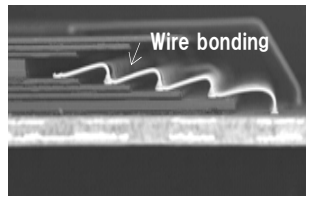
| Process technologies for 3D TSV stacking | CMOS imager WLP | CMOS imager BSI | Chip-on-Chip Logic on Memory | NAND Chip stacking |
|---|---|---|---|---|
| Carrier substrate bonding | + | + | | |
| Wafer thinning, cleaning | + | + | | + |
| TSV etching | + | | | |
| Fine pitch RDL<br>Low temp. curable DL | + | | + | |
| Micro bumping<br>Fine pitch solder joining | | | + | |
| Juggling thinned chips | | | | + |

+ qualified for mass production in Toshiba



# Chip-stacking and TSV : Current Status

- NAND flash memory modules
  - <30um thick Si chip
  - Stacking 17 chips in a package

- System LSI modules
  - Stacking logic on large-scale DRAM
  - Higher data rate has been realized while power consumption is kept lower.

- CMOS image sensor modules (8 inch)
  - Reflowable WLP using TSV
  - The worldwide first mass production supplier

# Large-scale memory module

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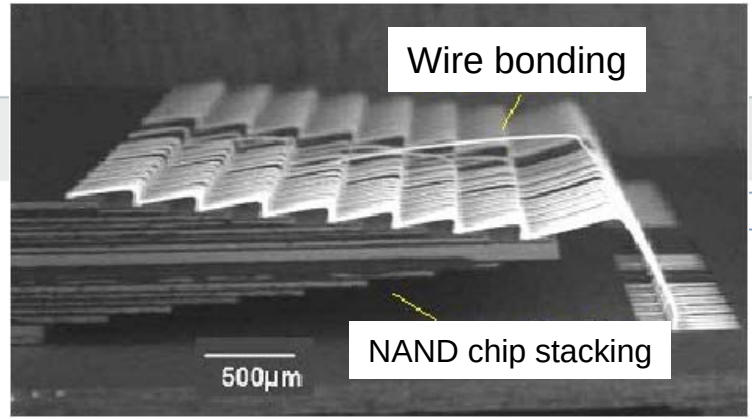
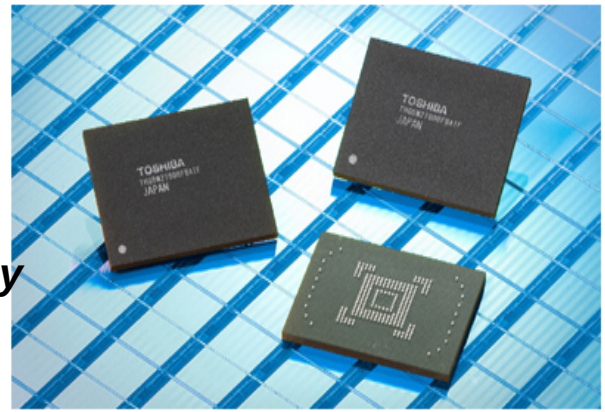
## Toshiba Launches Industry's Largest[1] Embedded NAND Flash Memory Modules

*e•MMC™[2] Compliant Embedded Memories Combine up to 128GB NAND and a Controller in a Single Package*

17 Jun, 2010




***Toshiba Semiconductor Company***
***HP/News Release/Topics***



TOKYO—Toshiba Corporation (TOKYO: 6502) today announced the launch of a 128-gigabyte (GB) embedded NAND flash memory module, the highest capacity yet achieved in the industry. The module is fully compliant with the latest e•MMC™ standard, and is designed for application in a wide range of digital consumer products, including smartphones, tablet PCs and digital video cameras. Samples will be available from September, and mass production will start in the fourth quarter (October to December) of 2010.

The new 128GB embedded device integrates sixteen 64Gbit (equal to 8GB) NAND chips fabricated with Toshiba's cutting-edge 32nm process technology and a dedicated controller into a small package only 17 x 22 x 1.4mm [3]. Toshiba is the first company to succeed in combining sixteen 64Gbit NAND chips, and applied advanced chip thinning and layering

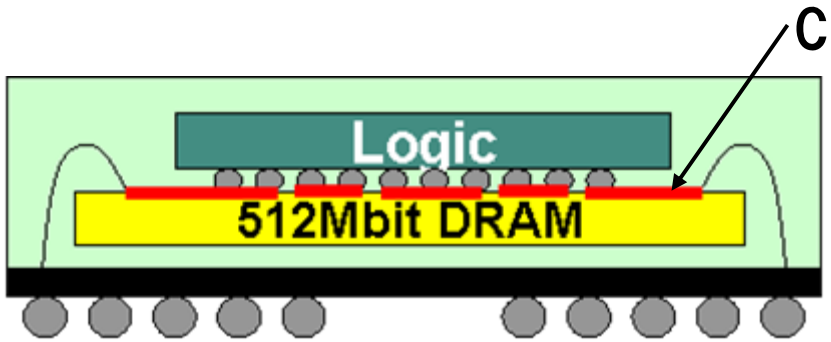
# Structure of SiP with CoC technology

## ■Stacking memory chip on logic chip


Chip size: Logic > Memory

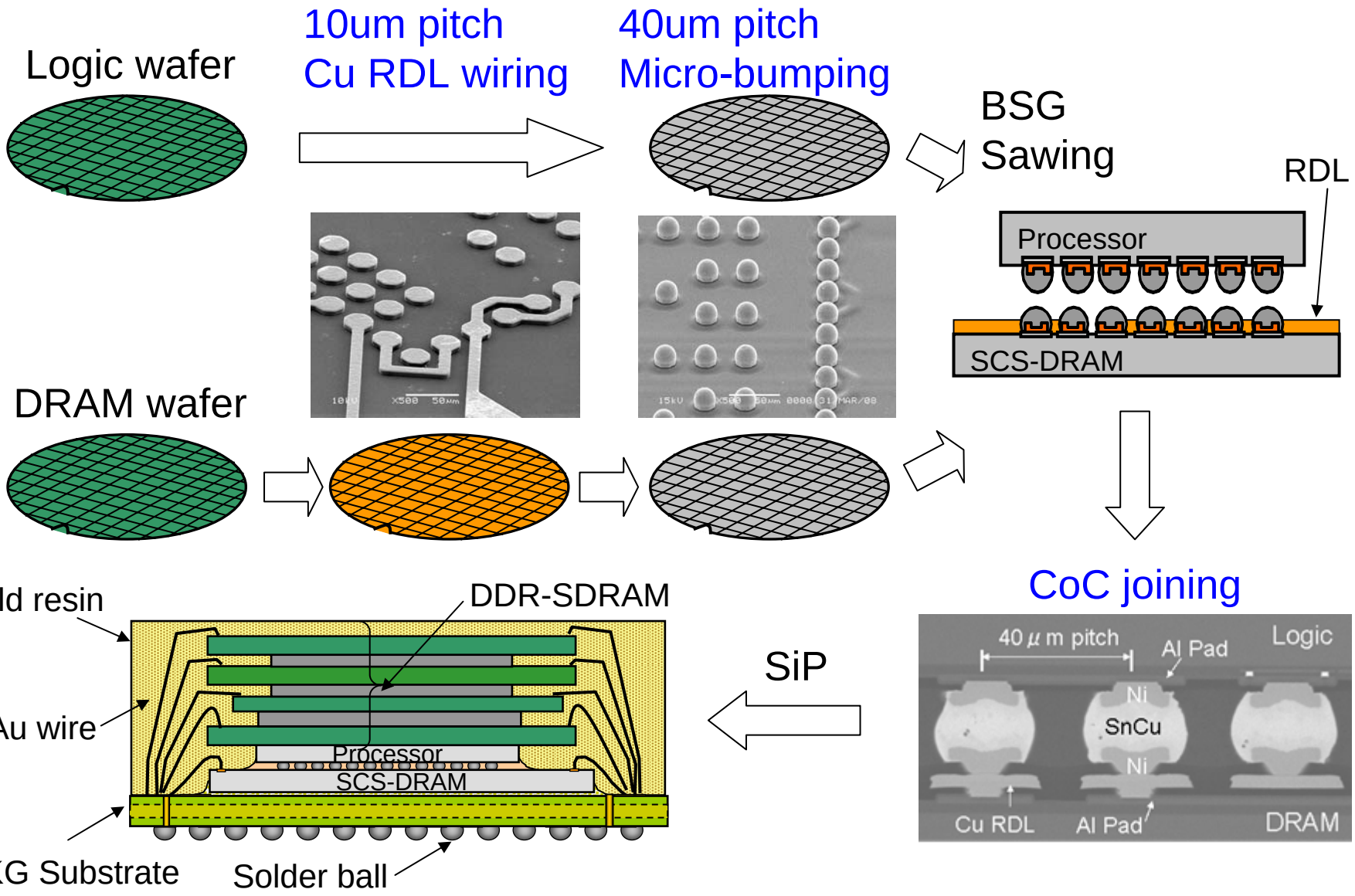
## ■Stacking logic chip on larger-size memory chip

RDLs on memory route signal I/Os from logic chip to peripheral pads on memory chip




Chip size: Memory > Logic

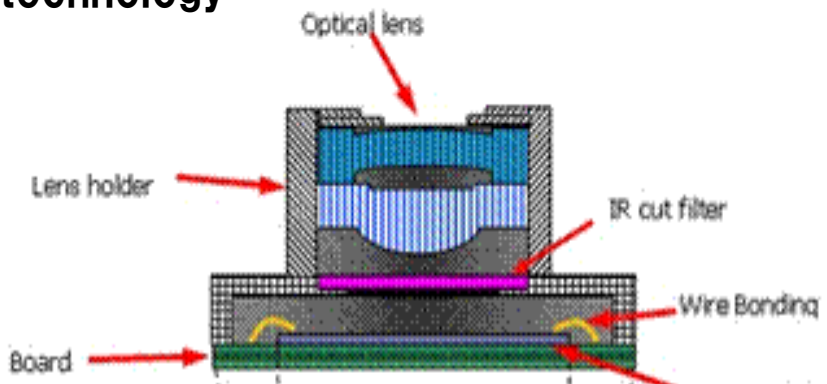
# Chip-stacking instead of e-DRAM



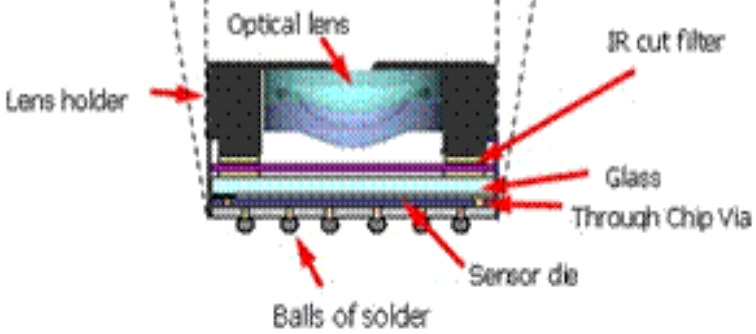
# Chip scale camera module

- Reduction of package size using TSV
- Cost reduction

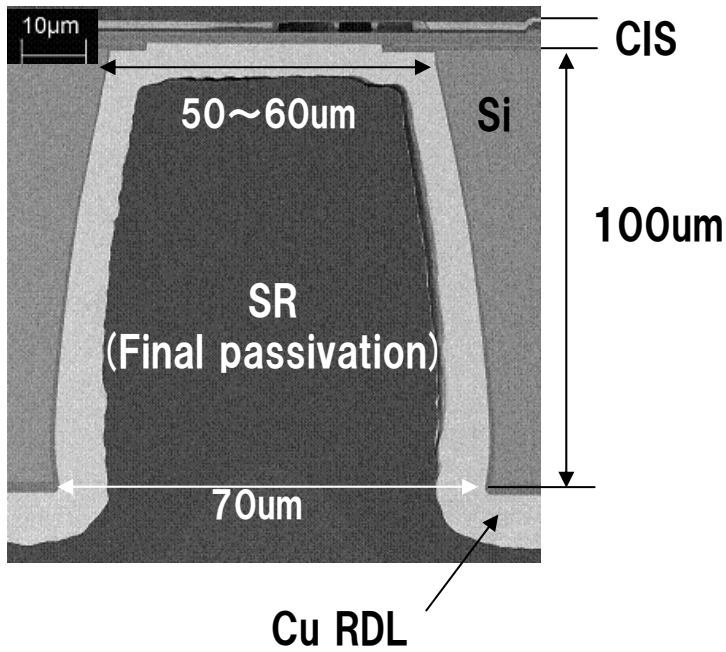
Current technology




CSCM technology




Cu RDL through TSV



# Chip-stacking and TSV : Challenges from now on

■ **NAND flash memory modules**

- **<20um thick Si chip**
- **Low power consumption**

***How thick would be allowed for proper functionality?***

***What makes TSV stacking affordable?***

■ **System LSI modules**

- **20um pitch bumping and CoC joining**
- **Hetero-integration** (RF,Analog,Memory,Sensors,MEMS )

***What facilitates synergies between WLCSP and TSV?***

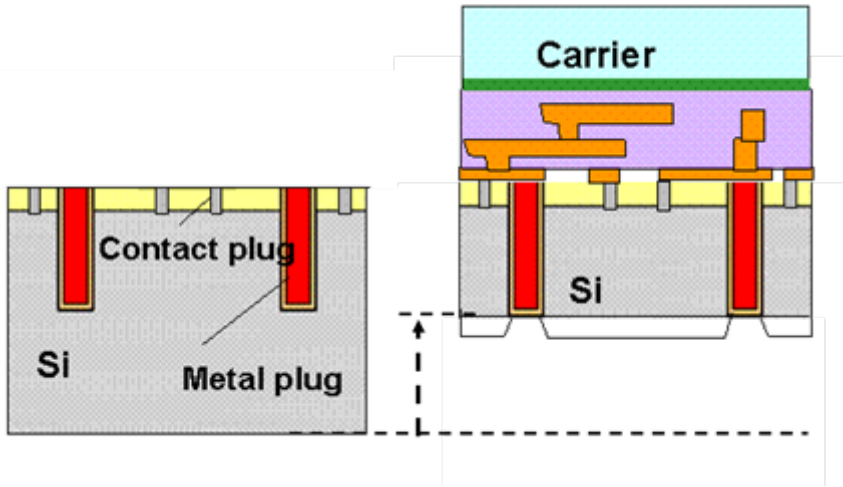
■ **CMOS image sensor modules**

- **Wafer level lens**

***How strong would be affinity of TSV for BSI?***

# Manage to narrow TSV process options

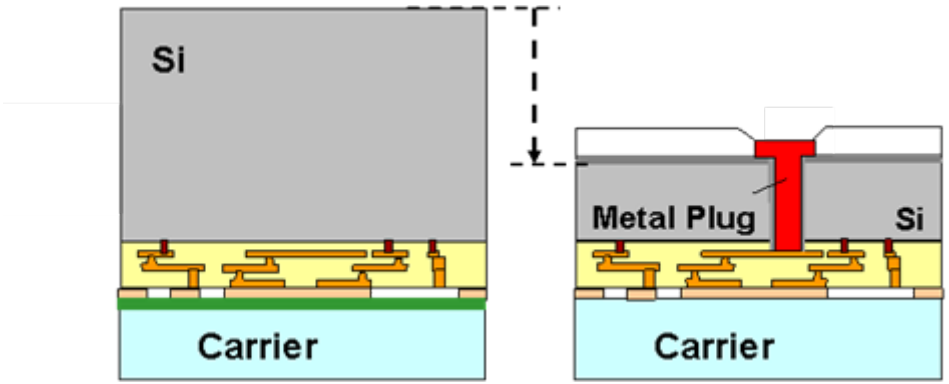
## ■Via-middle (Metal filling after FEOL)




Existing tools available in Si CR.
No need of low temp. liner-CVD

Concerns:
TSV process impacts on BEOL.
Metal contamination when via reveal.

## ■Back-side via (Metal filling after Si thinning)




Separate TSV line from Si fab

Concerns:
Adhesive limits TSV process temp.
Need of back-side aligning litho.
Carrier selection is critical.

# TSV stacking as of today and PKG challenges

- **Key equipments and materials for TSV mass production**
  *Still under basic development*
  - BSG/CMP/Wet-clean integrated tool
  - Temporary bonding adhesives and their relevant bonding/de-bonding HVP tool
  - 12inch WTW bonding tool. Yield allowance.
  - Inspection tool (via voids…)
  - Sawing tool for thinned wafer instead of blade.

- **Cost-reduced 3D packaging**
  - Wire free
  - Organic substrate free
  - Fine pitch RDL on Fan-Out WLCSP

# FAQ

- **Where do you allocate TSV production?**
  - **TBD.**

- **When would TSV products sprout up?**
  - **Depends on the market providing novel values.**

- **What are dominant factors affecting TSV process cost?**
  - **Thinner Si would be preferred.**
    - ***Specific design for thinned Si?***
  - **Throughput of multi-chip stacking**
    - ***W-to-W bonding would be preferred.***
    - ***Specific design dedicated to its stacking?***

***Any other vying technologies for 3D integration?...***

# Thank you.

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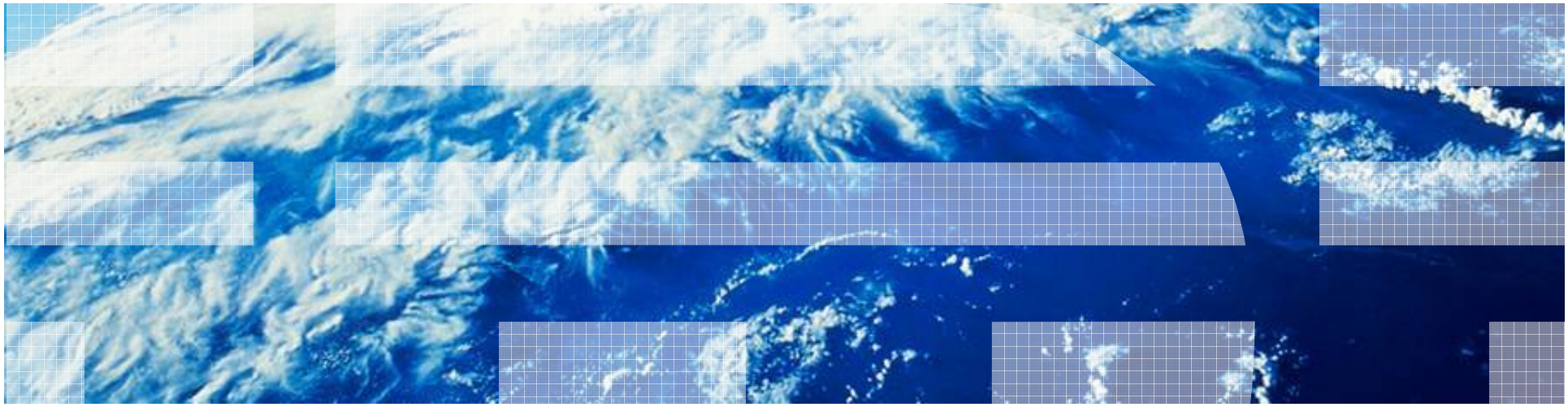
# Future Challenges for 3D-IC Packaging

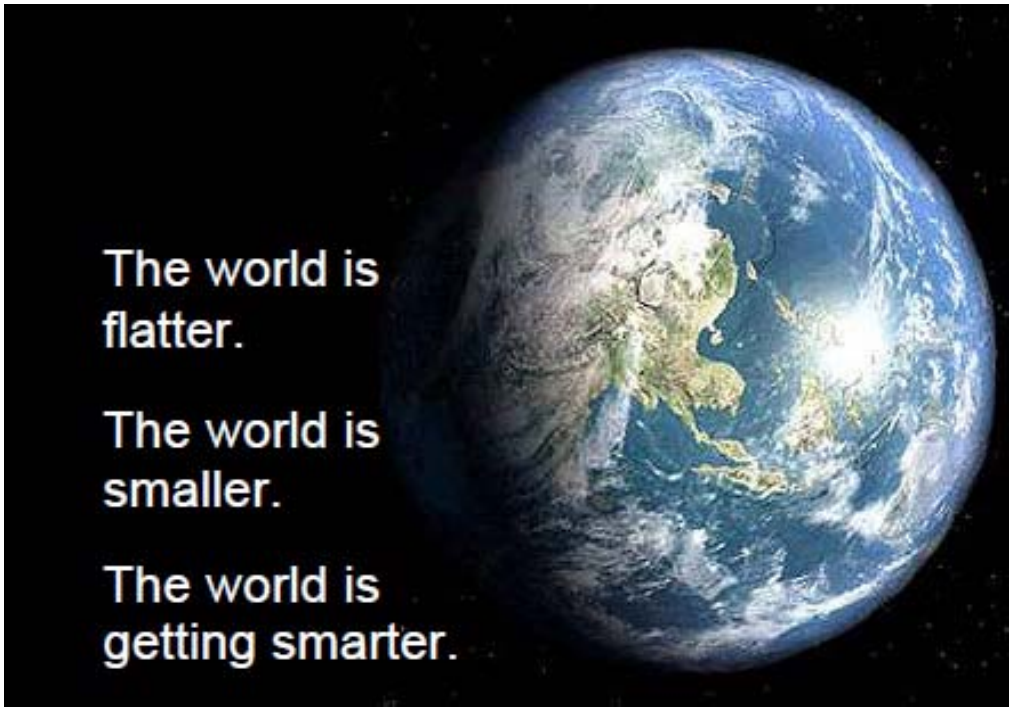
**Panel Discussion : Advanced Packaging & 3D Technologies**

Electronic & Optical Packaging, IBM Research Tokyo

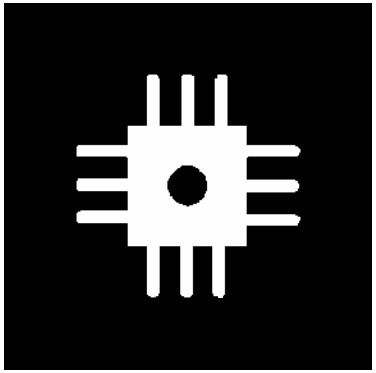
Yasumitsu Orii



# Smarter Planet

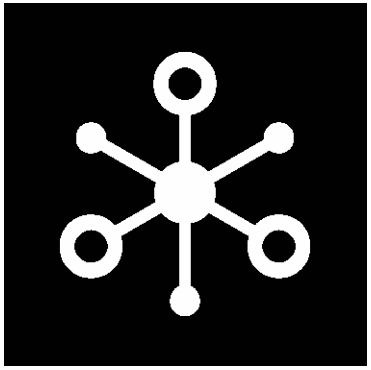



## Instrumented



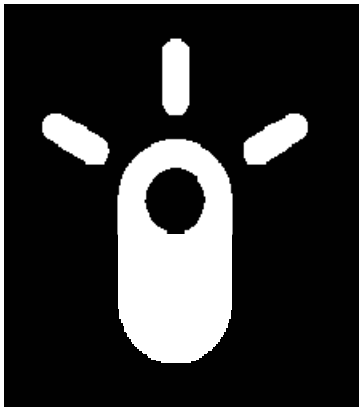
The world is becoming instrumented. Sensors are being embedded everywhere: in cars, appliances, cameras, roads, pipelines…

## Interconnected



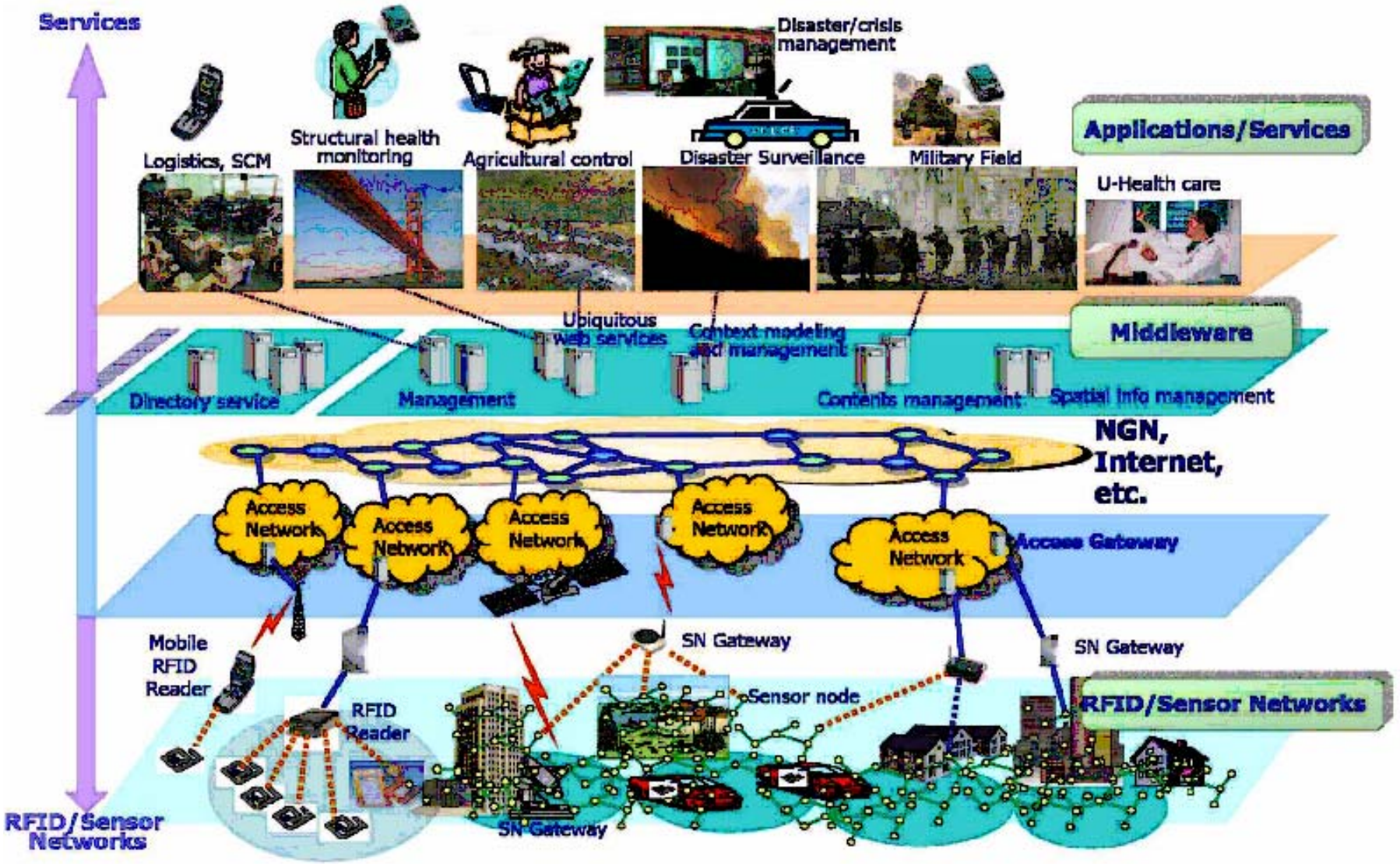
Our world is becoming interconnected.

## Intelligent



All of those instrumented and interconnected things are becoming intelligent. They are being linked to powerful new backend systems that can process all that data, and to advanced analytics capable of turning it into real insight, in real time.

# Internet of Things

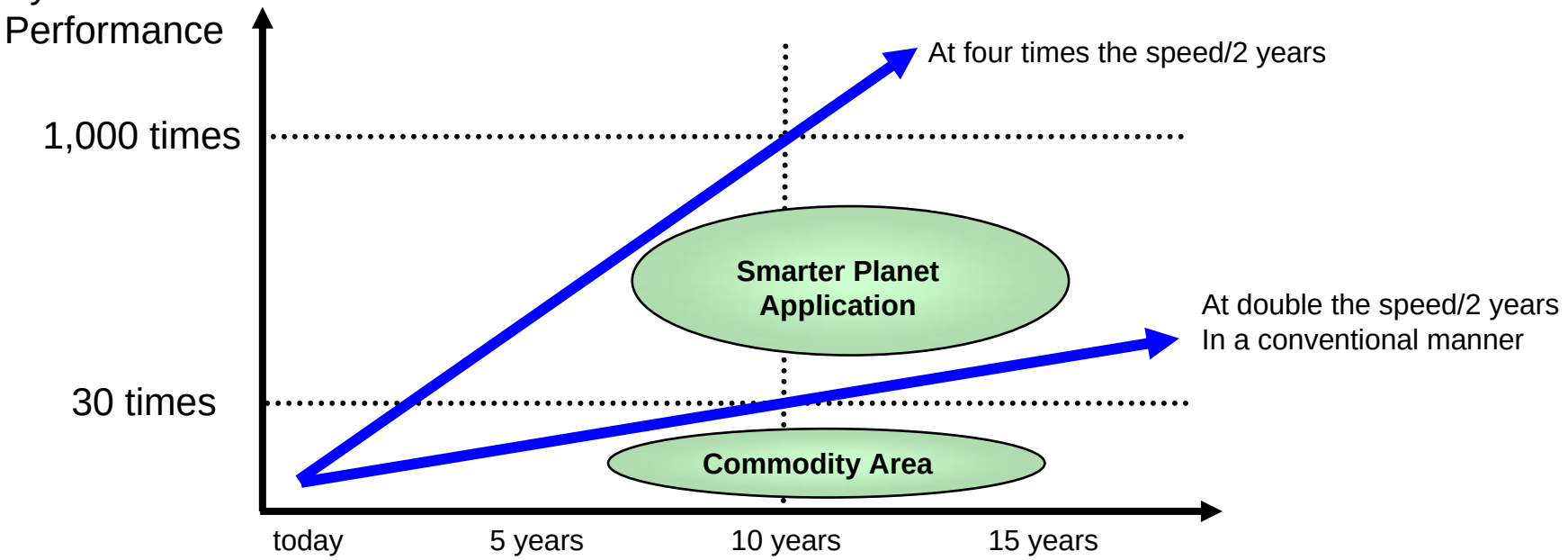


# More Powerful Computer System for Smarter Planet

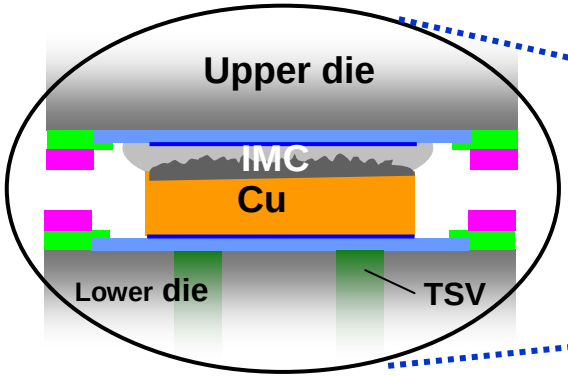
- ✓ Sensors are being embedded everywhere: in cars, appliances, cameras, roads, pipelines…
- ✓ The oceans of data to be produced.
- ✓ All of those instrumented and interconnected things are becoming intelligent. They are being linked to powerful new backend systems that can process all that data, and to advanced analytics capable of turning it into real insight, in real time.

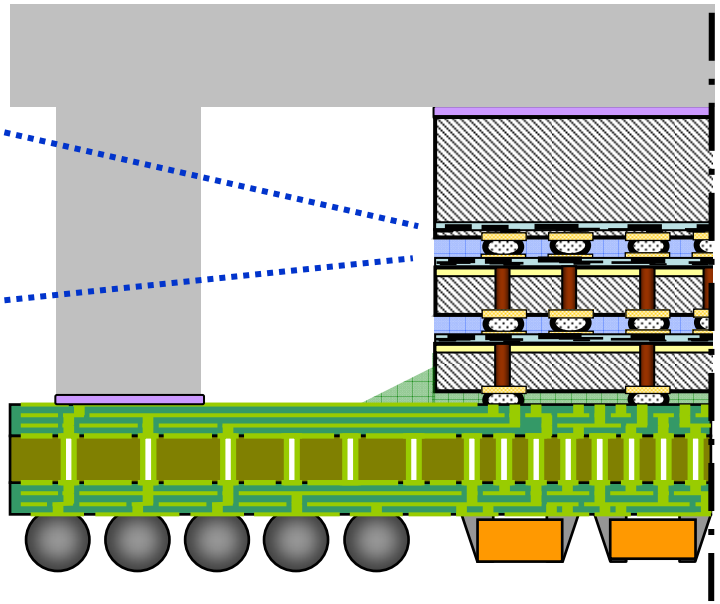

World First PFLOPS Super Computer :
1.03 PFLOPS (Jun/2008)

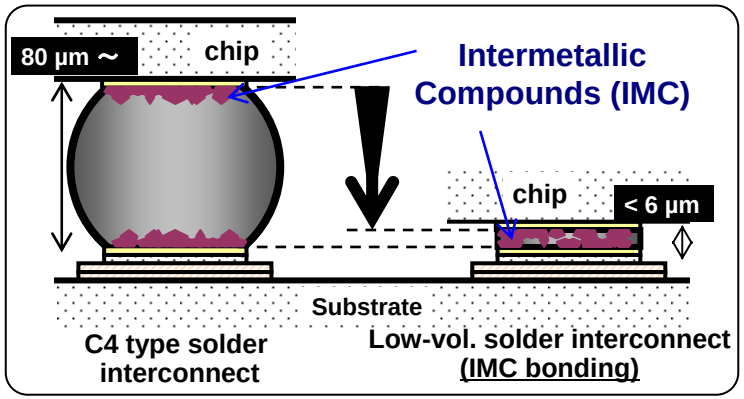
⇨ Exascale computing system

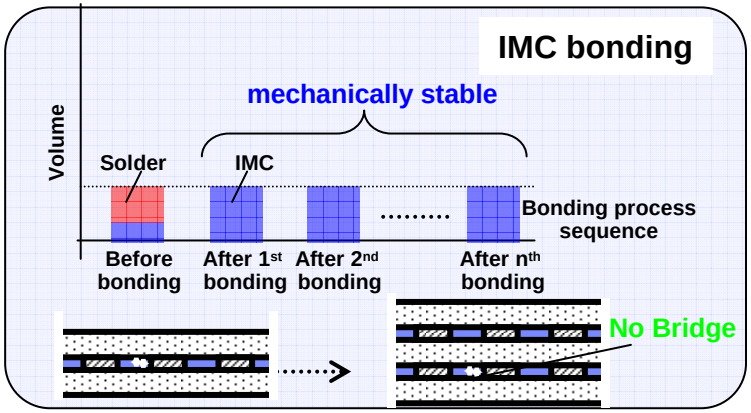


# Technical Challenges for 3D-IC



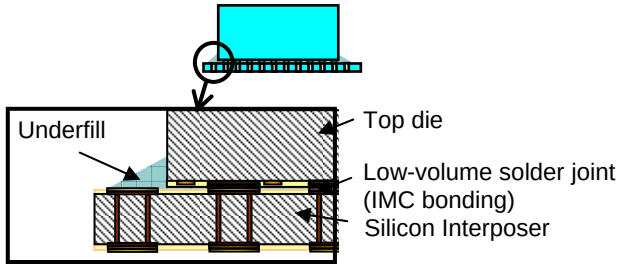


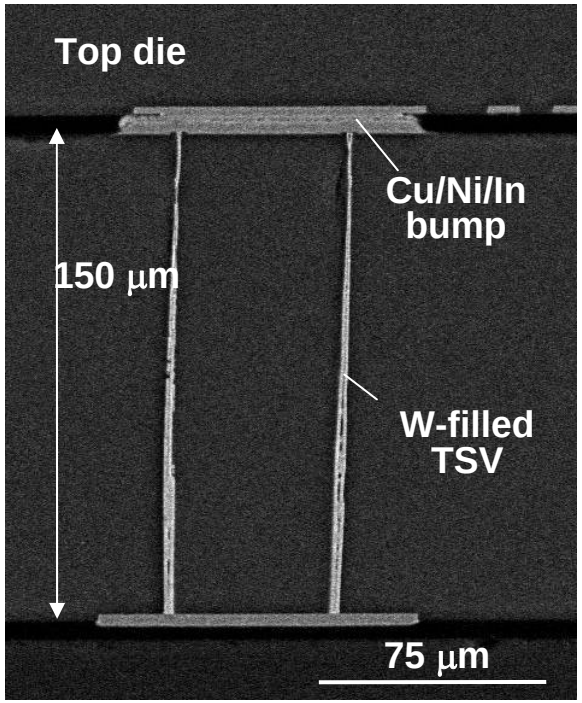




1. Die to Die Interconnection
2. Die to Die underfill

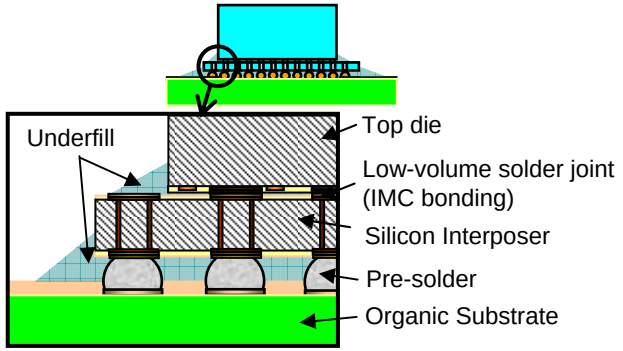
# Configurations of IMC Bonding Evaluation Test Vehicles

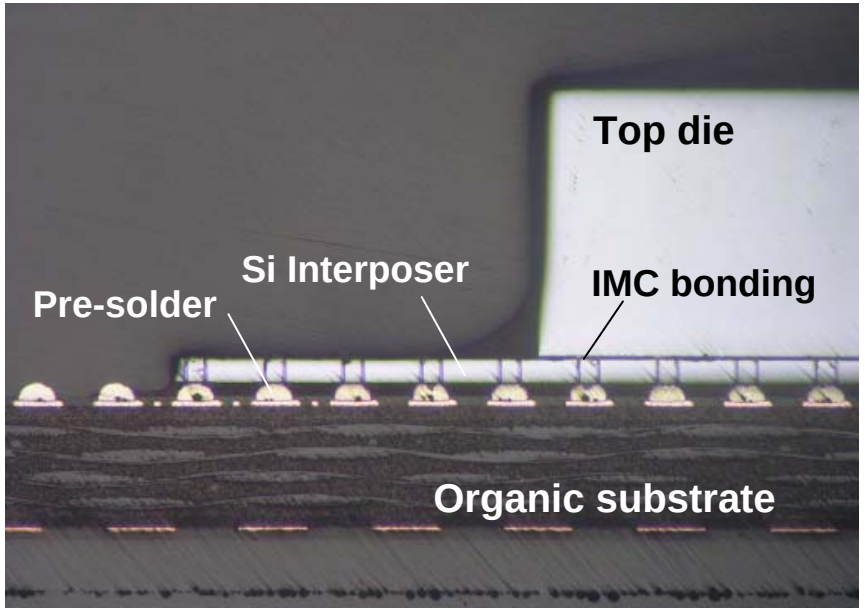
**Configuration-A : Si on Si**




**Configuration-B : Si on Si + Organic**

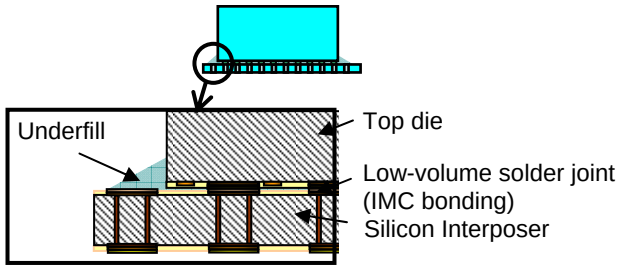


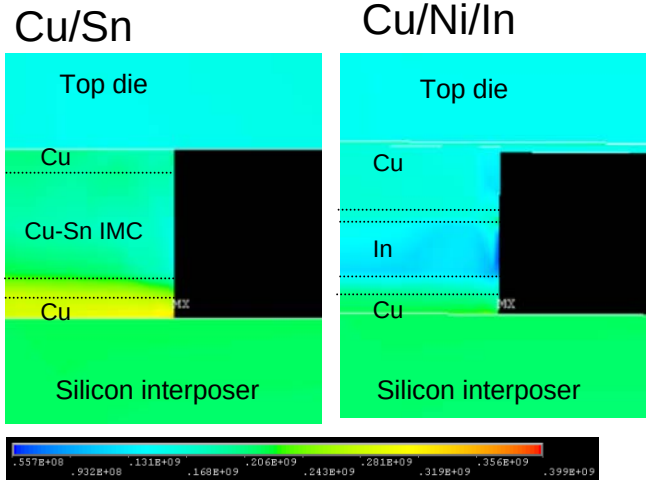

**60th ECTC, 2010, K. Sakuma, Y. Orii et al.,**

# Joint Materials Comparison : Cu/Sn and Cu/Ni/In

**Configuration-A : Si on Si**

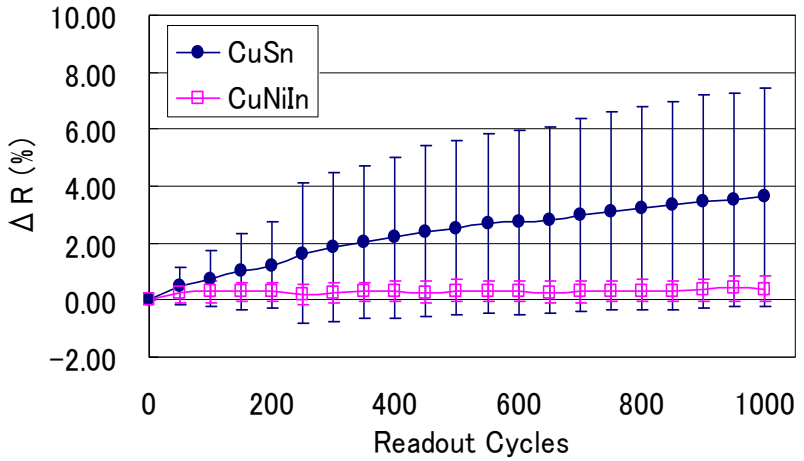



## Joint's Stress




DTC

| Test | Stress Conditions | Cycle time (min) | Number of cycles completed |
|---|---|---|---|
| DTC | -55ºC to +125ºC | 35 | 1,000 |




**60th ECTC, 2010, K. Sakuma, Y. Orii et al.,**

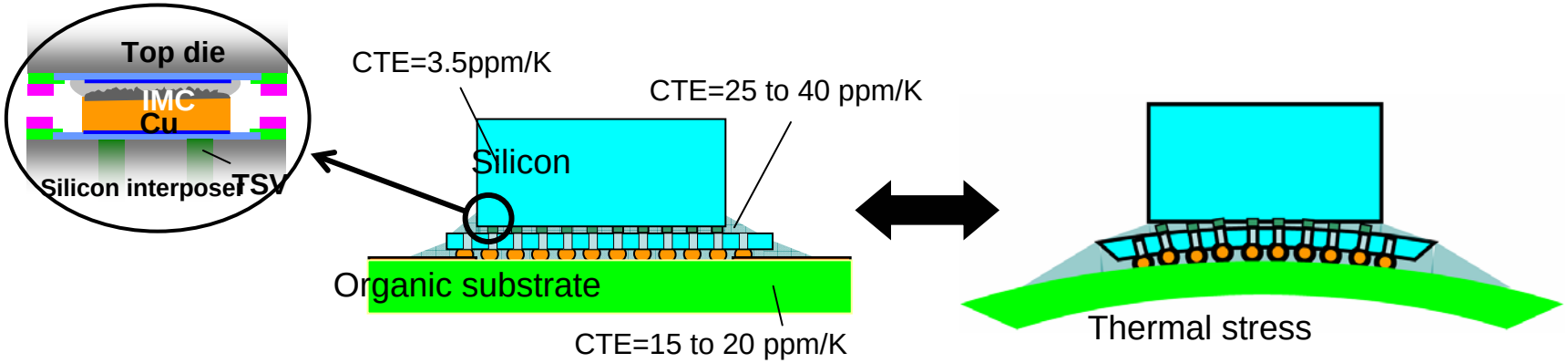
- **Stress on the joints is greater for the Cu/Sn joint than the Cu/Ni/In joint.**
- **A gradual increase in electrical resistance observed for the Si die stack samples with Cu/Sn joints.**

# Reliability Results of 3D Chip on Organic sub. with IMC Bonding

**Configuration-B : Si on Si + Organic**

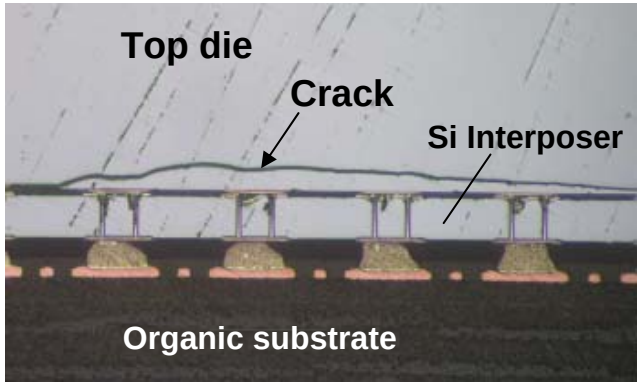
## Deep Thermal Cycle (DTC) results for stacked samples

**DTC Condition:** -55 to +125C, 15min/15min ($\Delta T$ = 180C)
Time of exposure at min and max T: 10min

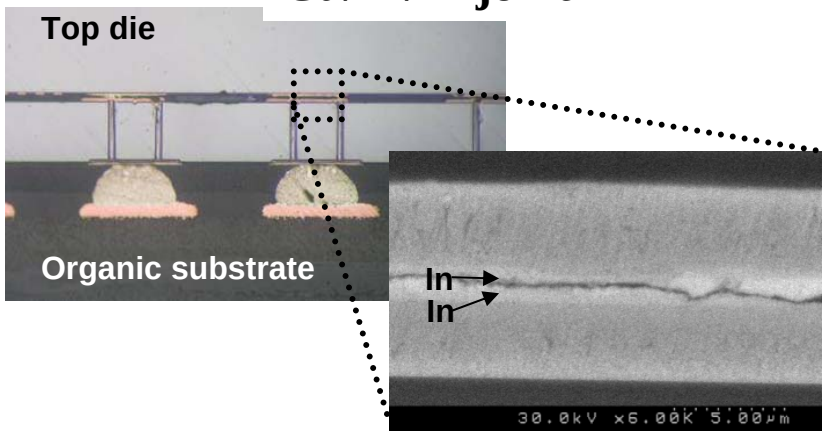



- The mechanical stress during thermal cycling has a significant impact on the bonding interconnections.

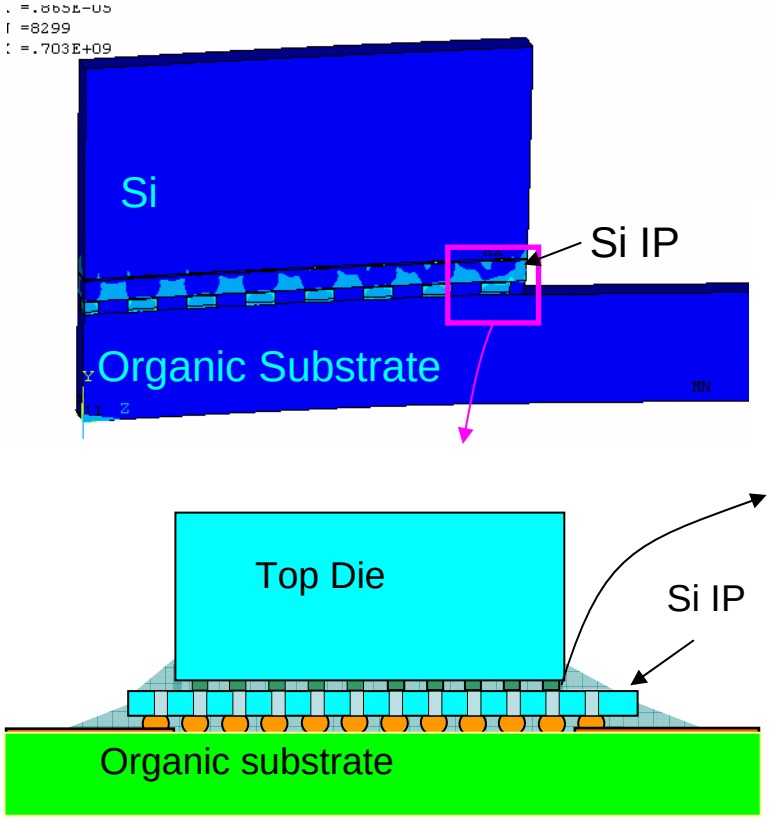
**Cu/Sn joint**

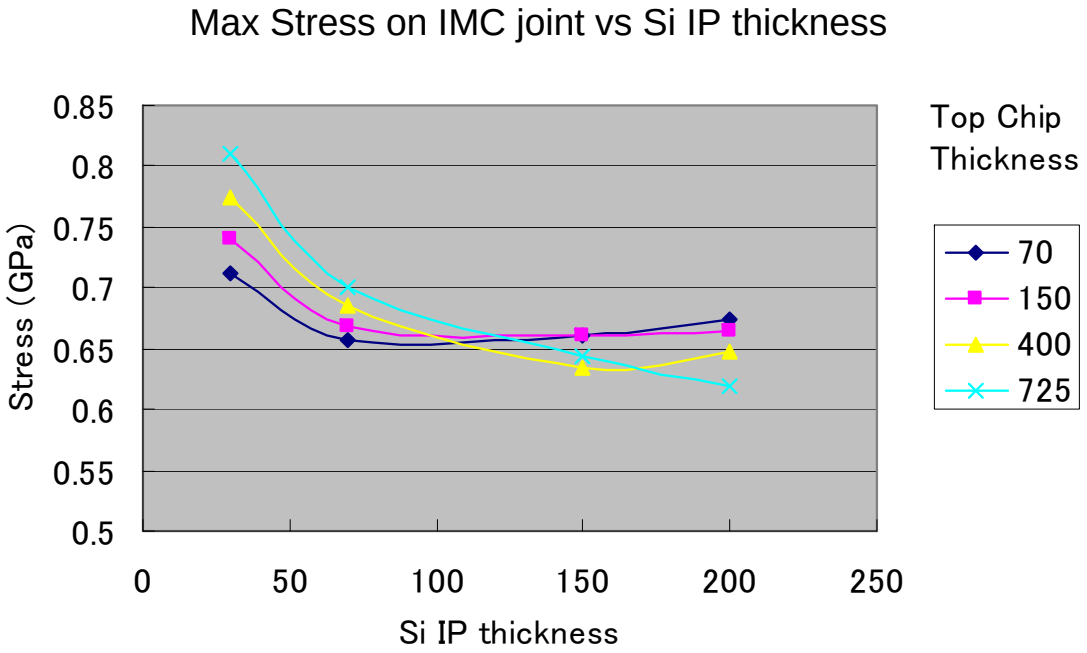



**Cu/Ni/In joint**



# Effect of Si thickness to the stress on the IMC joints

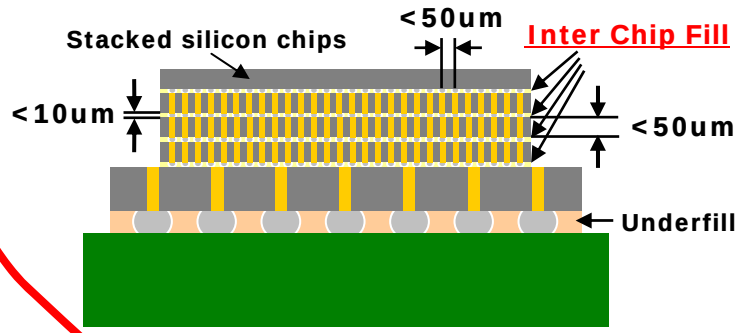


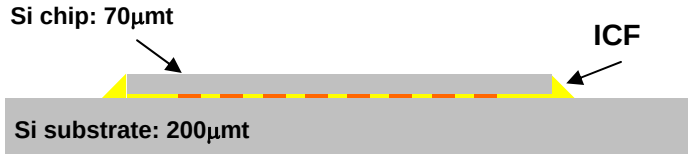



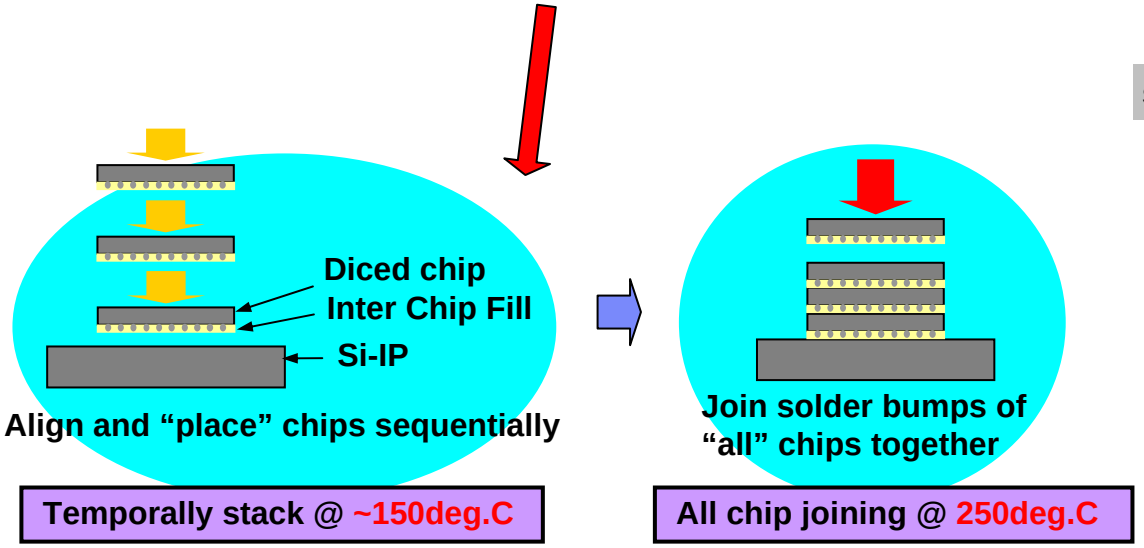

- The stress on the joints increases with decreasing Si IP thickness.
- The stress on the joints increases with increasing top Si chip thickness for thin Si IP, but the effect becomes less significant as the Si IP thickness increases.

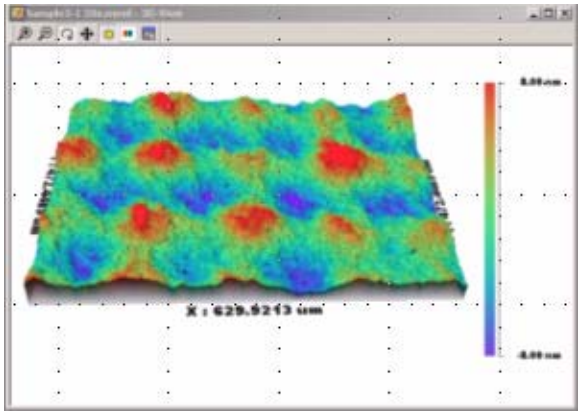
# Future Underfill Requirements for 3D-IC

- **New requirements for Inter Chip Fill**
  - **Higher thermal conductivity**
  - **Lower stress & high reliability**
    - ***Lower cure shrinkage***
    - ***Lower thermal expansion (low CTE)***
    - ***Not high modulus (for stress reduction)***
    - **High insulation and low ion content**
  - **Good 3D chip assemble capability for many-layers stack**
    - ***Stack Joining process (Patented)***



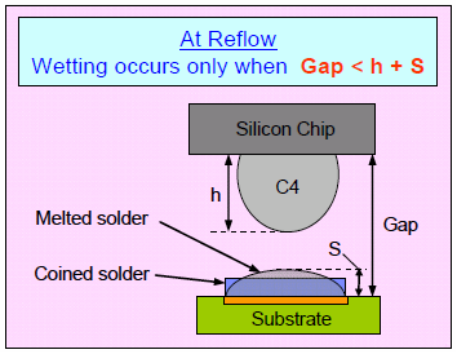



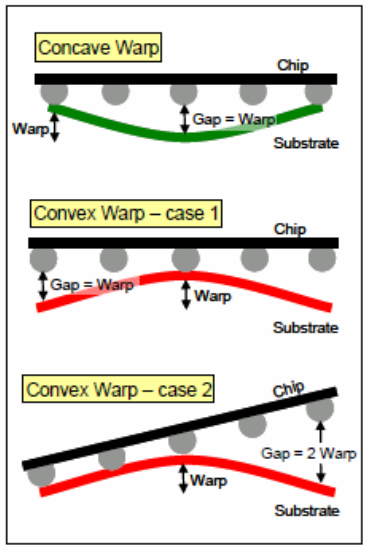



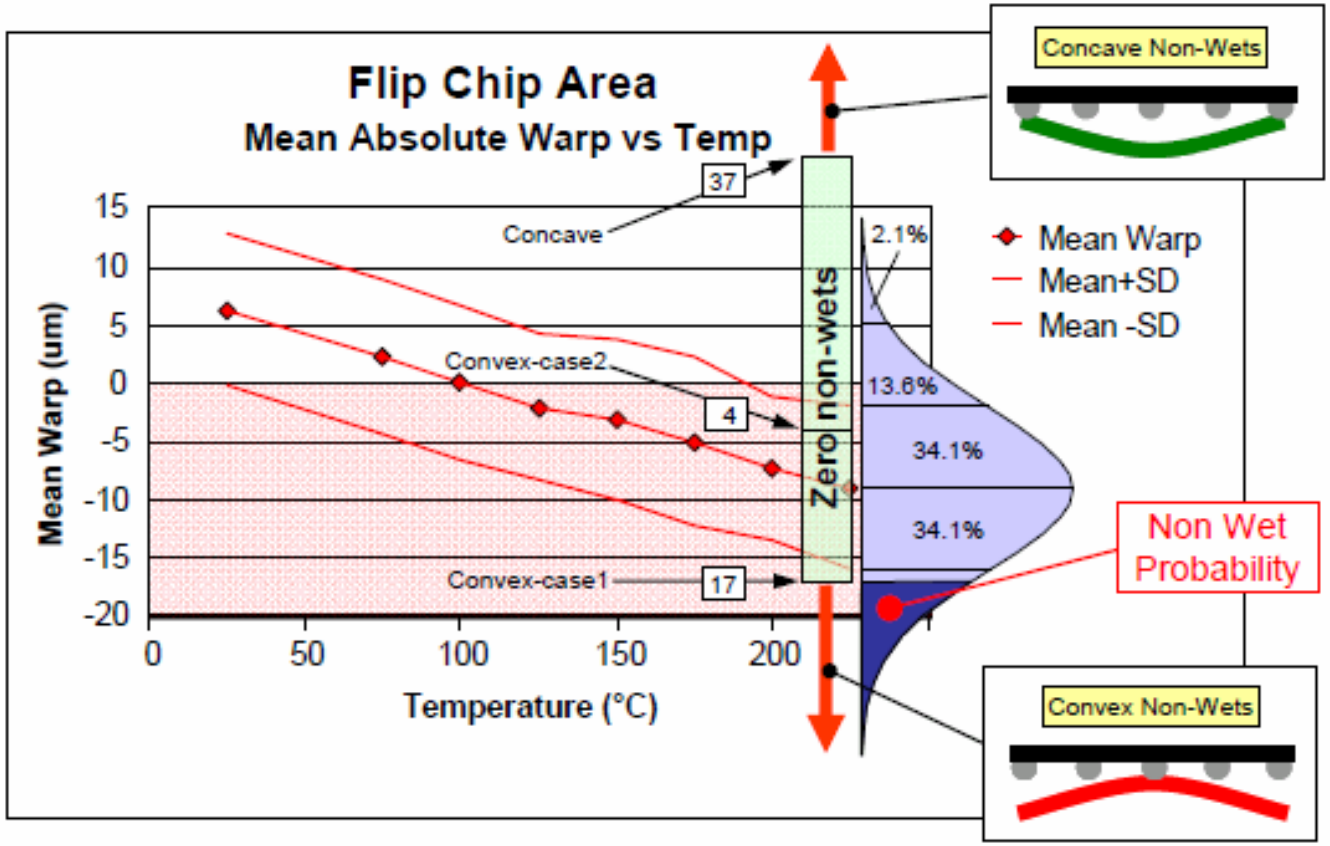
***Resin shrinkage has serious effect on device performance of thin silicon chip.***

# Organic Substrate: Warp Projection Tool

- **C4 Non-Wets in the chip attach process occurs due to the warpage of an organic substrate.**




Khanna et al, ECTC 2010.

- **The warpage of an organic substrate can be predicted based on the circuit design.**

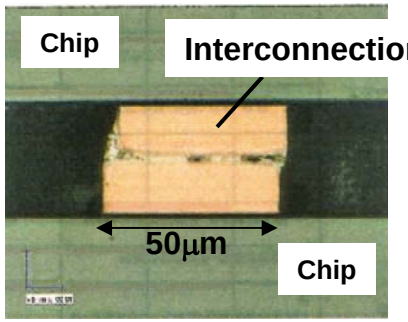
- **SEM-DICM can detect the fine pitch interconnection displacement with 0.02μm resolution.**

**Ex. Measured displacement of 100μm pitch interconnection by laser microscope DICM**

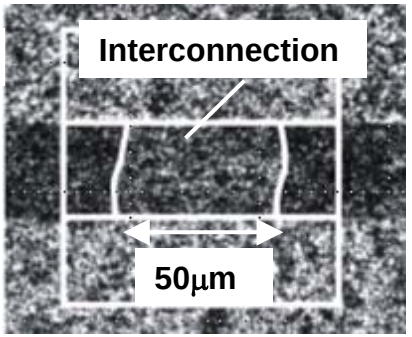
**Types of DICM (Digital Image Correlation Method)**

| | Conventional | Laser Microscope, SEM |
|---|---|---|
| Resolution (μm) | 1 | 0.02 - 0.05 |

- We are aiming to detect the displacement of 10μm pitch interconnection.

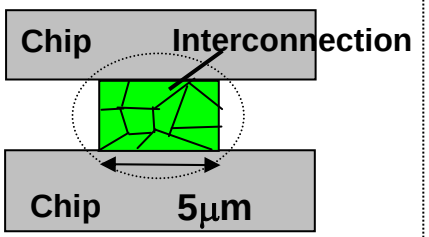



**Microscope photo of cross-section**



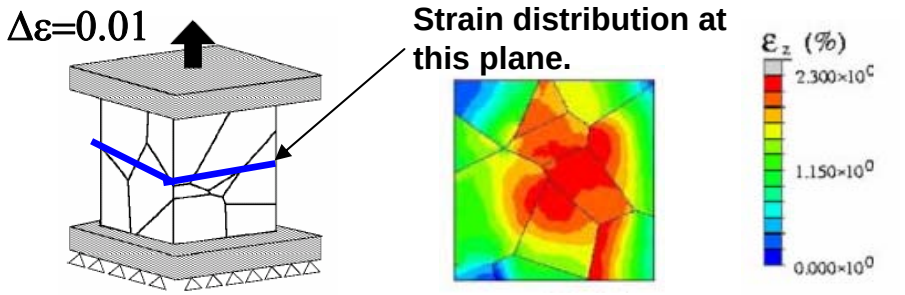

**Shaded cross-section for DICM**

- **Crystal orientation in fine pitch interconnection may have an impact on the reliability.**
  - The number of crystals in 10μm pitch interconnection is only 10-20.
  - Strain distribution may be dependent on the crystal orientation.



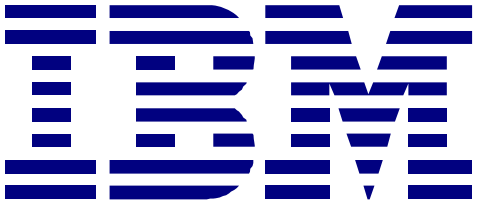

10μm pitch interconnection

**Ex. Simulated strain distribution, considering the orientation of 20 crystals.**




- High strain area reaches the outer surface and when a crack exists here, the interconnection can fail immediately.

Miyazaki et al., Material & Mechanics Conference 2010, The Japan Society of Mechanical Engineering
Kitamura et al., http://cyber.kues.kyoto-u.ac.jp/research%20activities/research%20activities.html



# Thank for your attention.

# Advanced Packaging and 3D Technologies

## ～Packaging Technology～

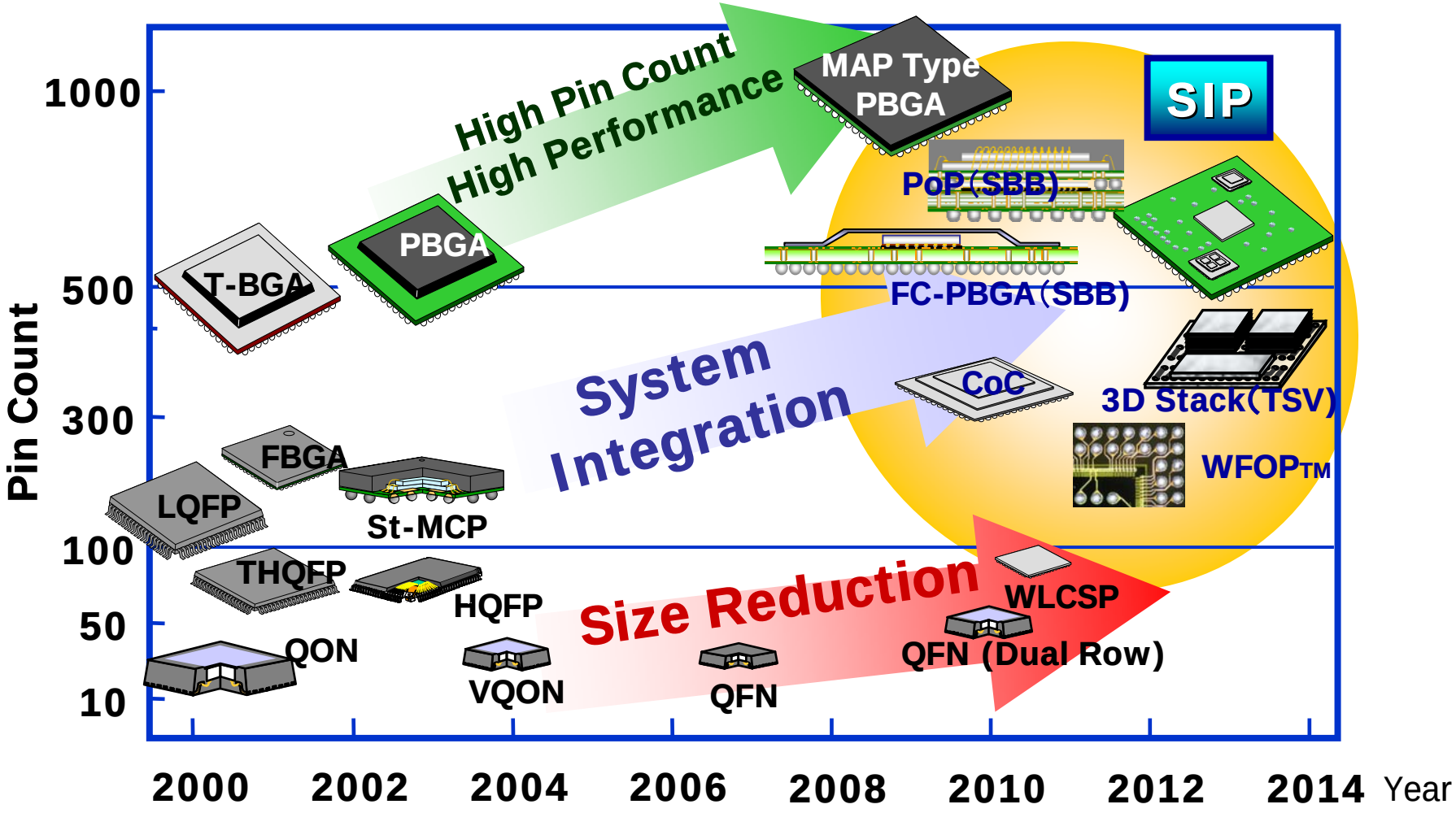
J DEVICES

YOICHI HIRUTA

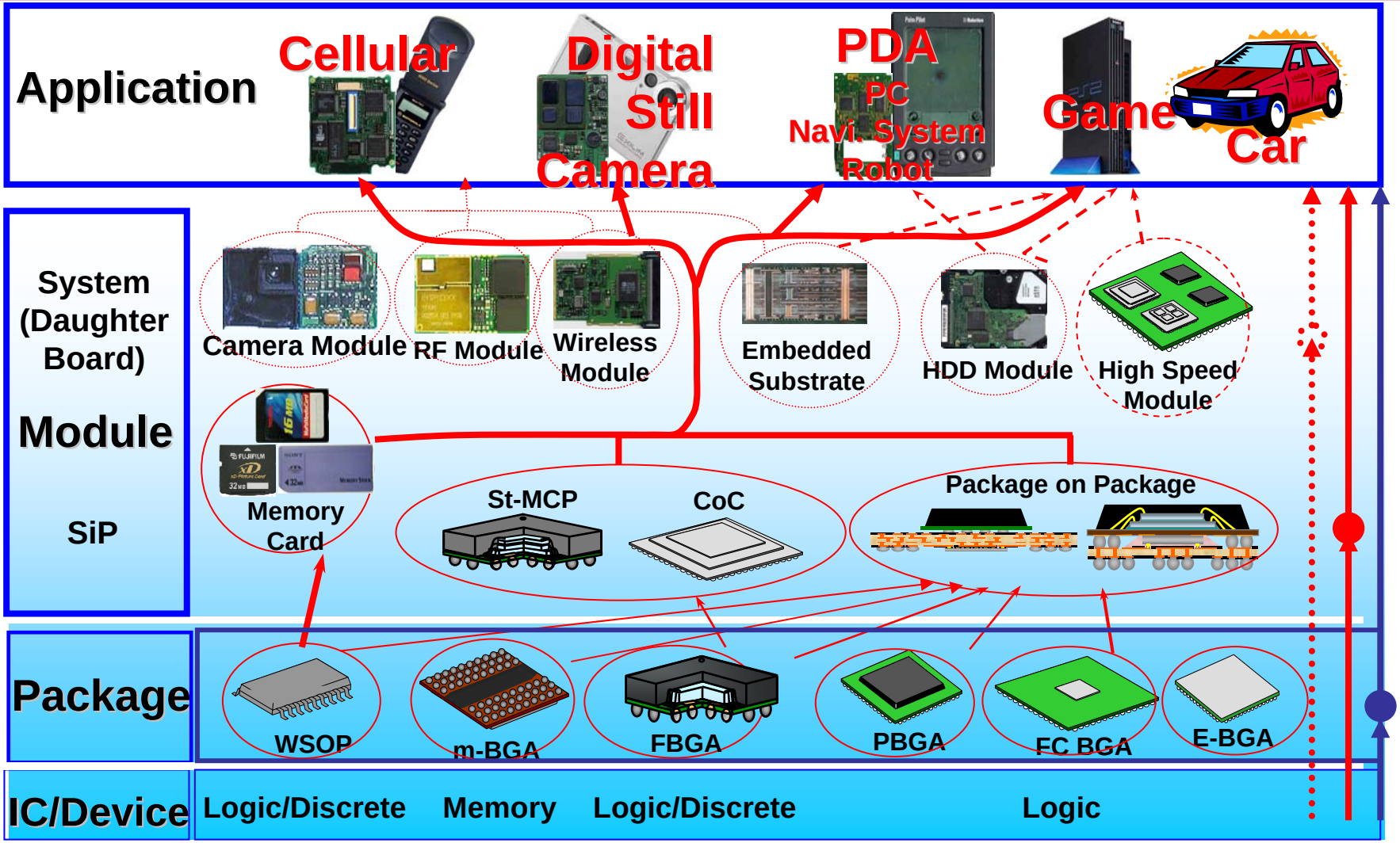
http://www.j-devices.co.jp

Feb. 28, 2011

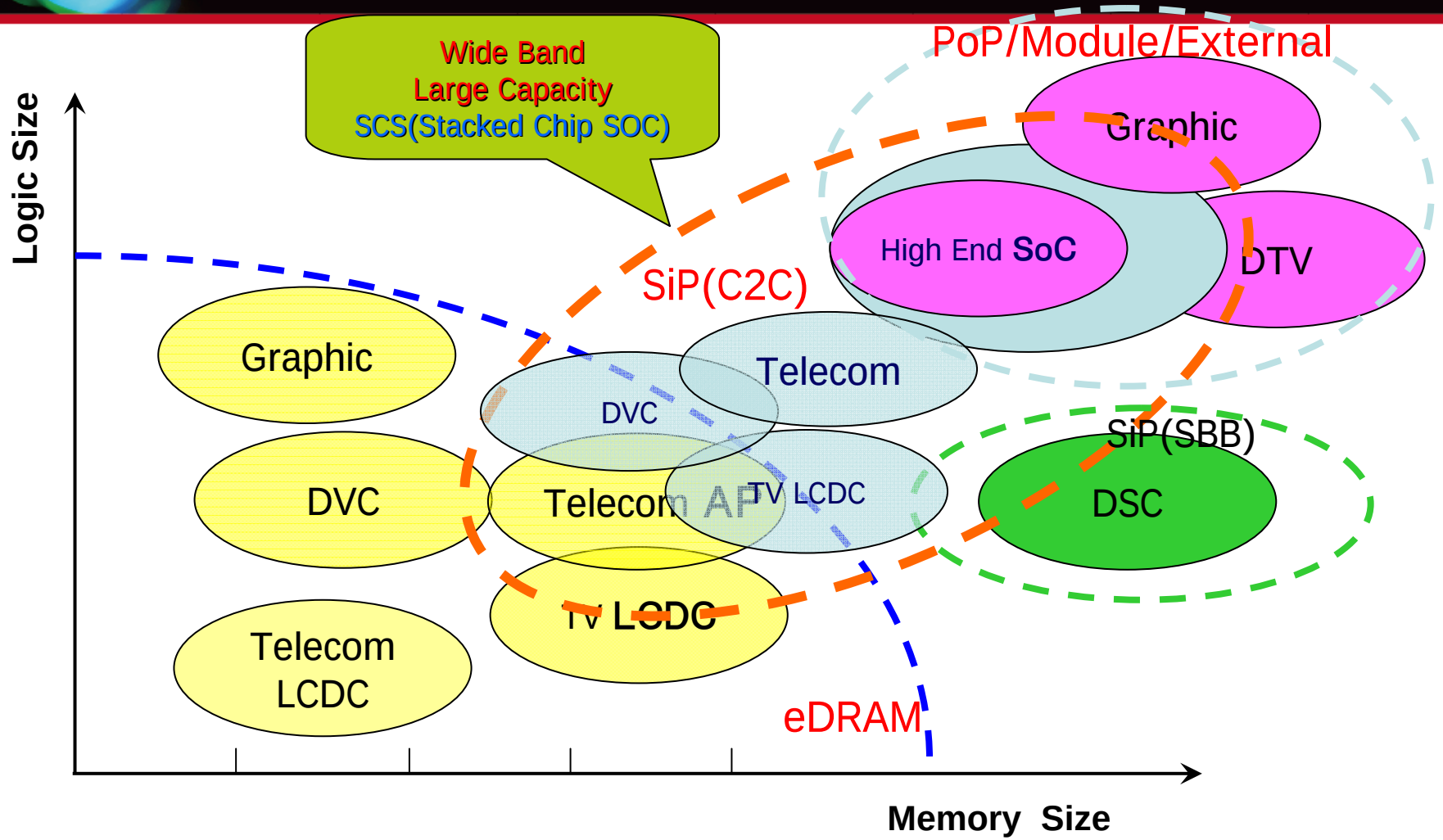
# Package Roadmap



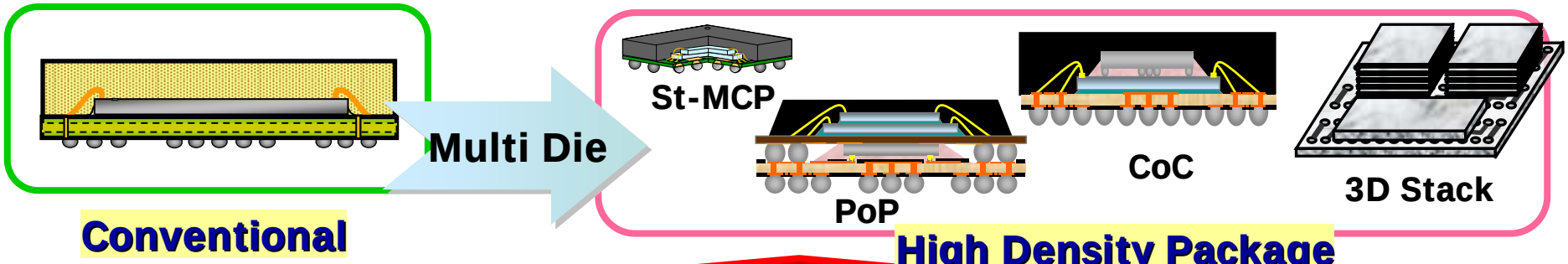
# Hierarchy


Application
Cellular
Digital Still Camera
PDA
PC
Navi. System
Robot
Game
Car
System (Daughter Board)
Module
SiP
Camera Module
RF Module
Wireless Module
Embedded Substrate
HDD Module
High Speed Module
Memory Card
St-MCP
CoC
Package on Package
Package
WSOP
m-BGA
FBGA
PBGA
FC BGA
E-BGA
IC/Device
Logic/Discrete
Memory
Logic/Discrete
Logic

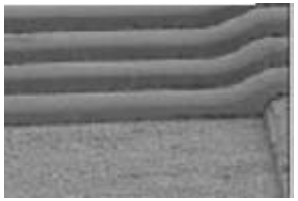
# Memory Assembly & System Application



# Assembly Technology for High Packing Density




## RDL



Fine Pitch RDL

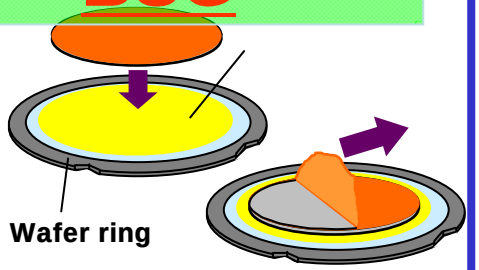
## μ Interconnect

Wire Bonding

Micro Bump interconnect

TSV

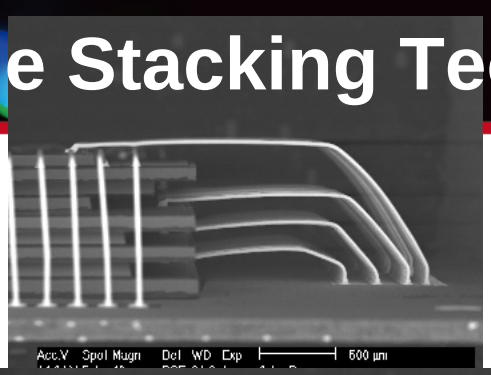
## BSG

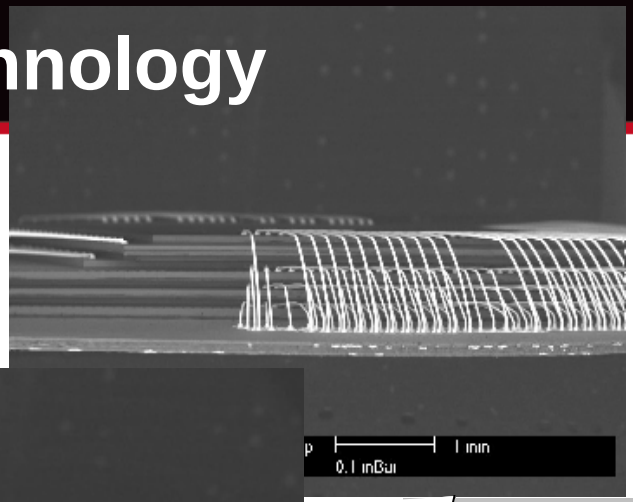


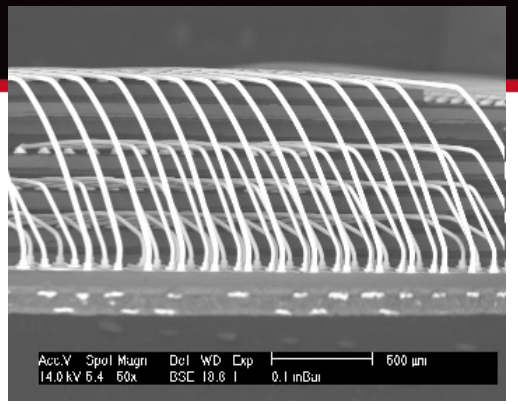

DBG(Dicing before Grinding)

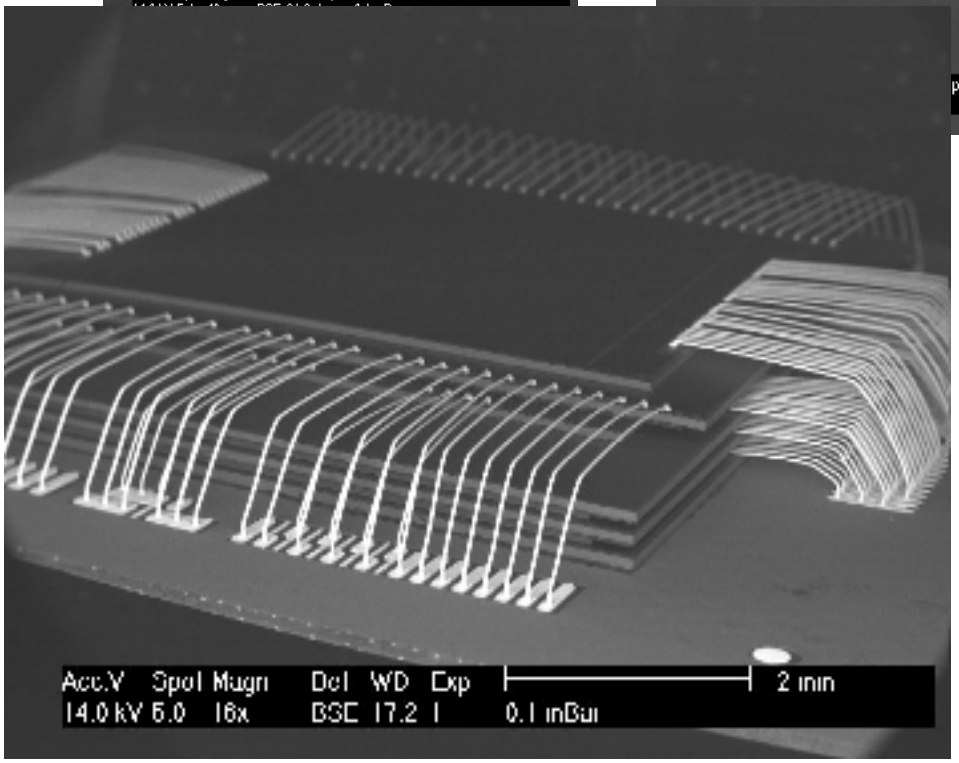
**Unit Process Activities**

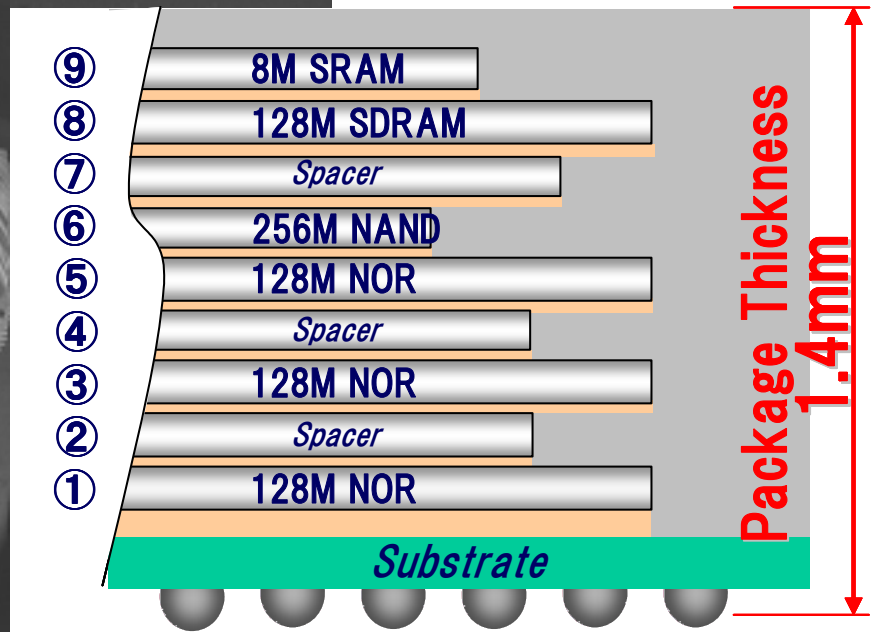
# Die Stacking Technology



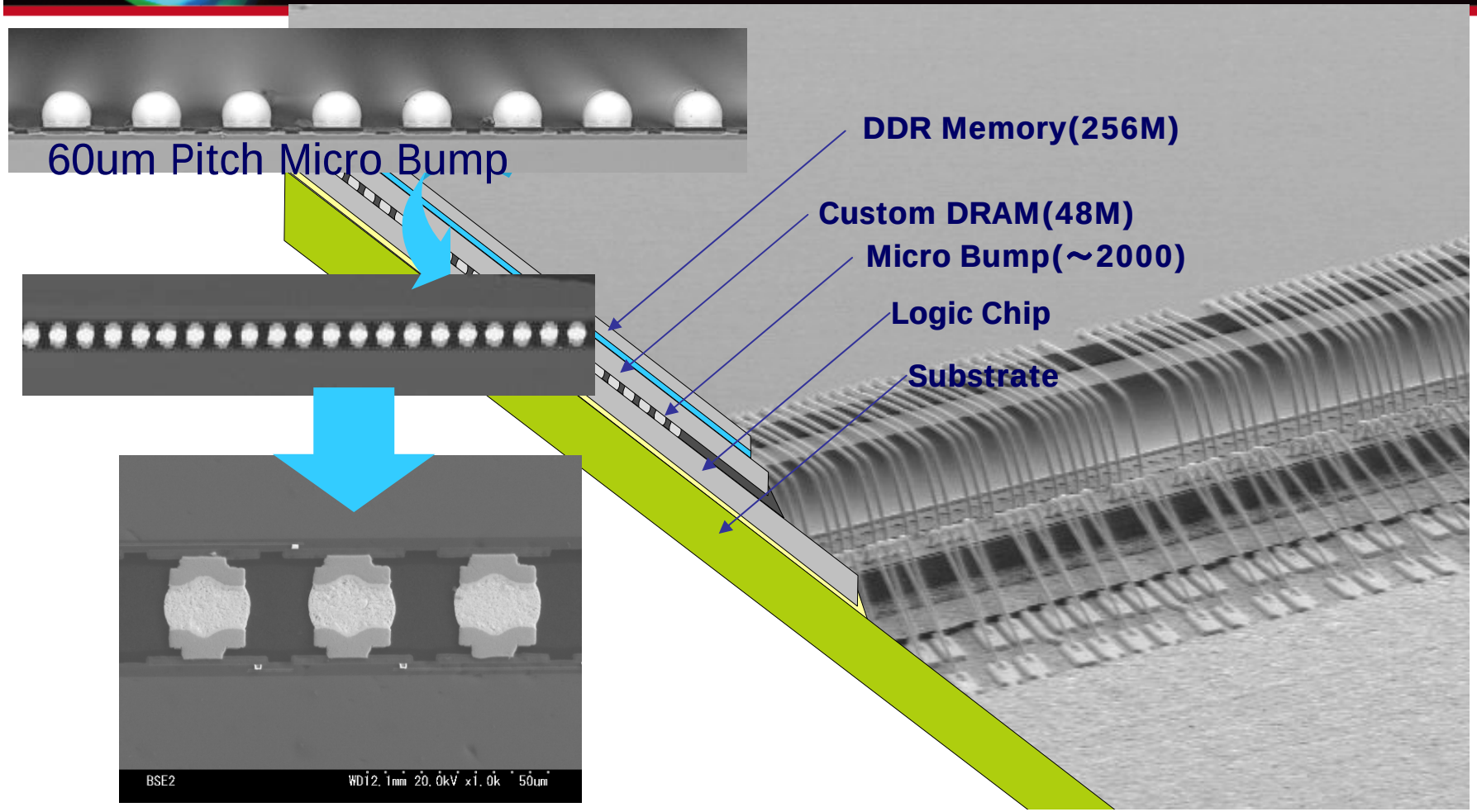






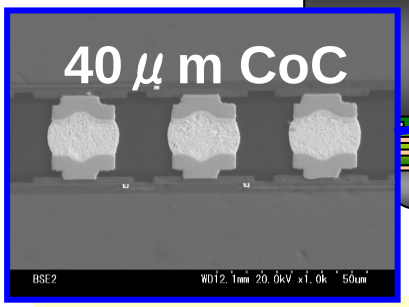



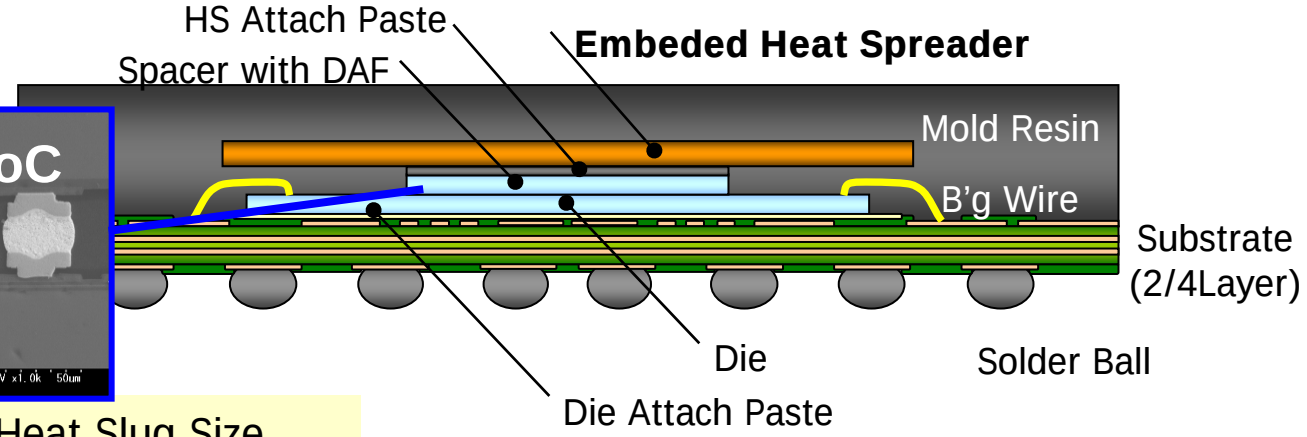
# Die Stacking Technology

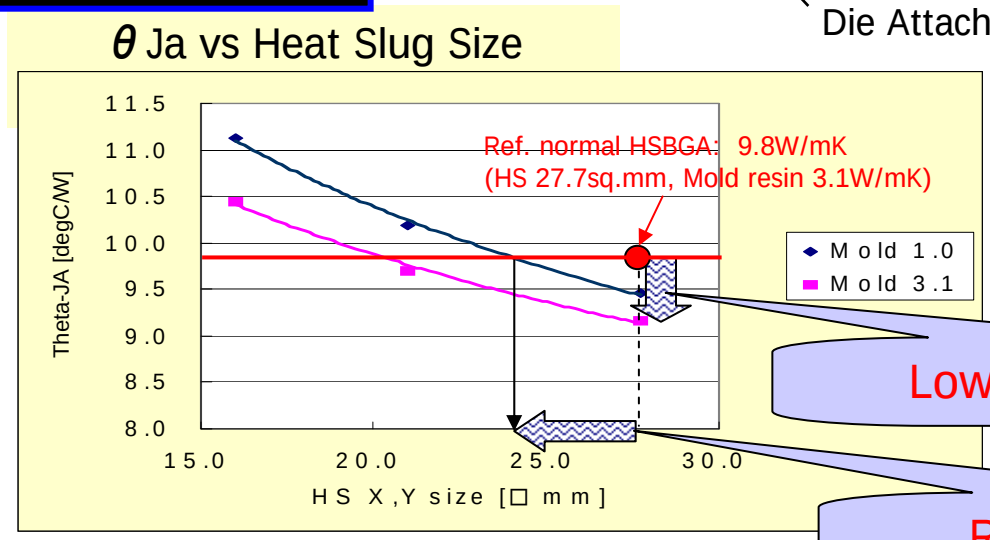


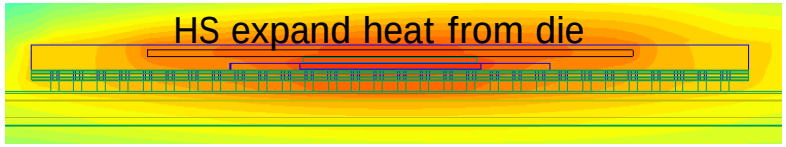

**Cross section of inter-connection**

# Highly Integrated BGA (Embeded HS & CoC Interconnect)




Lower θja @ Same mold resin

Reduce HS size @ Same θja

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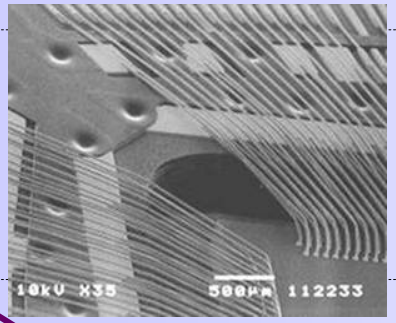
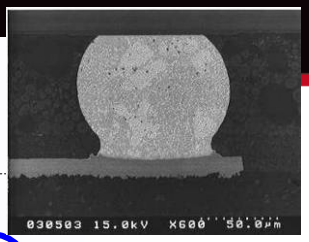
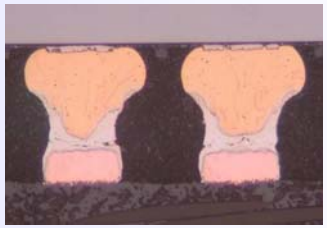
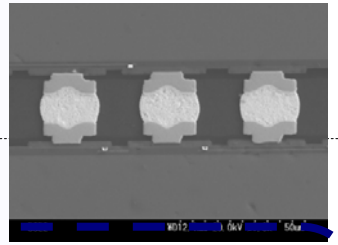
# Interconnection Roadmap





Pad Pitch[um]

200
150
50

250
C4
226
200
180
150

150
120
100
80
60
Wire Bonding
(US+Thermo-
compression)

120
Wire Bondhing
(US)

80
60
50
TAB

SBB (Stud Bump Bonding)
150
80
60
50
45
40
35
30

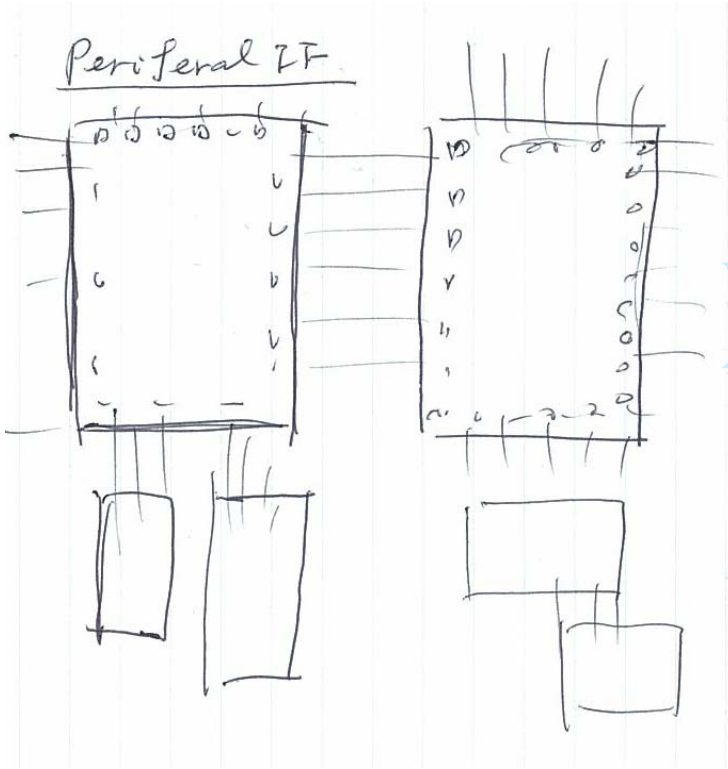
CoC
60
40
20
TSV

µ Interconnect

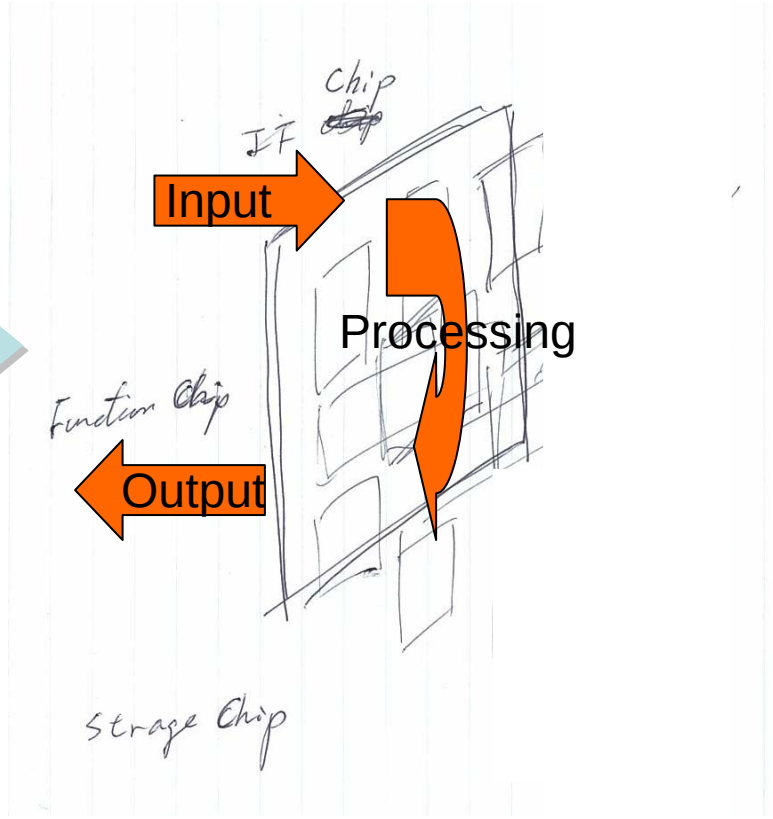
1990
1995
2000
2005
2010

# Design Issue in 3D

**Peripheral I/F**

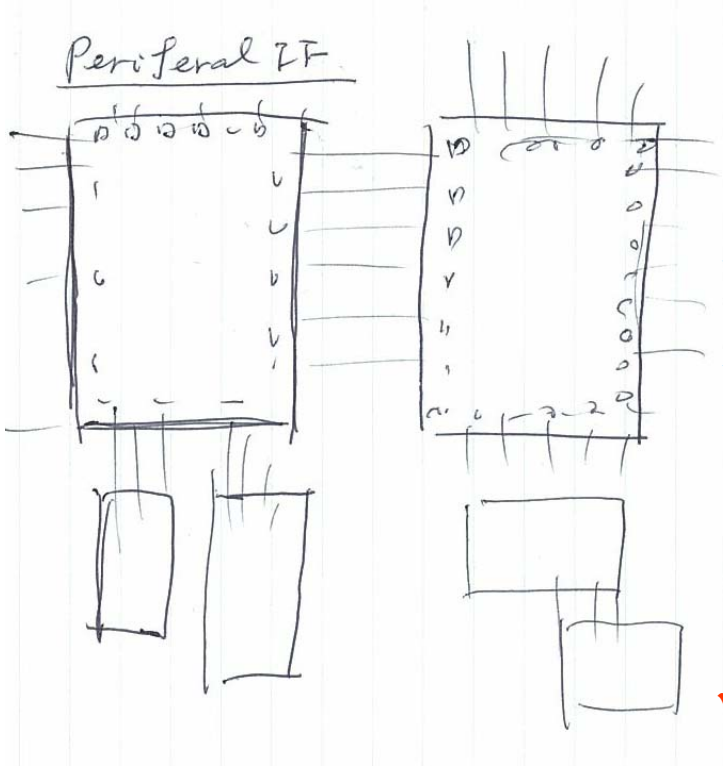



**2D I/F**

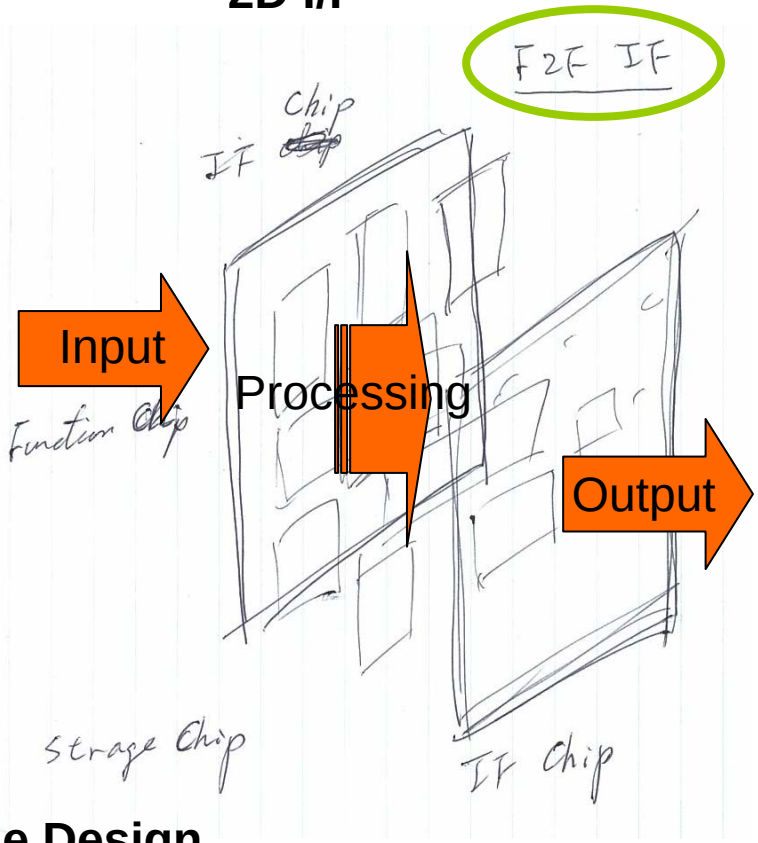


# Design Issue in 3D

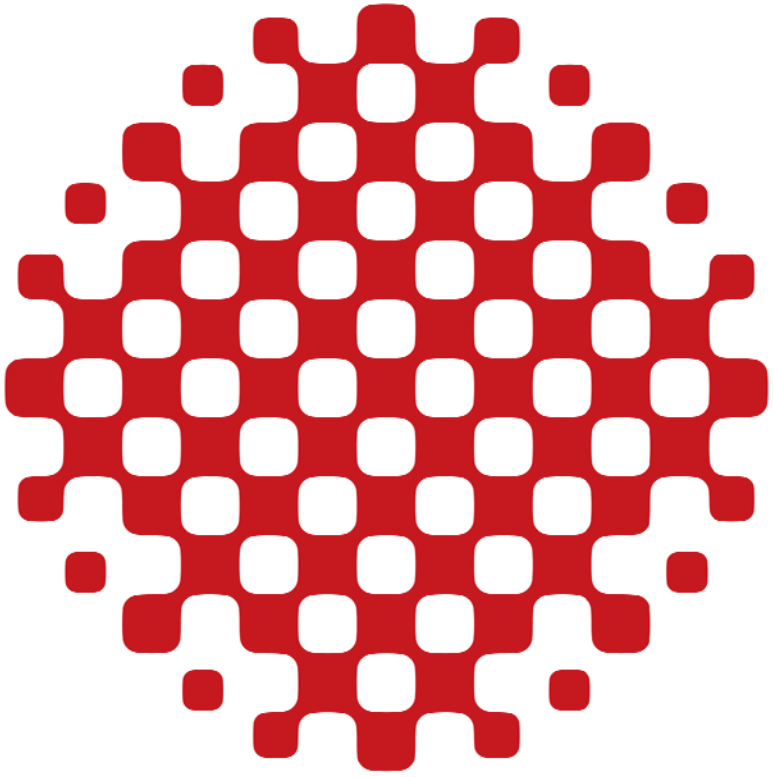
**Peripheral I/F**




**2D I/F**




- ✓**Floor Plan**
- ✓**Optimizing the Design**
- ✓**Linkage with Packaging**



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INVENTIVE

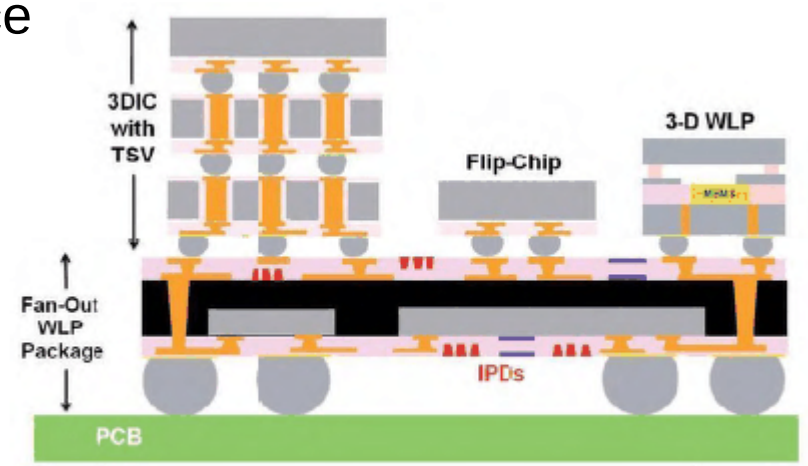
# ASP-DAC 2011 Panel Discussion: Advanced Packaging and 3D Technologies

Chris Cheung
Engineering Director
Silicon-Package-Board
Cadence Design Systems

Jan 28, 2011

# Challenges in 3D-IC & Packaging Design

- Mixed Technologies
  - Flip chip, Wire bond, stacked (face to face) or Side by side, with or without Silicon Interposer, SiP (System in Package), PoP (Package-on-Package)
  - Digital vs Mixed Signal designs
  - Net list, Physical Implementation (DRC and manufacturing requirements)
  - Electrical, Power and Thermal Analysis




Overall Tool-box solution for 3D Packaging
*(Source Yole Developpement)*



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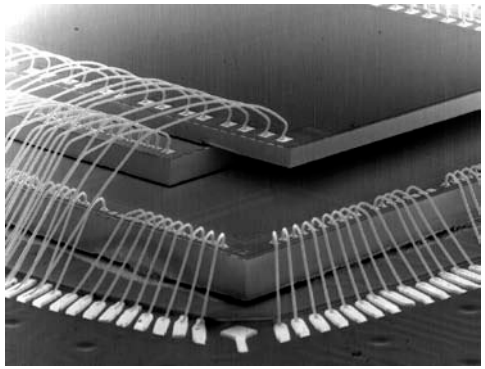
# Challenges in 3D-IC & Packaging Design

- Multiple factors to consider in today's Product Design
  - Chip set proliferation may require a "reference board" design
    - Ease of adoption
    - Reference guide
  - Time to market pressure may influence your design choice
    - Buy (or re-use) vs "Start from scratch"
  - True cost and performance has to take a system view
    - Chip, Package and Board
- "Distributed" Design
  - Teams may be at different locations and time zones
  - Co-Planning / Co-Design / Co-Analysis
  - Manage data exchange (Between design teams, vendors)

# Technologies at Cadence: "Prototyping for 3D Packaging"

- The ability to view and prototype the entire product (chip, package and/or board) in an "integrated" environment.
- For rapid prototyping one must be able to optimize chip, package and board for routability and layer utilization, constraint budgeting across the design fabrics.
  - Signal traversed through the entire "system", thus delay has to be measured from chip to chip.
  - Consider different design options to identify a design choice or at least narrow down to couple options for further analysis
  - An interesting application may be "RFQ" (Request for Quote)

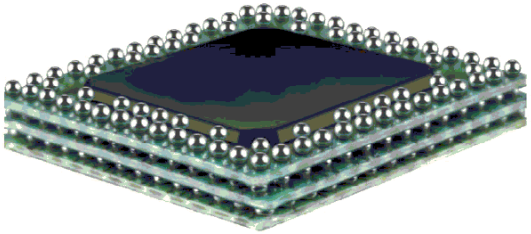
# Technologies at Cadence: "Prototyping for 3D Packaging "



- Results from prototype may be disseminated to design teams for implementation
  - Net lists, constraints, stack-ups, "rough" physical layouts
  - Data flows from prototype into design tools
- ECO Management
  - Be able to resolve design conflicts or changes during implementation phase
- Final Design Verification
  - Does your final design met the original specification?
  - Cost analysis

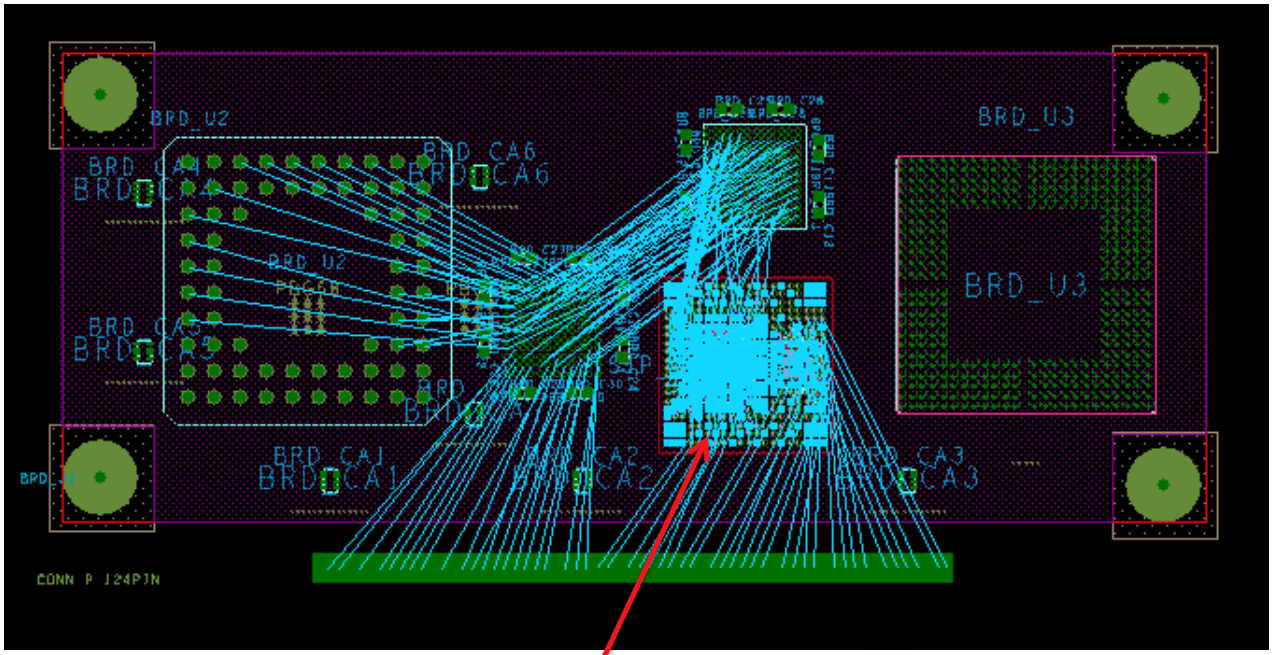
# Technologies at Cadence: Considerations in “3D Packaging Prototype”

- Obviously: Planar and 3D viewing of the design
  - Picture worth a thousand words
- For Prototyping to be effective, all design fabrics must be integrated into the same environment
  - One tool, one window and one UI
  - Each fabric must maintains its own net list, substrate layers and design units, design rules.
- Prototype system must integrate seamlessly with design tools
  - Who is the typical owner of the prototype?
  - Support distributed design teams



# Idea to Reality?

- Example of a reference board with a co-design package + co-design die. The board contains additional standard parts.
- Flight lines showing possible routing congestions, results of net assignments and placement.




Co-Design Package + Chip



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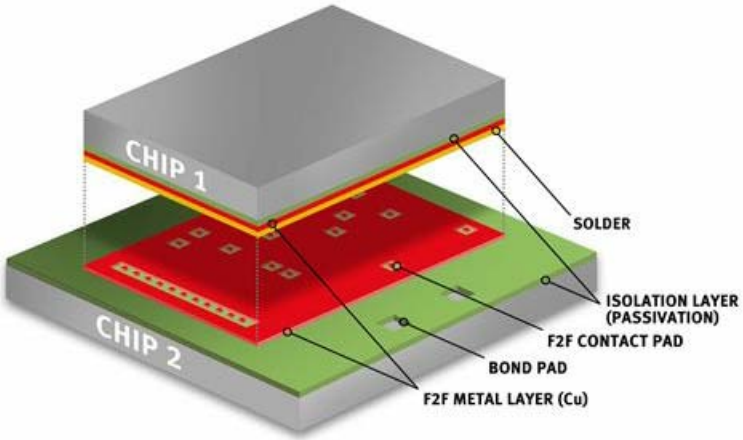
# Future of 3D Packaging …

- EDA company's goal is to provide solutions for electronic designs
  - EDA company must listen to and understand customers' needs
  - EDA company must provide leading edge solutions
  - EDA company need to partner when a solution requires multiple technology disciplines
- We are here to listen!



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