Call for Papers
ASP-DAC 2011

Asia and South Pacific Design Automation Conference 2011

http://www.aspdac.com/aspdac2011/

January 25-28, 2011

Yokohama, Japan

Aims of the Conference:

ASP-DAC 2011 is the sixteenth annual international conference on VLSI design automation in Asia and South Pacific region, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:

Original papers on, but not limited to, the following areas are invited. Please note that ASP-DAC will work cooperatively with other conferences and symposia in the field to check for double submissions.

Paper Submission Deadline:
July 19, 2010, 5:00 PM JST (GMT +09:00)

[1] System-Level Modeling and Simulation/Verification:
System-level modeling, specification, language, performance analysis, system-level simulation/verification, hardware-software co-simulation/co-verification, etc.

[2] System-Level Synthesis and Optimization:
System-on-chip and multi-processor SoC (MPSoC) design methodology, hardware-software partitioning, hardware-software co-design, IP/platform-based design, application-specific instruction-set processor (ASIP) synthesis, low power system design, etc.

[3] System-Level Memory/Communication Design and Networks on Chip:
Communication-based architecture design, network-on-chip (NoC) design methodologies and CAD, interface synthesis, system communication architecture, memory architecture, low power communication design, etc.

[4] Embedded and Real-Time Systems:
Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues.

[5] High-Level/Behavioral/Logic Synthesis and Optimization:
High-Level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, and synthesis.

[6] Validation and Verification for Behavioral/Logic Design:
Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL and gate-level modeling and validation, assertion-based verification, coverage-analysis, constrained-random testbench generation.

[7] Physical Design:
Floorplanning, partitioning, placement, buffer insertion, routing, interconnect planning, clock network synthesis, post-placement optimization, layout verification, package/PCB routing, etc.

[8] Timing, Power, Thermal Analysis and Optimization:
Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis, etc.

[9] Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, high-frequency and electromagnetic simulation of circuits, etc.

[10] Design for Manufacturability/Yield and Statistical Design:
DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics, etc.

[11] Test and Design for Testability:
Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

[12] Analog, RF and Mixed Signal Design and CAD:
Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design considerations.

[13] Emerging technologies and applications

i. Design case studies for emerging applications: multimedia, consumer electronics, communication, networking, ubiquitous computing and biomedical applications, etc.

ii. Post CMOS technologies: nanotechnology, quantum, optical interconnect, 3D integration, probabilistic architecture, microfluidics, molecular, bioelectronics, etc., with emphasis on modeling, analysis, novel circuit/architecture, CAD tools, and design methodologies.

ASP-DAC 2011 University LSI Design Contest encourages submitting original papers on LSI design and implementation at universities and other educational organizations.

Submission of Papers:

Deadline for submission:	**5 PM JST (GMT+9)**	**July 19 (Mon.), 2010**
Notification of acceptance:		**Sept. 24 (Fri.), 2010**
Deadline for final version:	**5 PM JST (GMT+9)**	**Nov. 15 (Mon.), 2010**

Specification of the paper submission format will be available at the WEB site:
http://www.aspdac.com/aspdac2011/

Panels, Special Sessions and Tutorials:

Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (e-mail: aspdac2011-sec@mls.aspdac.com) no later than June 7 (Mon.), 2010.

Prospective Sponsors:

ACM SIGDA, IEEE Circuits and Systems Society

ASP-DAC2011 Chairs:

General Chair: Kunihiro Asada(Univ. of Tokyo)
Technical Program Chair: Hyunchul Shin (Hanyang Univ.)

Contact:

Conference Secretariat: aspdac2011-sec@mls.aspdac.com
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