SAN DIEGO STATE UNIVERSITY

Equivalent Circuit Model Extraction for Interconnects in 3D ICs

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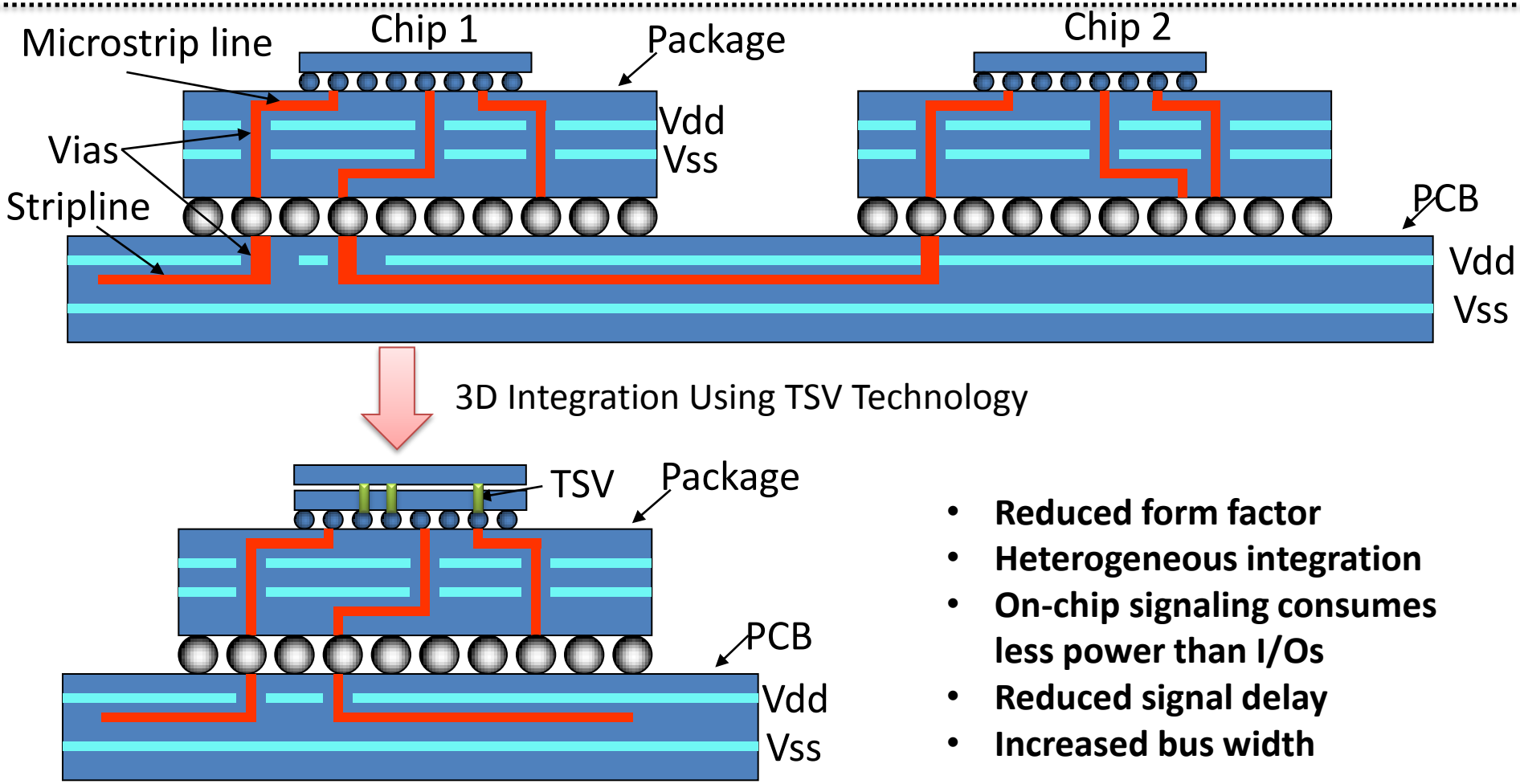
Outline

- 3D IC technologies
  - Power consumption & bandwidth
- Parasitic RC model extraction for through-silicon vias (TSVs)
  - Analytical modeling (circular TSVs)
  - Model fitting (arbitrary cross section)
  - RC curve fitting (including microbumps, RDLs, etc.)

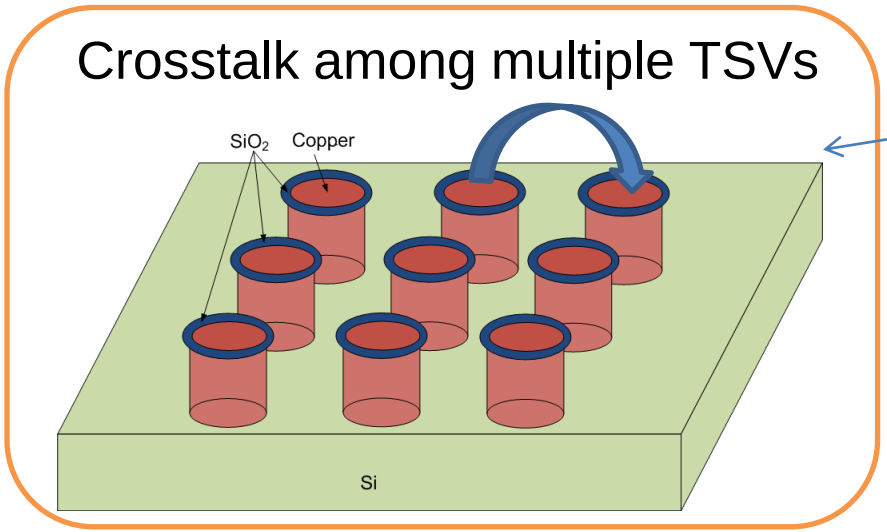
3D IC Integration

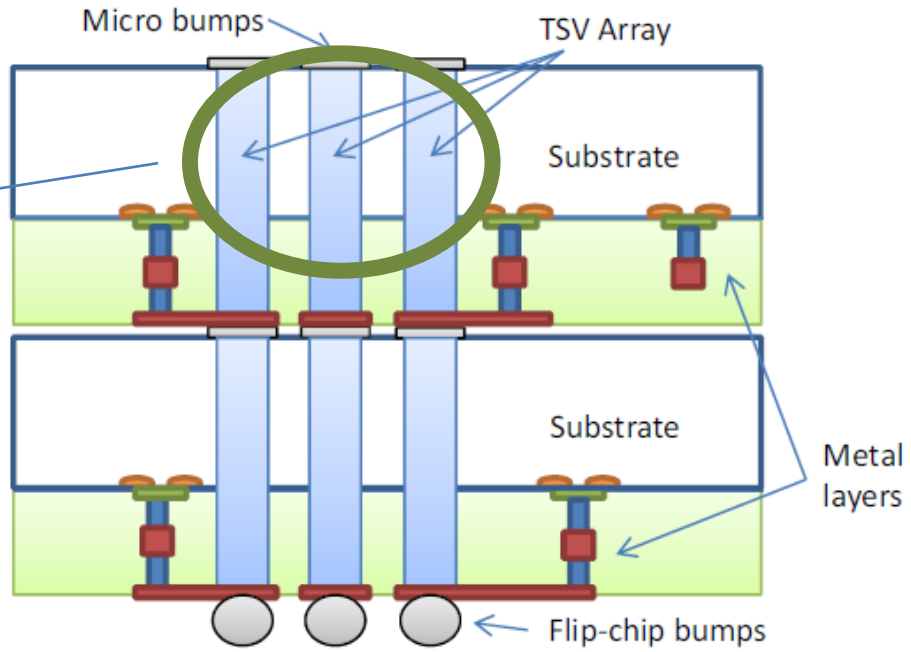


- **Reduced form factor**
- **Heterogeneous integration**
- **On-chip signaling consumes less power than I/Os**
- **Reduced signal delay**
- **Increased bus width**

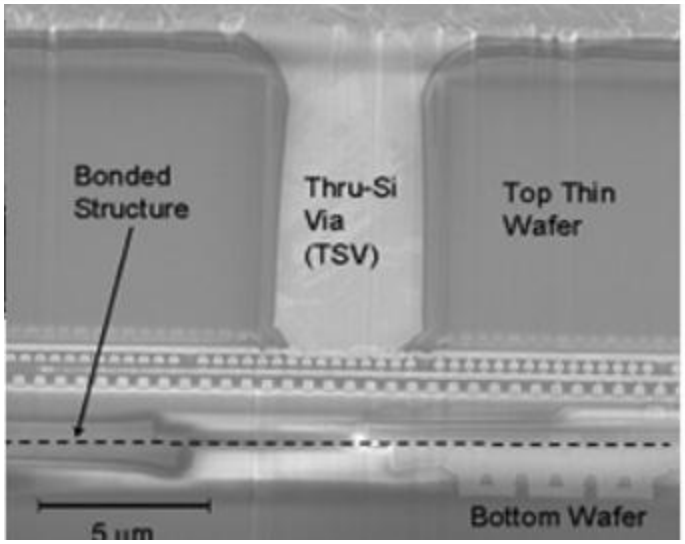
Electrical Design of TSVs

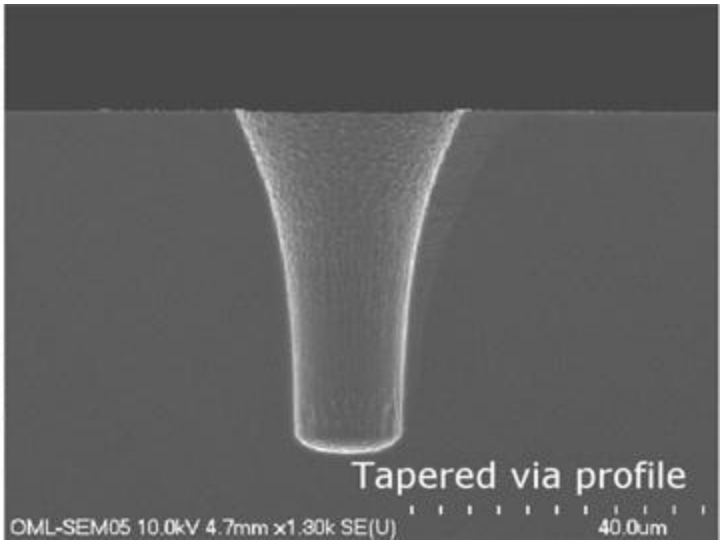
- TSVs are the major new components in 3D ICs.
- The parasitic capacitance, inductance, and resistance of a TSV will dictate its performance to improve power consumption and bandwidth.





Size Comparison of TSVs





Ref: Intel. T. Karnik D. Somasekhar S. Borkar, "Microprocessor system applications and challenges for through-silicon-via-based three-dimensional integration," IET 2011.

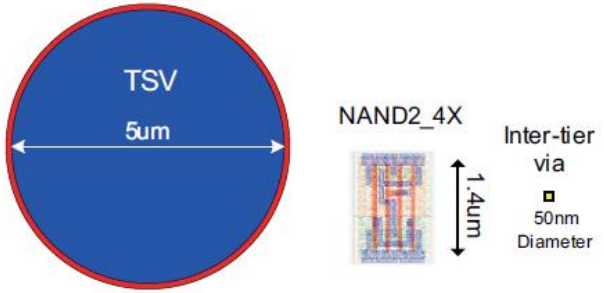
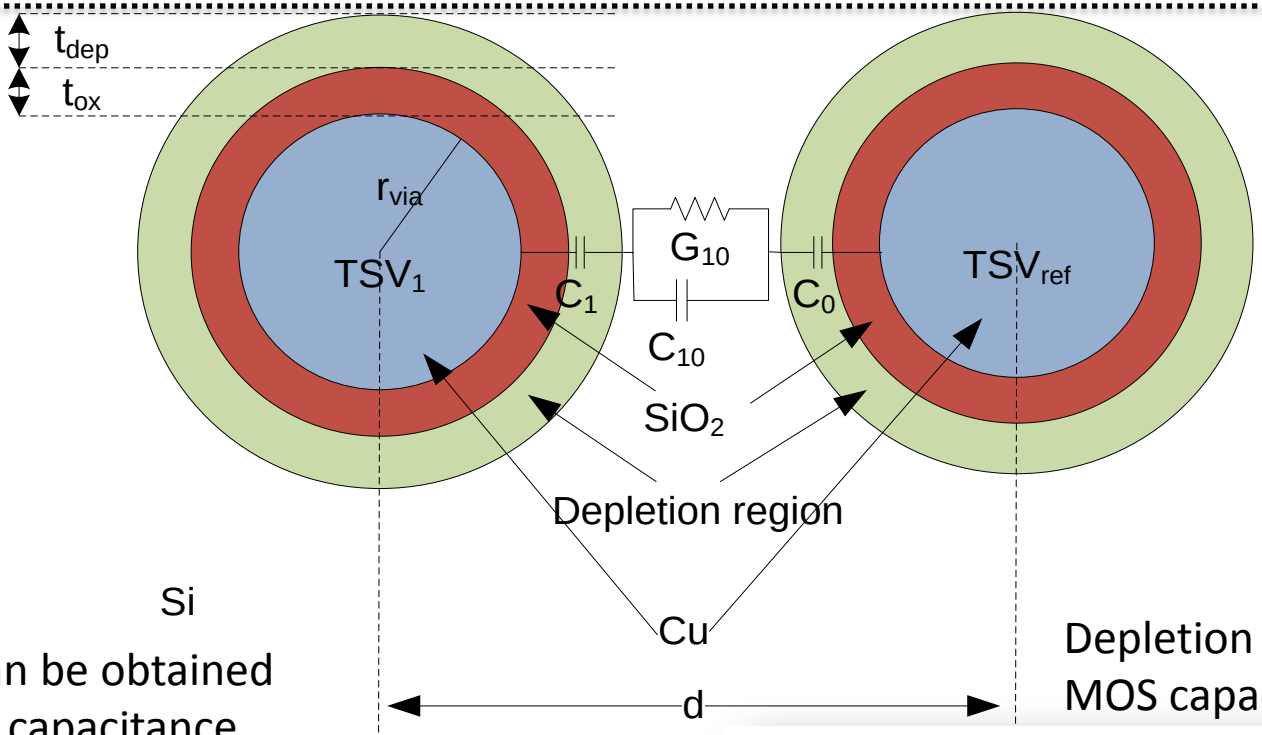


Fig. 2. Size comparison among a TSV, a gate, and an inter-tier via

Ref: Chang Liu and Sung Kyu Lim, "A Design Tradeoff Study with Monolithic 3D Integration," ISQED 2012

RC Model of a TSV Pair



G_{10} and C_{10} can be obtained from two-wire capacitance formulas.

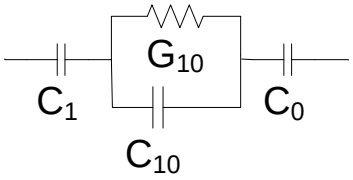
$$C_1 = \left(\frac{\ln\left(\frac{r_{via}+t_{ox}}{r_{via}}\right)}{2\pi\varepsilon_{ox}} + \frac{\ln\left(\frac{r_{via}+t_{ox}+t_{dep}}{r_{via}+tox}\right)}{2\pi\varepsilon_{Si}} \right)^{-1}$$

Depletion width (due to MOS capacitance):

$$\frac{4\varepsilon_{Si}kT}{q^2 N_a} \ln\left(\frac{N_a}{n_i}\right) = -0.5t_{dep}^2 - t_{dep}(r_{via}+t_{ox}) + (r_{via}+t_{ox}+t_{dep})^2 \ln\left(\frac{r_{via}+t_{ox}+t_{dep}}{r_{via}+t_{ox}}\right)$$

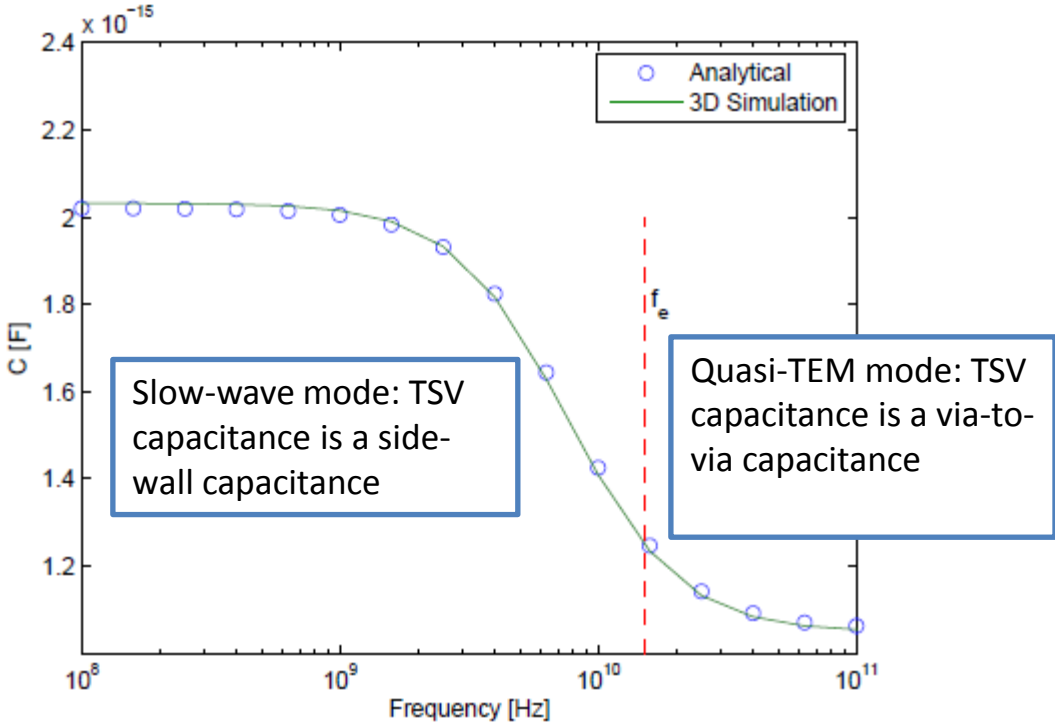
Slow-Wave to Dielectric Quasi-TEM Mode Transition

$$G_{10} = C_{10}\frac{\sigma_{Si}}{\varepsilon_{Si}}$$



At low frequencies, the wave propagation will be in slow-wave mode:

- Magnetic field is not affected by the presence of the lossy silicon, hence the loop inductance is same as if the two vias were in free space.
- Capacitance, however, is a side wall capacitance defined by the gate-oxide thickness and depletion widths, since silicon behaves more as a lossy conductor than a dielectric.

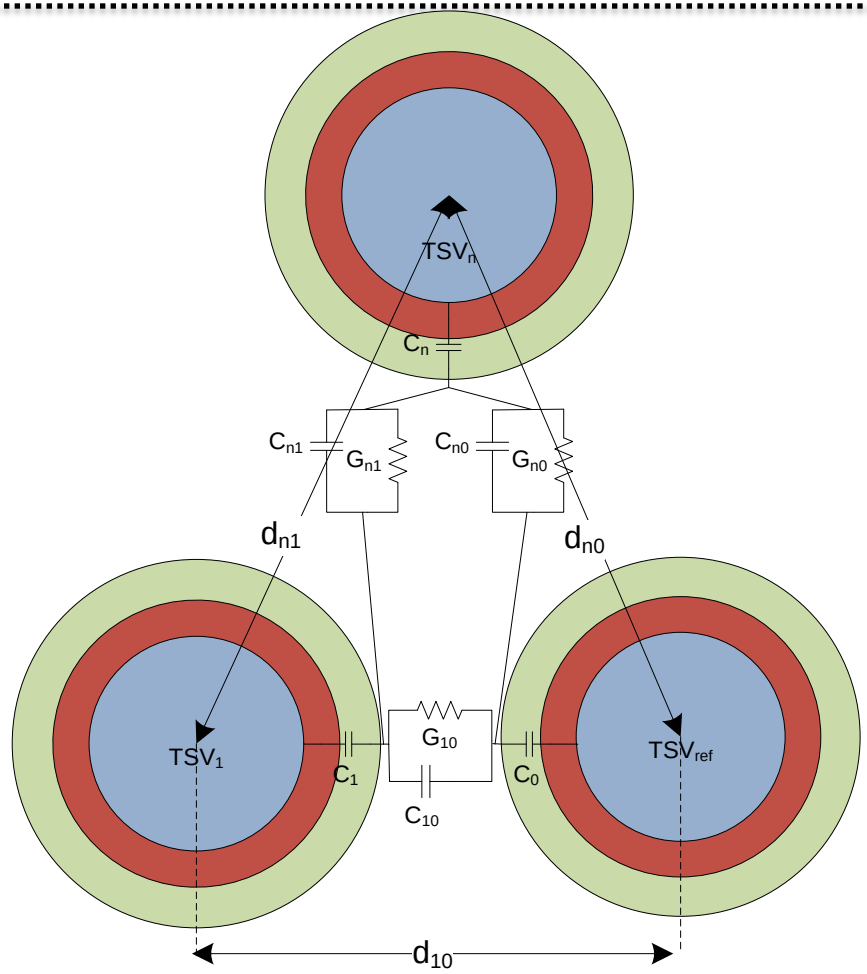


Transition frequency: $f_e = \frac{\sigma_{Si}}{2\pi\varepsilon_{Si}}$

$r_{via} = 1\mu\text{m}, t_{ox} = 0.5\mu\text{m}, t_{dep} = 0.74\mu\text{m}, d = 10\mu\text{m}, \varepsilon_{Si} = 11.9\varepsilon_0, \varepsilon_{ox} = 3.9\varepsilon_0, \sigma_{Si} = 10\text{S/m}$

Capacitance and Conductance of Coupled TSVs

- Consider that there are other TSVs in the vicinity of the original TSV pair.
- The presence of other TSVs do not affect the side-wall capacitances Ci, however the capacitances through the Silicon layer Cij change in the presence of other TSVs.
- Hence, the formulas for a single TSV pair cannot be applied for this configuration. The full coupled TSVs need to be simultaneously considered.



Multi-Conductor Transmission Line Model

- This is a general coupled TSV model similar to the representation of a multiconductor transmission line in terms of its per unit length parameters.

Capacitance and conductance matrix:

$$\overline{\overline{C}} = \mu_0 \varepsilon_{Si} \overline{\overline{L}}^{-1}$$

$$\overline{\overline{G}} = \mu_0 \sigma_{Si} \overline{\overline{L}}^{-1}$$

Inductance matrix:

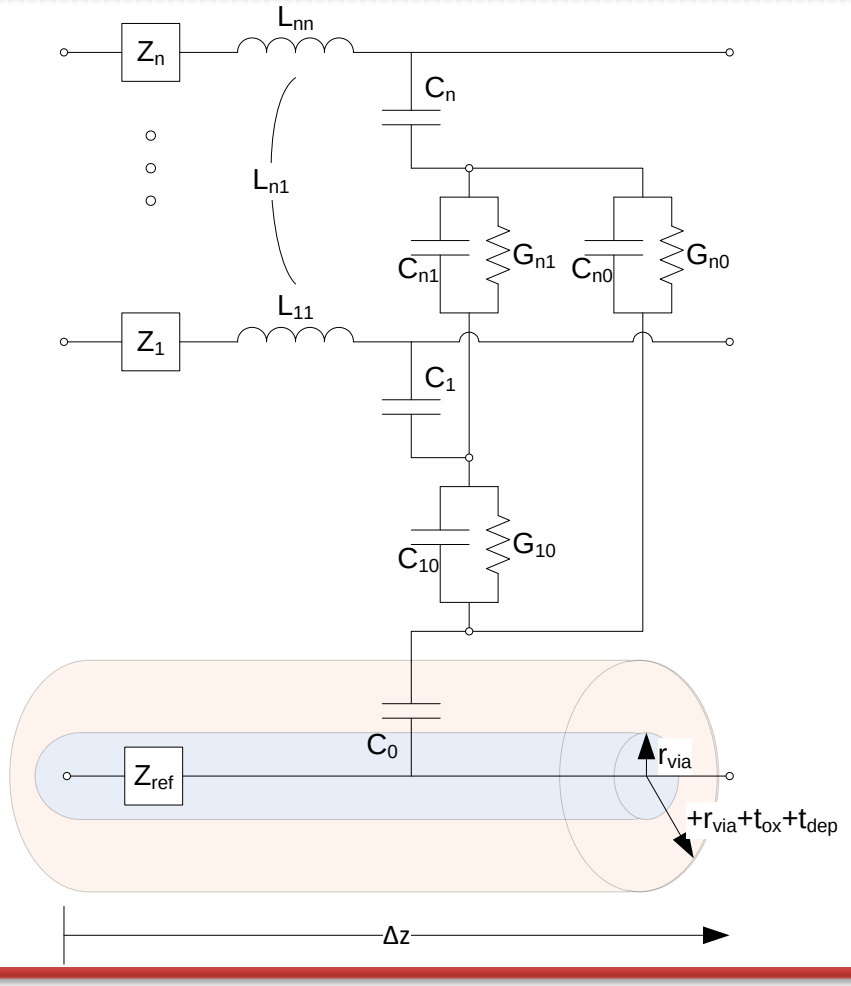
$$L_{ii} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0}^2}{r_i r_0}\right)$$

$$L_{ij} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0} d_{j0}}{r_0 d_{ij}}\right)$$

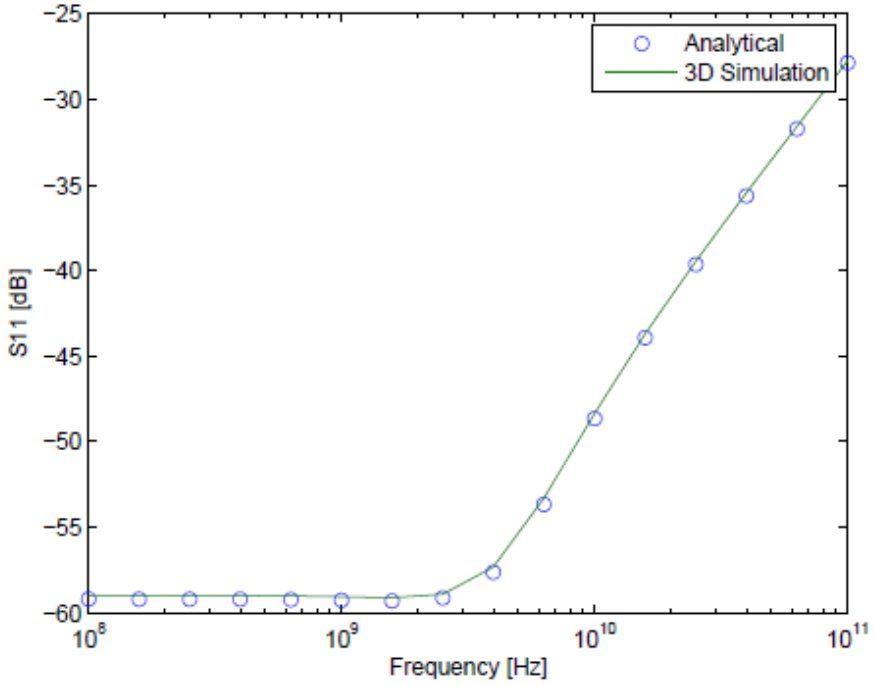
$$r = r_{via}$$

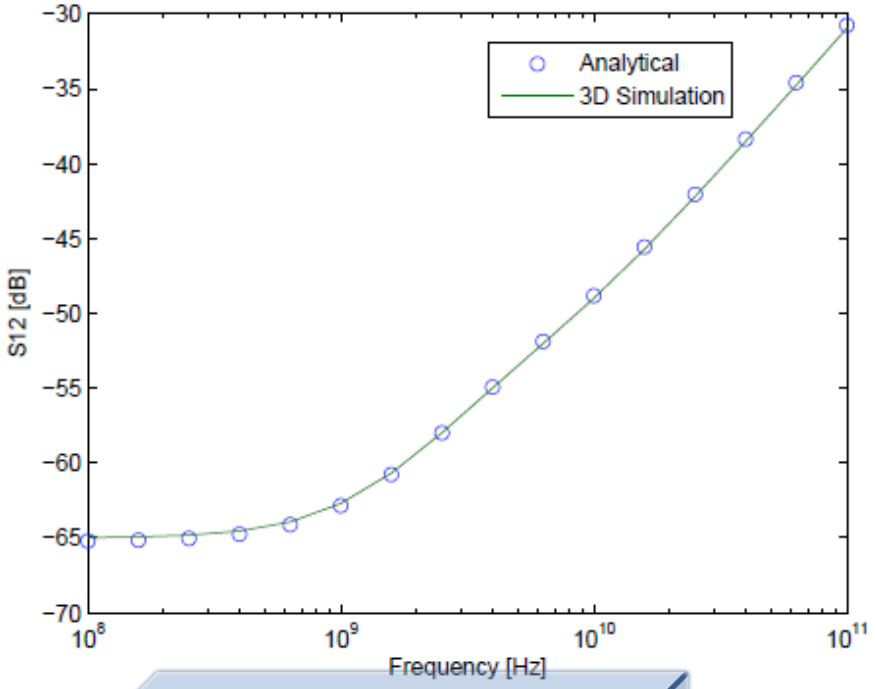
Internal impedance:

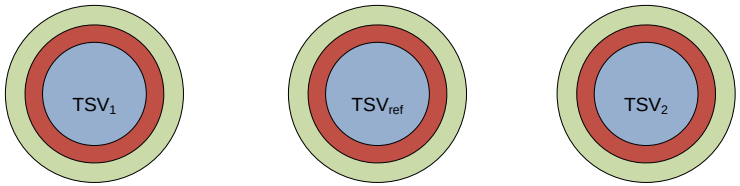
$$Z = \frac{\sqrt{j\omega\mu/\sigma}}{2\pi r} \frac{I_0(r\sqrt{j\omega\mu\sigma})}{I_1(r\sqrt{j\omega\mu\sigma})} \quad \Omega/m$$

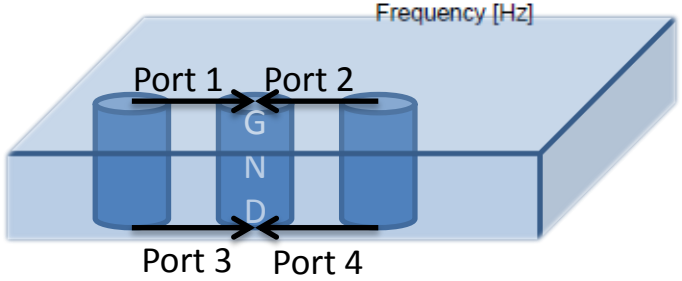


TSV Crosstalk

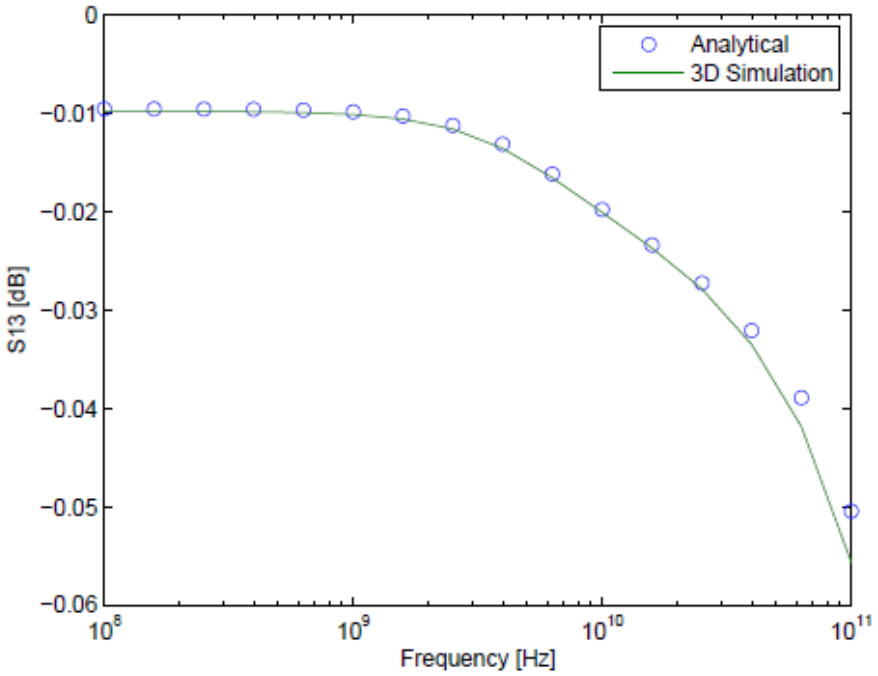


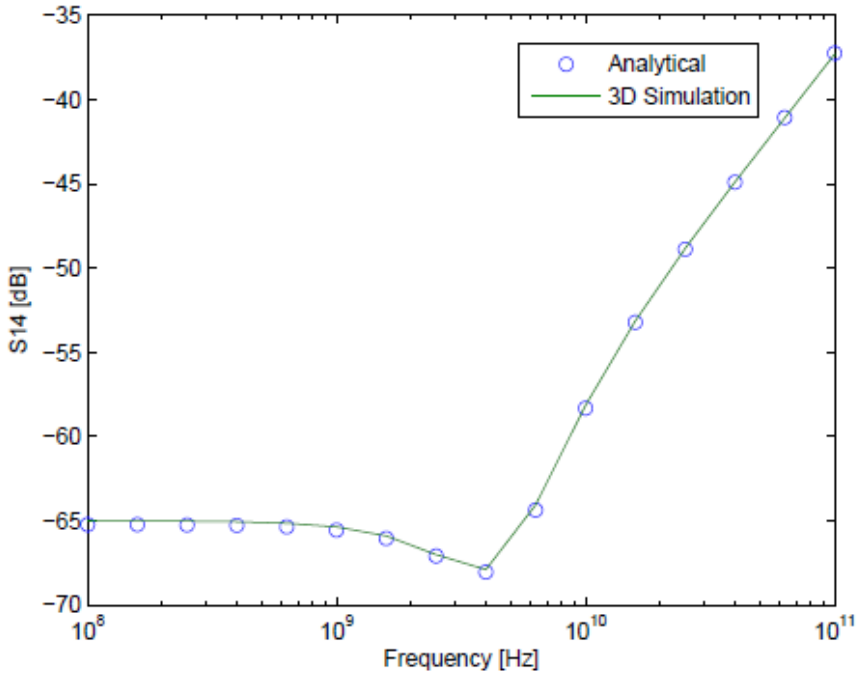




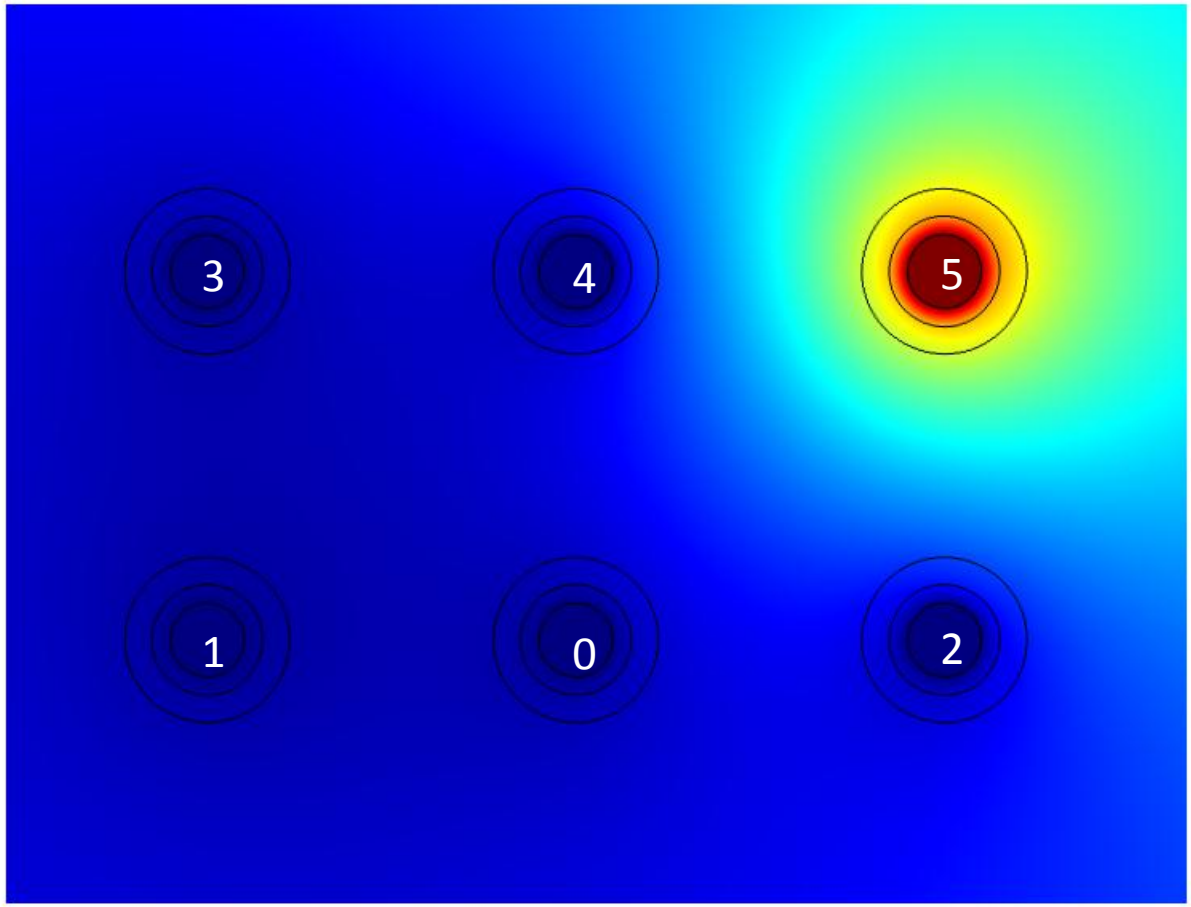


TSV Crosstalk

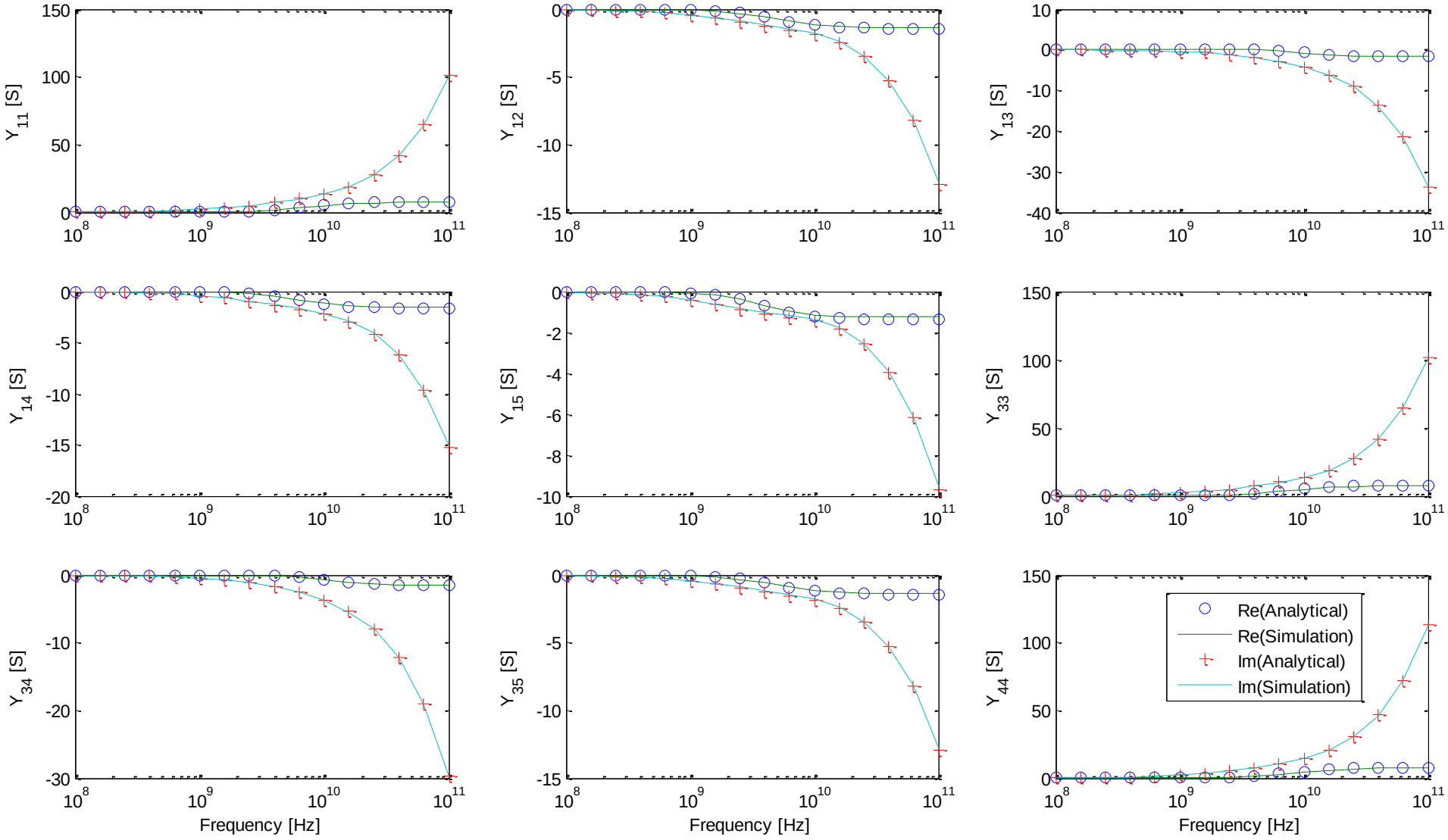




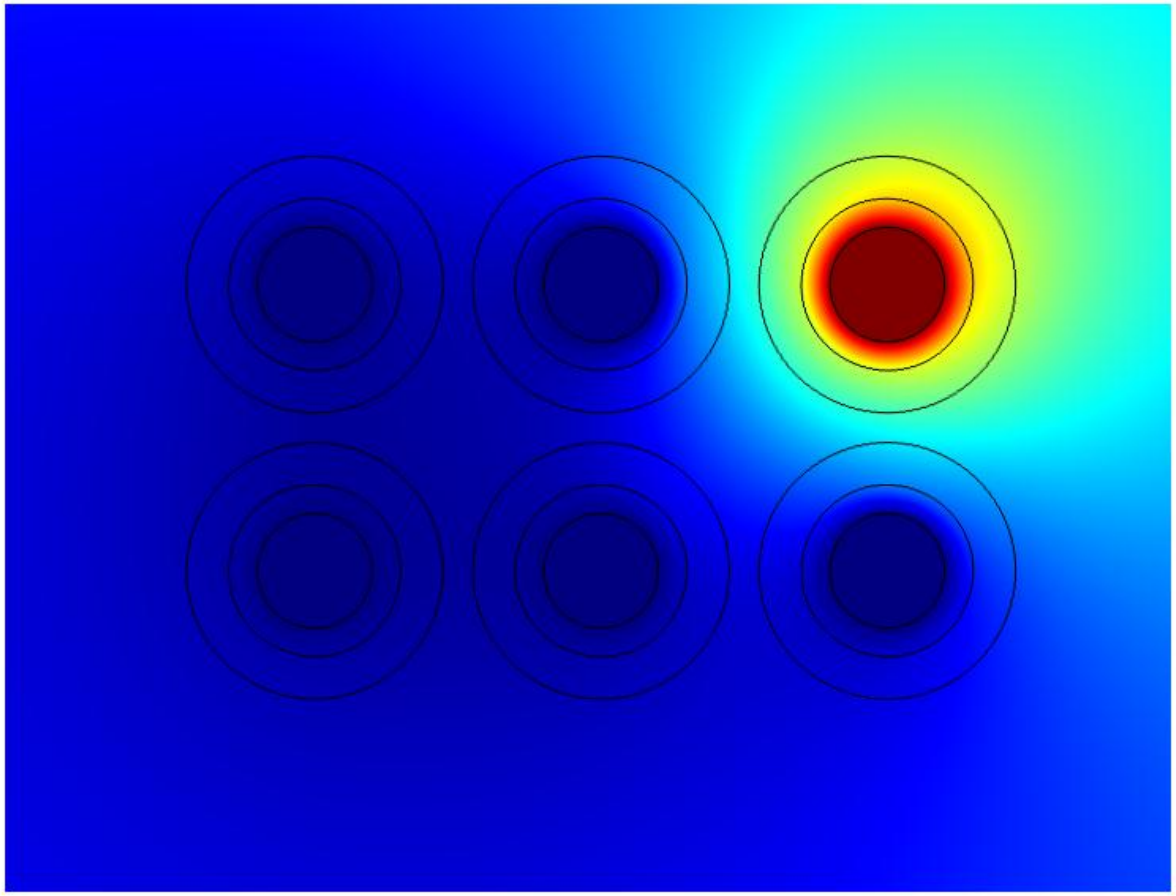
Via Array with 10um Pitch



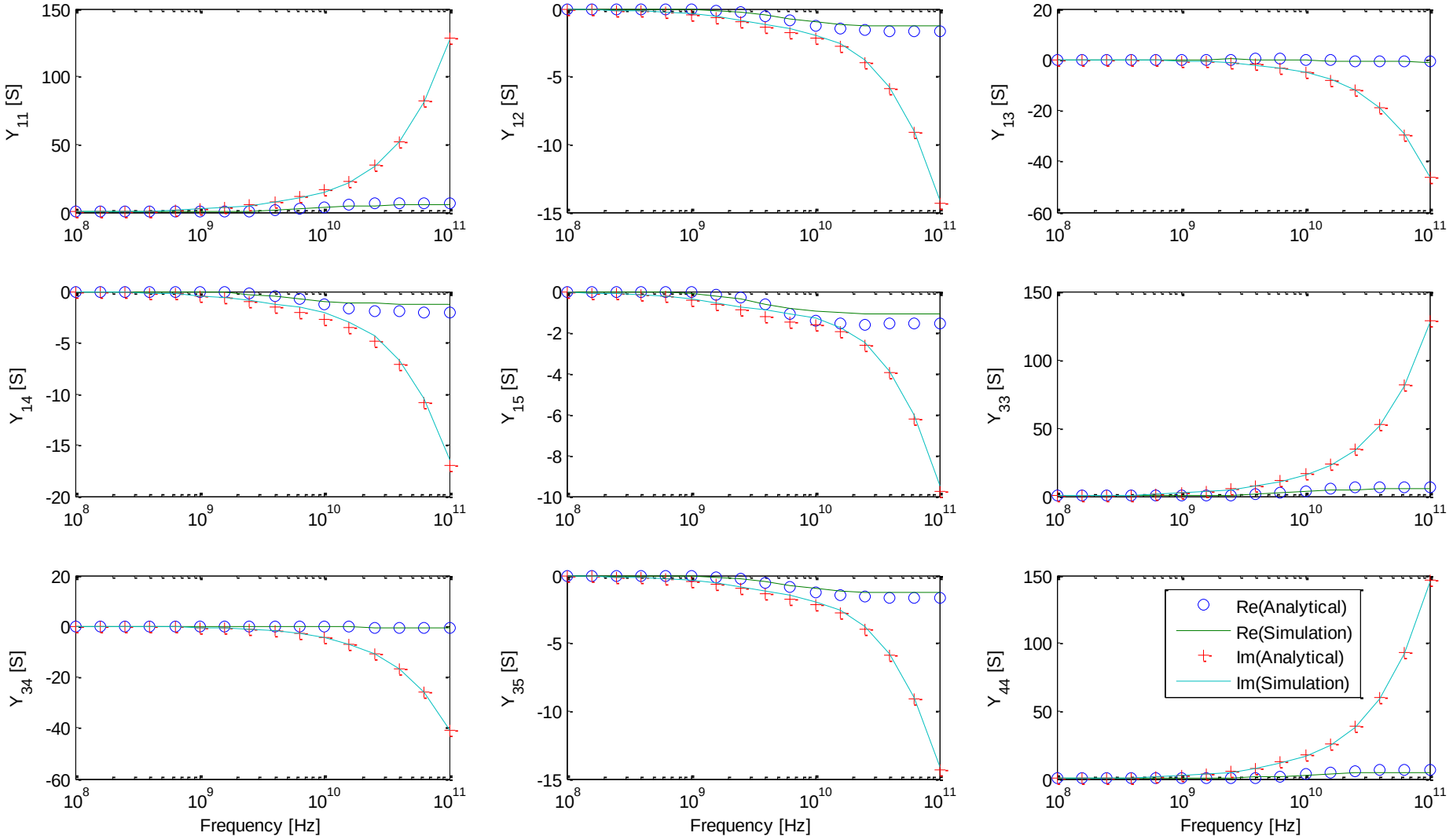
Results


Y11 [S]
Y12 [S]
Y13 [S]
Y14 [S]
Y15 [S]
Y33 [S]
Y34 [S]
Y35 [S]
Y44 [S]
Frequency [Hz]
Re(Analytical)
Re(Simulation)
Im(Analytical)
Im(Simulation)

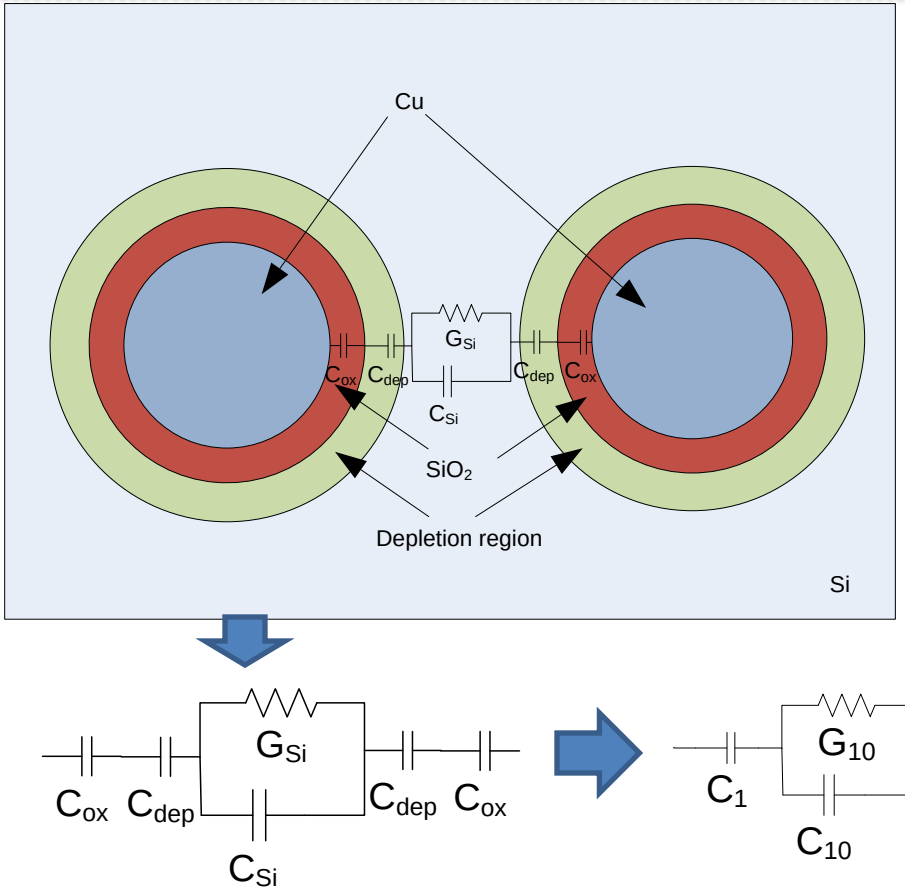
Via Array with 5um Pitch

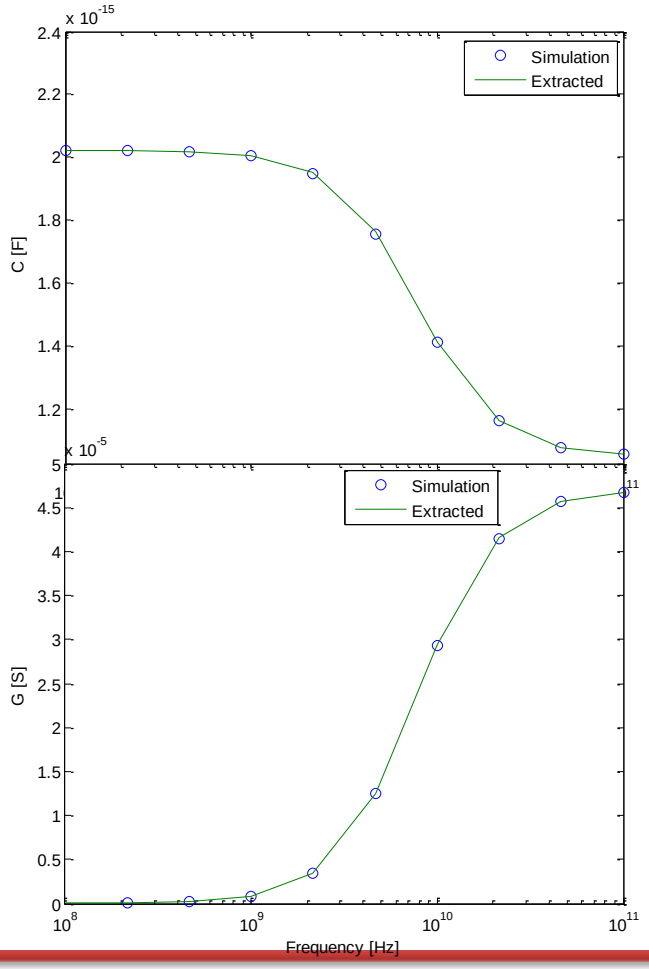


Results


Y11 [S]
Y12 [S]
Y13 [S]
Y14 [S]
Y15 [S]
Y33 [S]
Y34 [S]
Y35 [S]
Y44 [S]
Frequency [Hz]
Re(Analytical)
Re(Simulation)
Im(Analytical)
Im(Simulation)

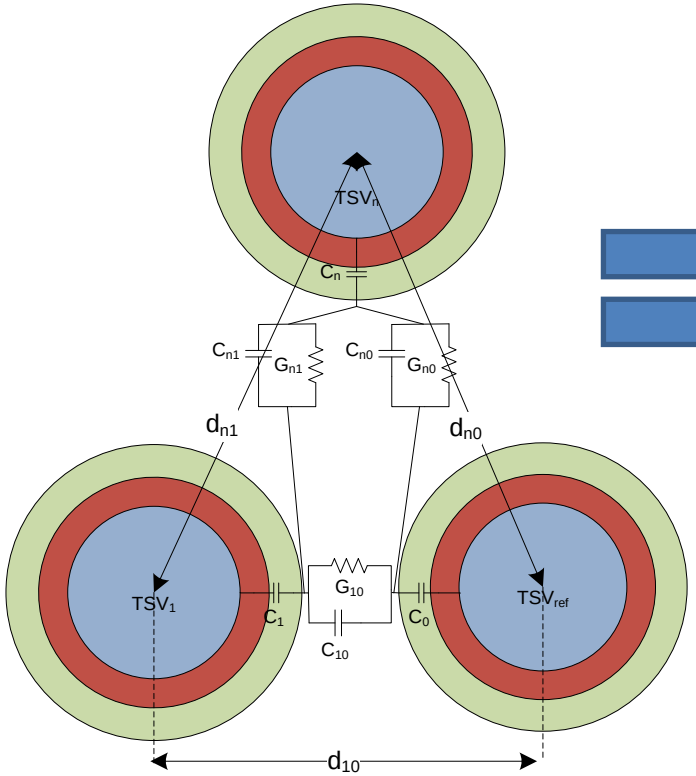
Model Fitting for a Single Pair

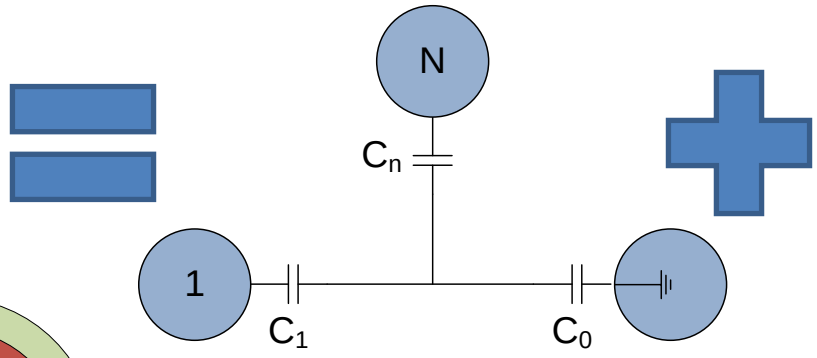




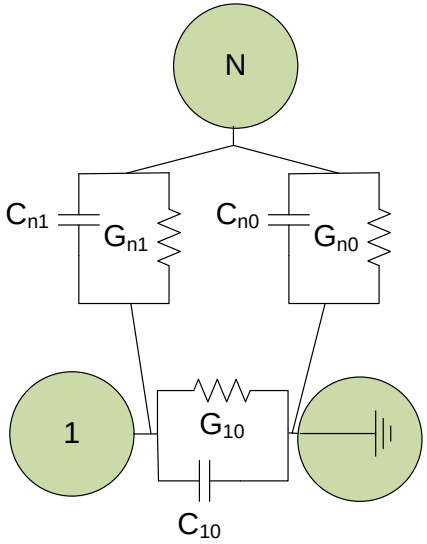
Model Fitting for N TSVs

- Problem: Extract $C_i, C_{i,j}, G_{i,j}$ from simulation or measurement



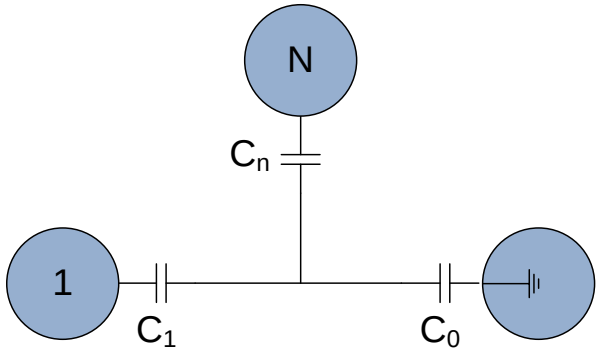


Oxide capacitances extracted at lowest frequency



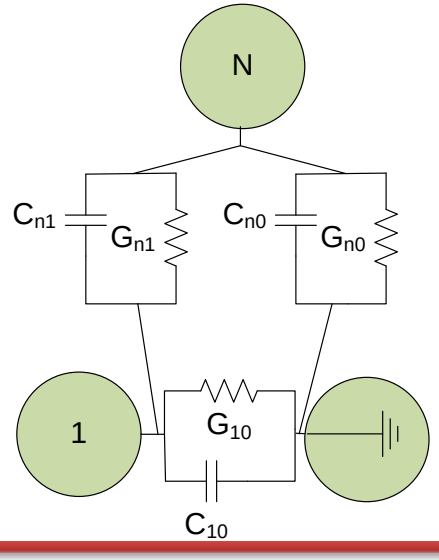
Substrate capacitances and conductances extracted at high frequency

Model Fitting Steps



$$\overline{\overline{Z}}_{ox} = \begin{bmatrix} Z_1 + Z_0 & Z_0 & \cdots & Z_0 \\ Z_0 & Z_2 + Z_0 & \cdots & Z_0 \\ \vdots & \ddots & \ddots & \vdots \\ Z_0 & Z_0 & \cdots & Z_N + Z_0 \end{bmatrix}$$

$$Z_i = 1/(j\omega C_i)$$

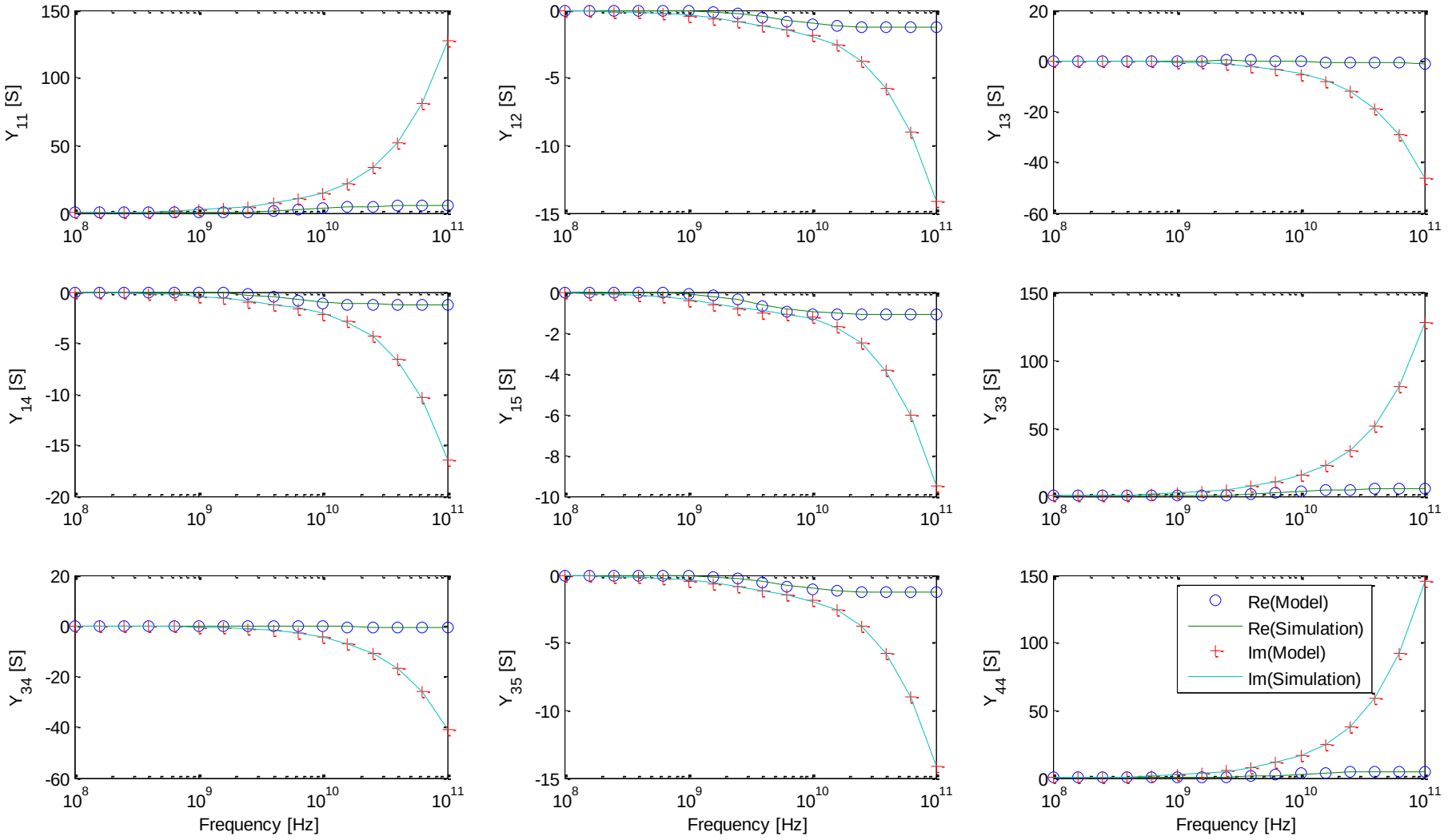


$$\overline{\overline{Z}}_{Si} = \overline{\overline{Z}}_h - \overline{\overline{Z}}_{ox}$$

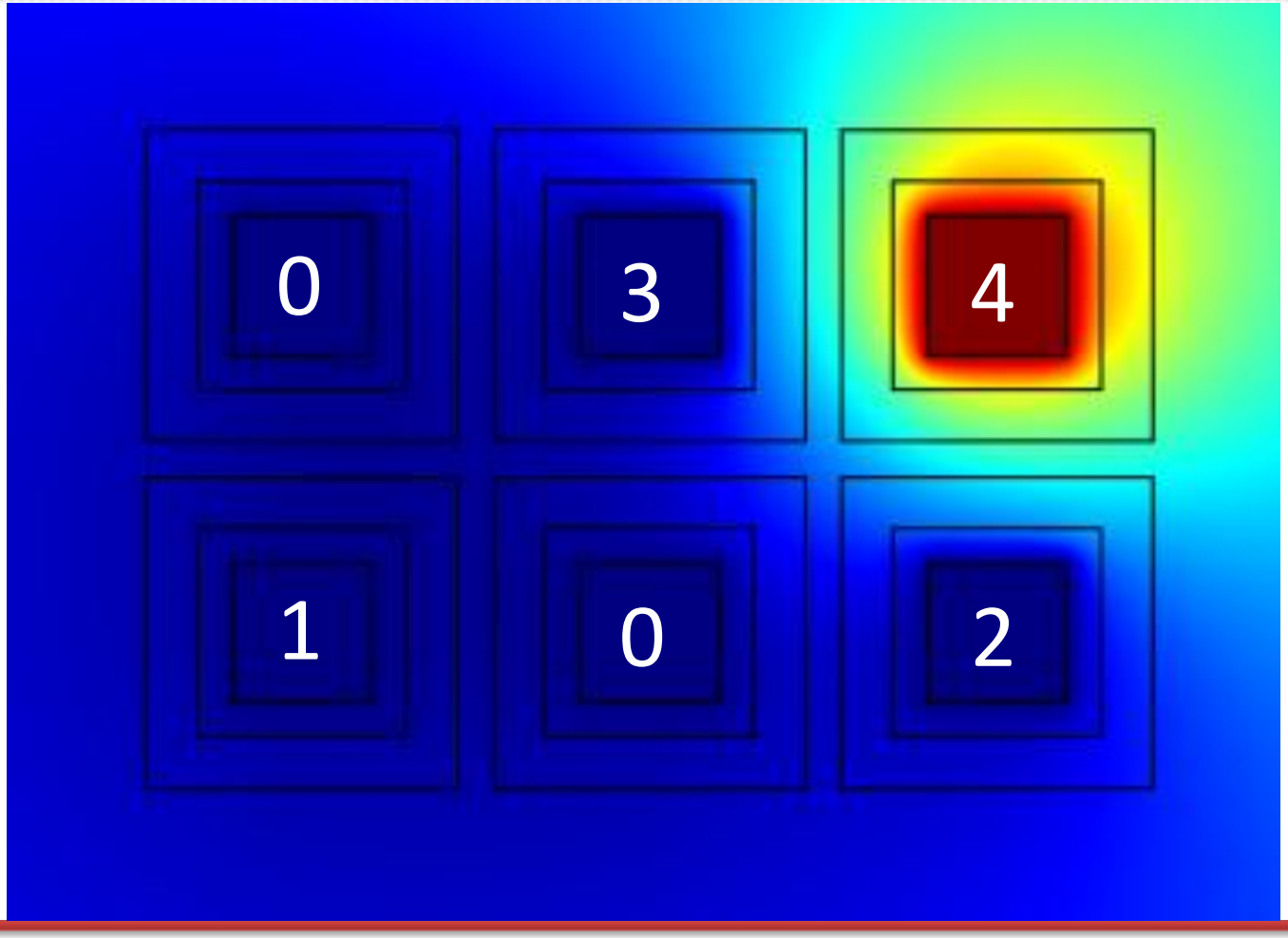
$$\overline{\overline{Y}}_{Si} = \begin{bmatrix} \sum_{i=1}^{N} Y_{1i} & -Y_{12} & \cdots & -Y_{1N} \\ -Y_{21} & \sum_{i=1}^{N} Y_{2i} & \cdots & -Y_{2N} \\ \vdots & \ddots & \ddots & \vdots \\ -Y_{N1} & -Y_{N2} & \cdots & \sum_{i=1}^{N} Y_{Ni} \end{bmatrix}$$

$$Y_{ij} = Y_{ji} = G_{ij} + j\omega C_{ij}$$

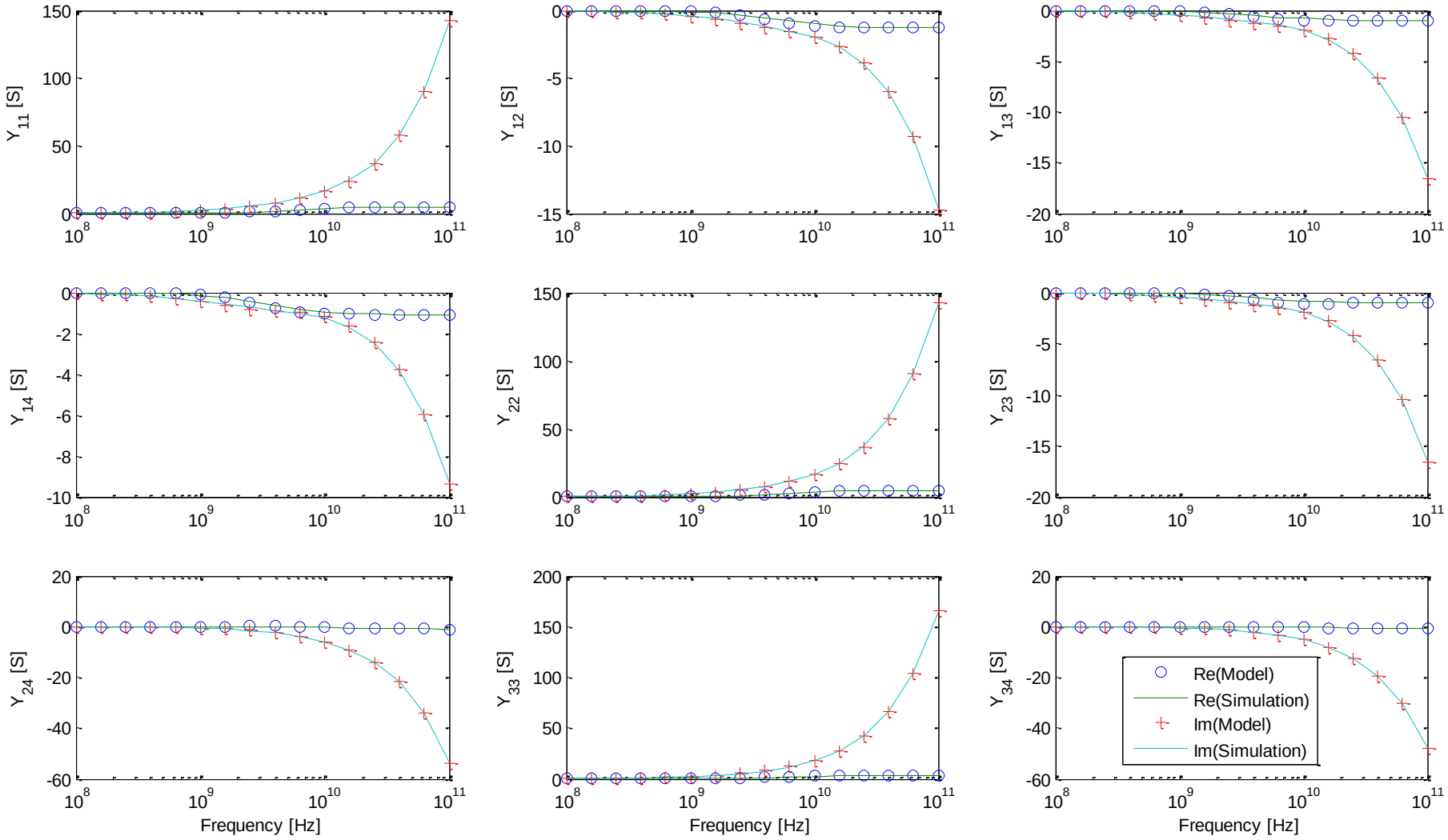
Model Fitting for 5um Pitch TSVs



Square-Shaped TSVs



Results


Y11 [S]
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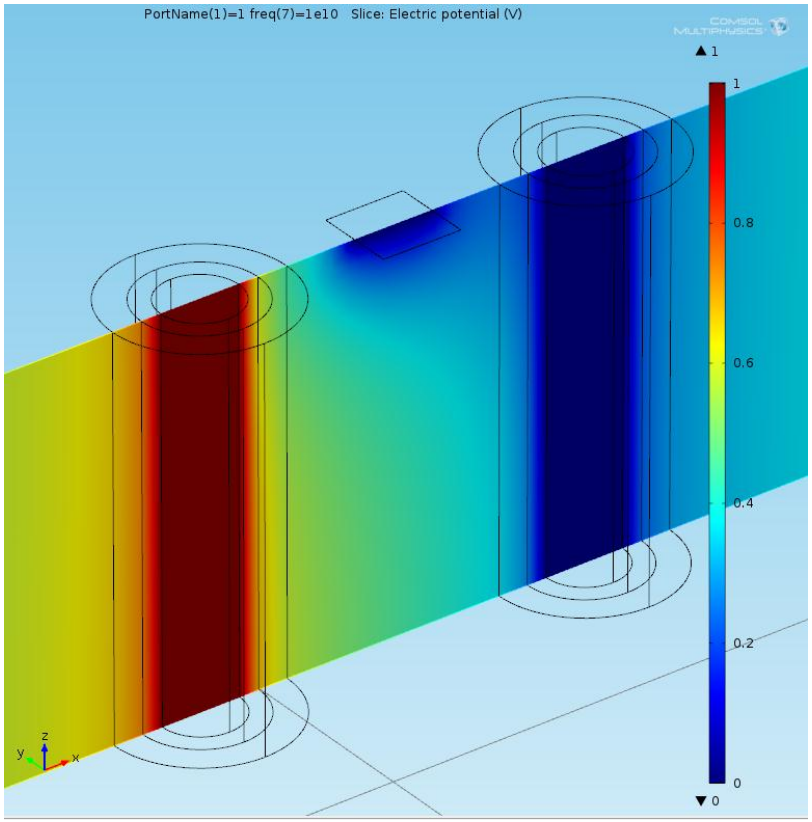
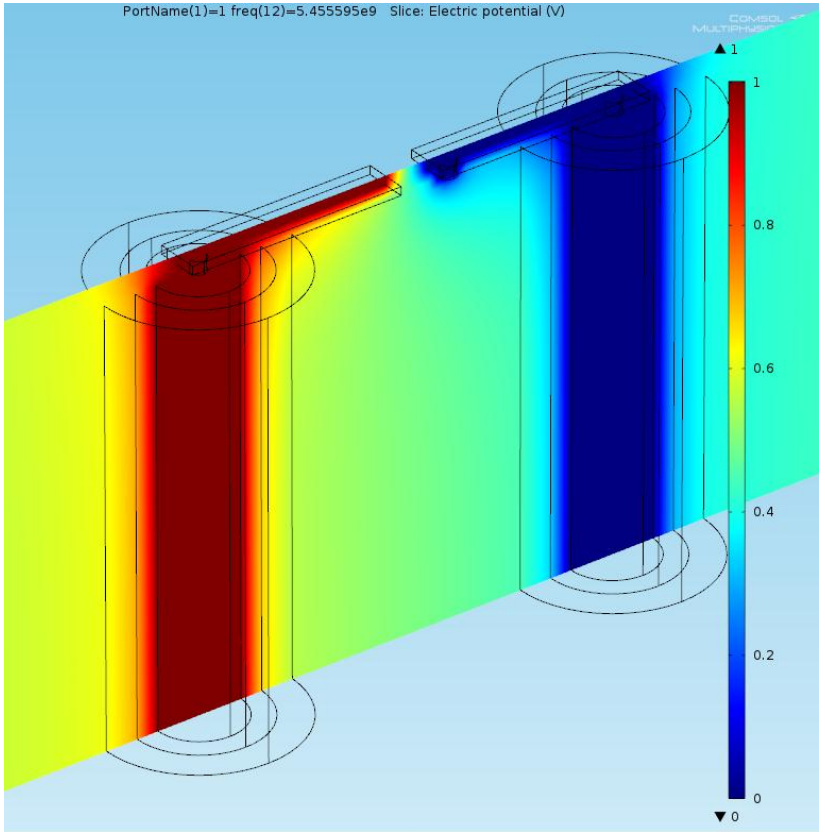
Y13 [S]
Y14 [S]
Y22 [S]
Y23 [S]
Y24 [S]
Y33 [S]
Y34 [S]
Frequency [Hz]
Frequency [Hz]
Frequency [Hz]
Re(Model)
Re(Simulation)
Im(Model)
Im(Simulation)

3D Structures

Substrate Contact

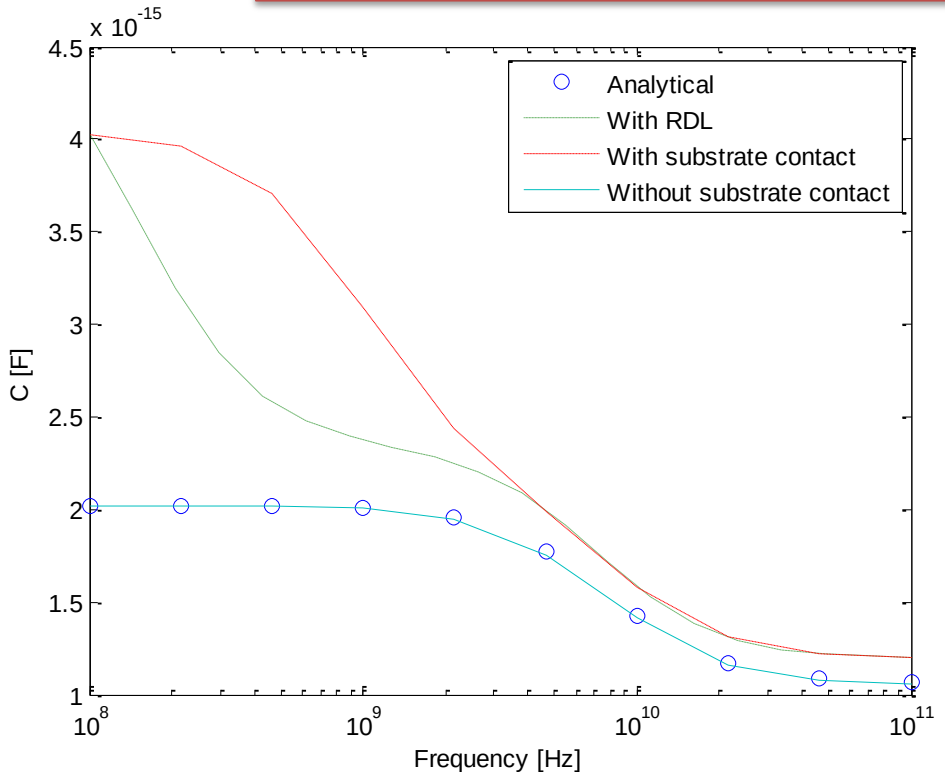


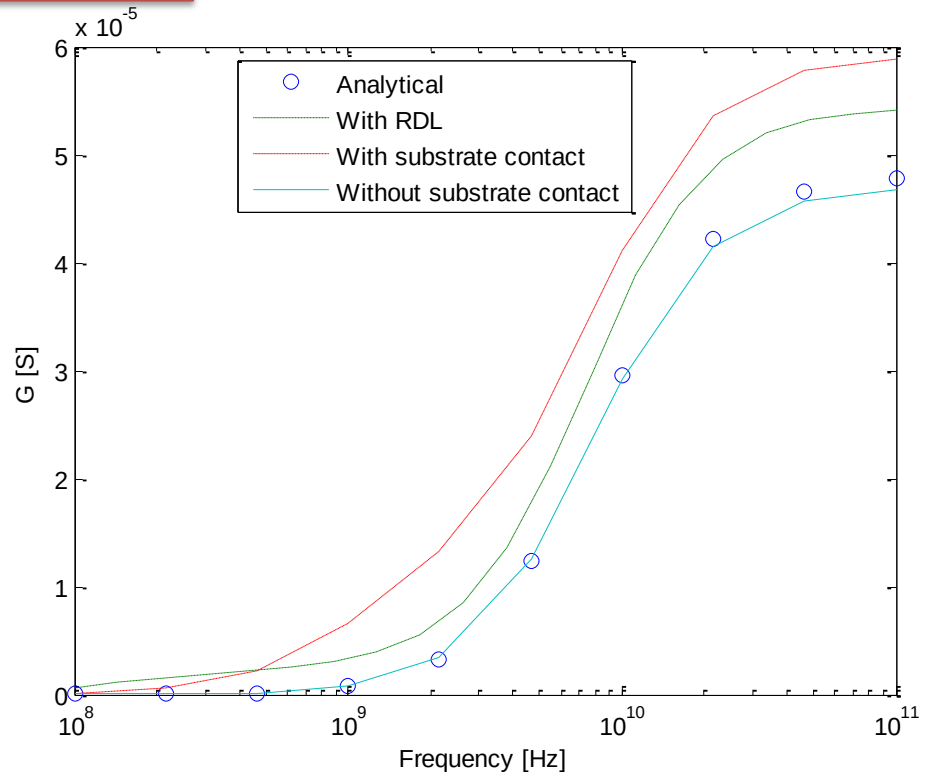
Redistribution Layers



Analytical Method

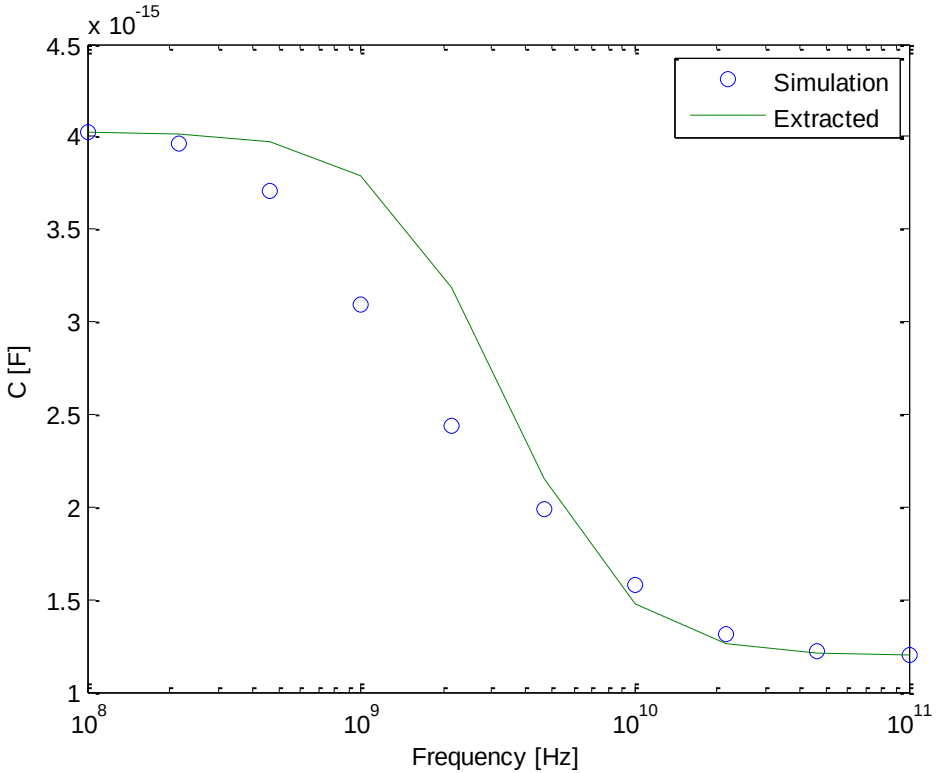
Does not work for general 3D structures!



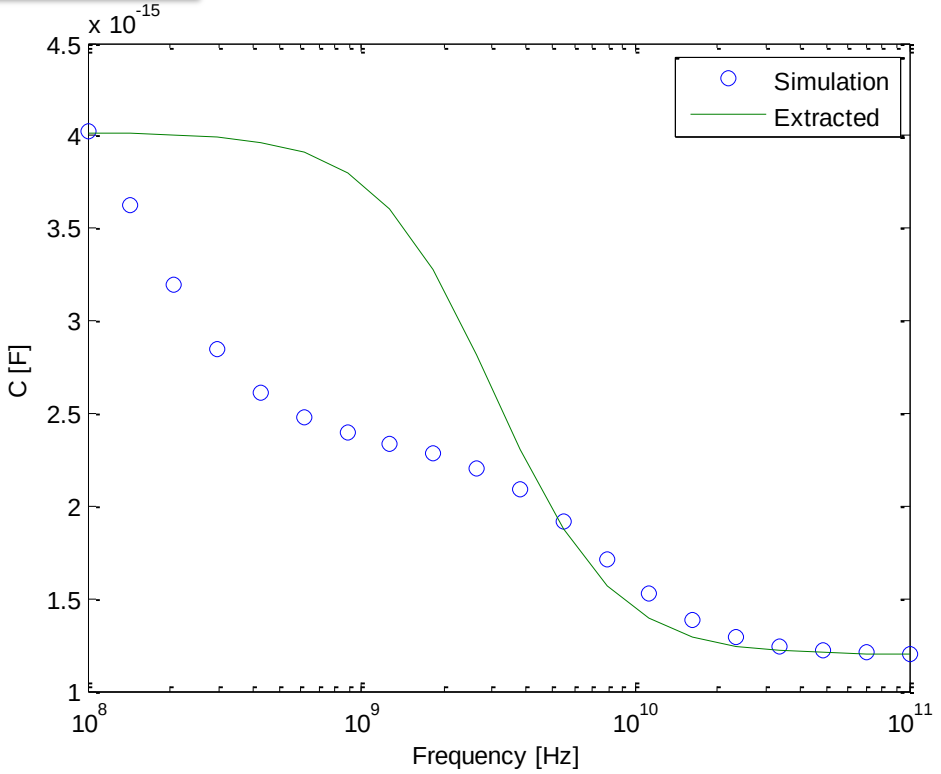


Model Fitting

Does not work for general 3D structures!



Substrate Contact



RDL

RC Vector Fitting

- A general approach is curve fitting a rational function:

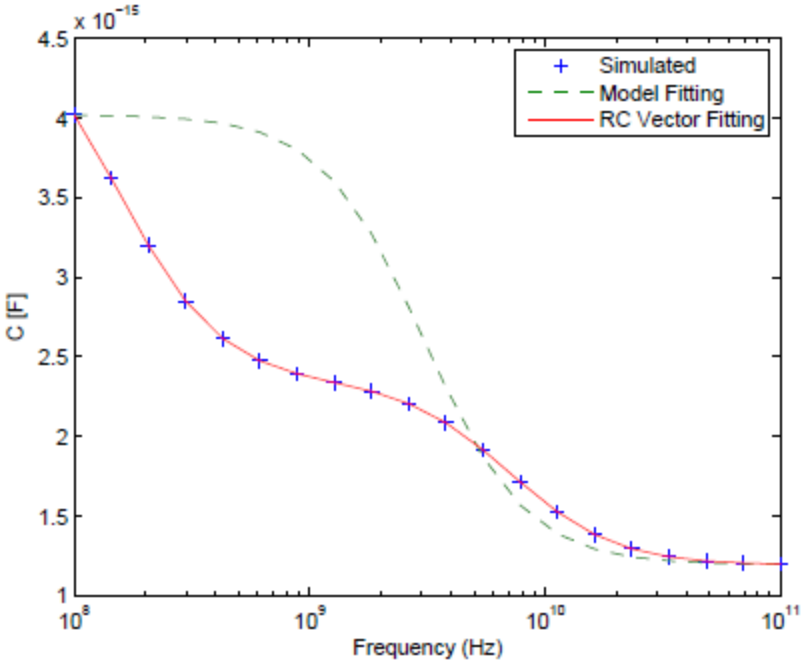
$$Z_{RC} = \frac{Y_{RC}}{s} = c + \sum_{i=1}^{M} \frac{k_i}{s - p_i}$$

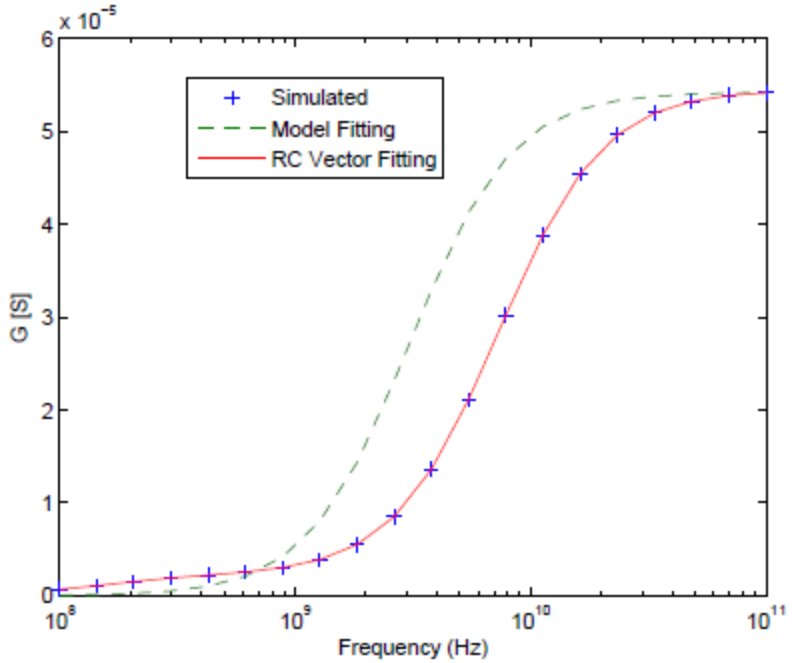
- All residues and constant terms are non-negative for RC network: $c, k_i \geq 0$
- All poles are non-positive real: $p_i \leq 0$
- We modify the standard vector fitting algorithm to enforce an RC model using non-negative least squares

$$\begin{bmatrix} c \\ k_1 \\ \vdots \\ \vdots \\ k_M \end{bmatrix} \geq 0$$

RC Vector Fitting for RDL

- Excellent match using 3 poles
- RC model can easily be generated from pole-residue description





Summary

- Pre-layout:
  - Analytical method and model fitting can be used to have rough estimate of self and mutual capacitance and conductance.
- Post-layout:
  - 3D EM simulation needed in the presence of substrate contacts, active devices, and RDLs. Model extraction can be done using RC vector fitting.