18th Asia and South Pacific Design Automation Conference
University LSI Design Contest
23 January 2013

A Ring-VCO-Based Sub-Sampling PLL CMOS Circuit with 0.73 ps Jitter and 20.4 mW Power Consumption

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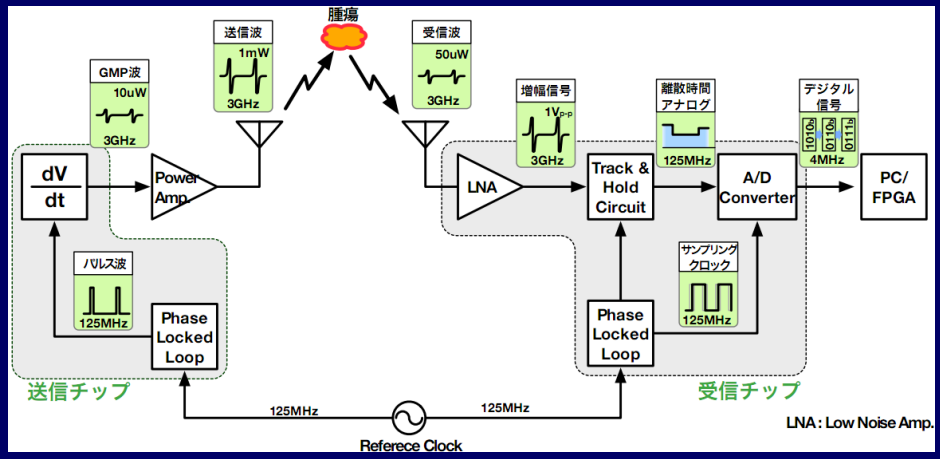
Introduction

Motivation

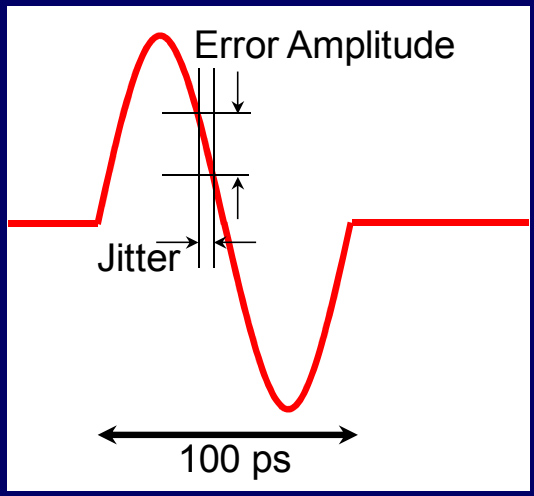
To detect malignant tumors, impulse-radio UWB (IR-UWB) radar-based CMOS breast cancer detection system using non-ionizing electromagnetic waves becomes a viable diagnostic option for women.

Goal

To develop IR-UWB radar system, low-jitter phase locked loop (PLL) is necessary for digital sampling of Gaussian monocycle pulse (GMP).



Early-breast cancer detection system

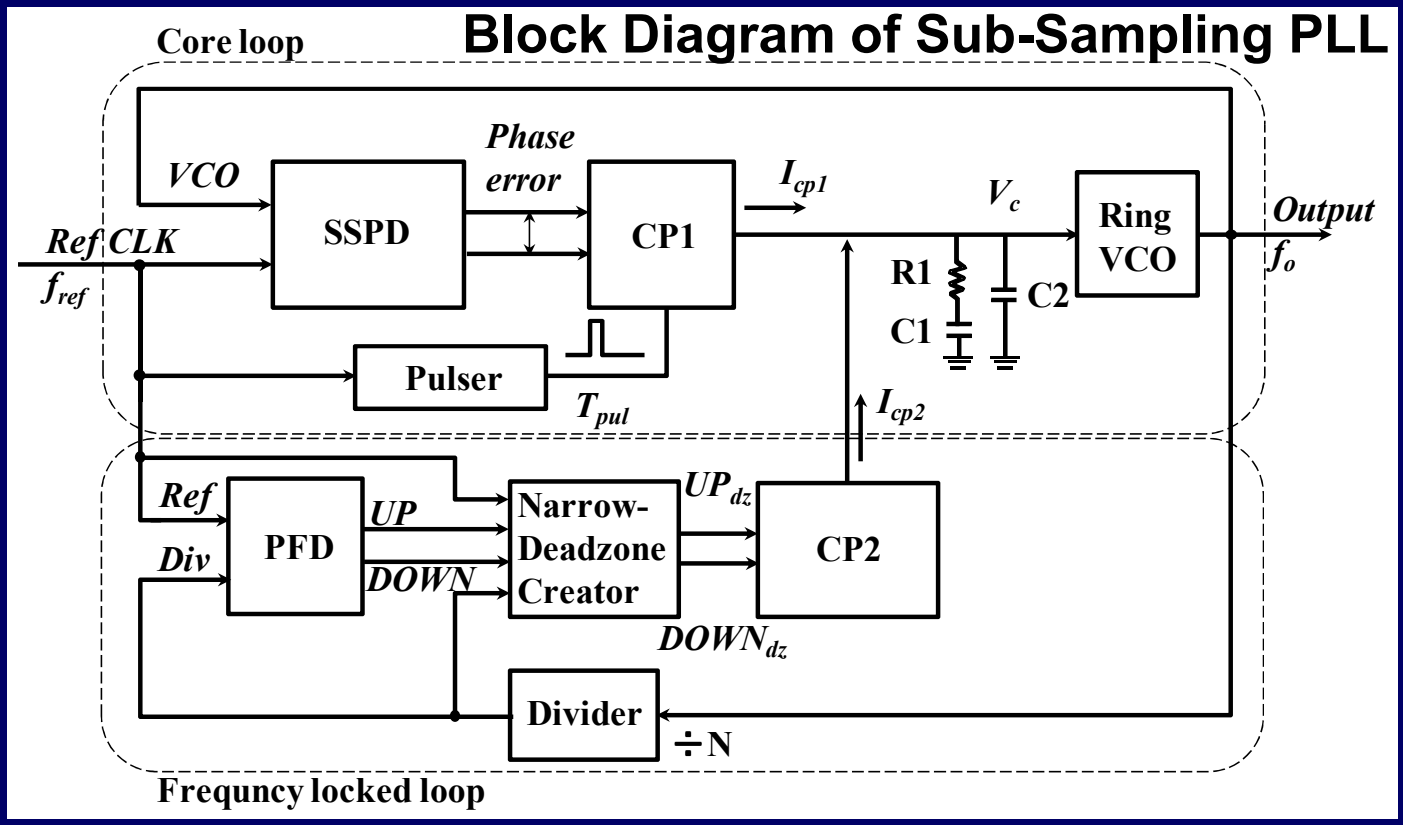


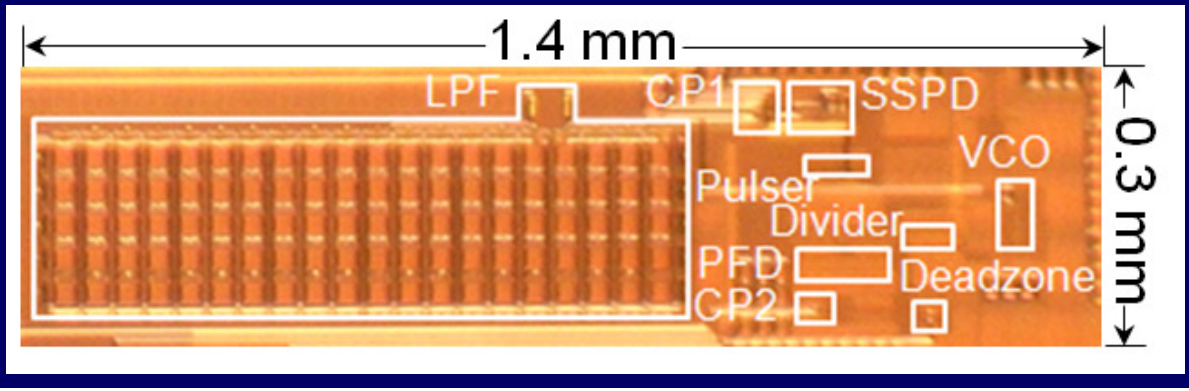
GMP: UWB signal

Issues of Conventional PLL

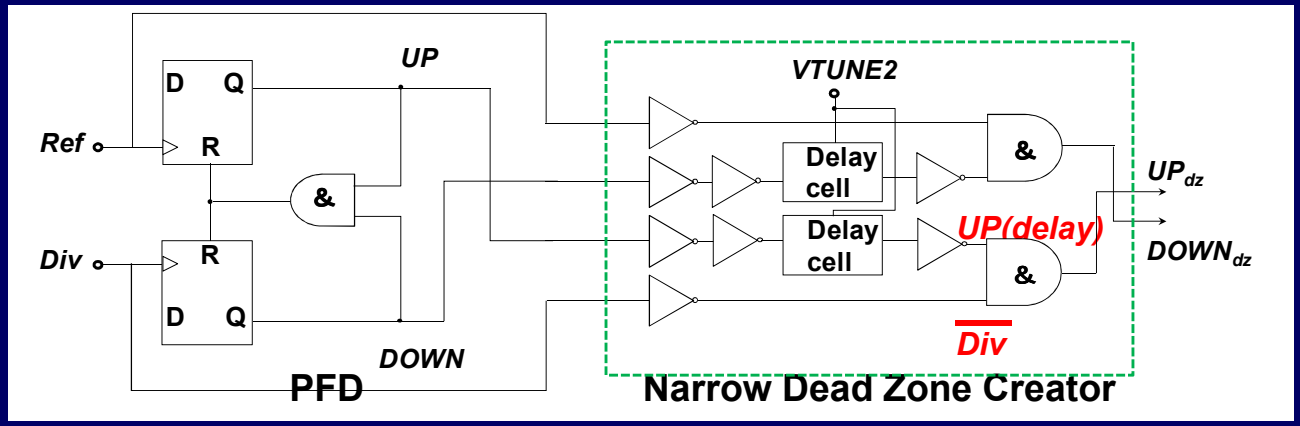
Due to the existence of divider in the feedback pass, in-band phase noise generated by the PFD, CP and the divider for conventional PLL is proportional to power spectral density multiplied by N^2 when transferred to the PLL output.

Sub-Sampling PLL for Ring-VCO

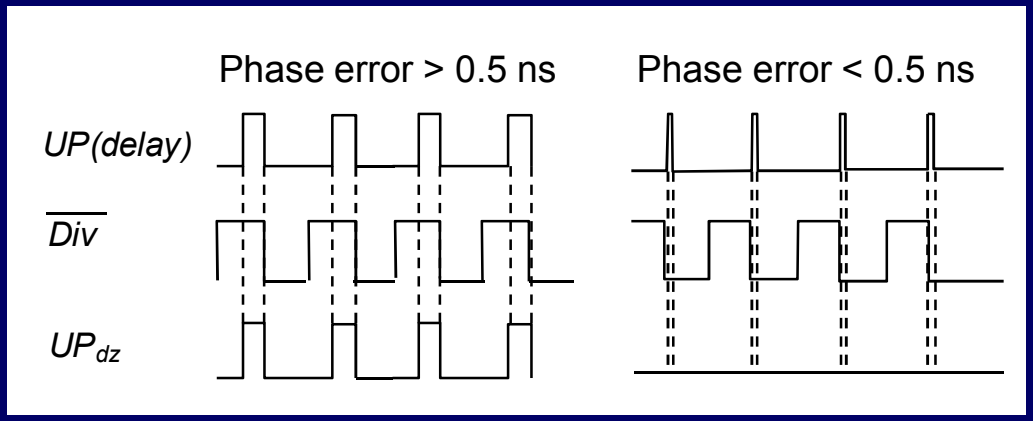




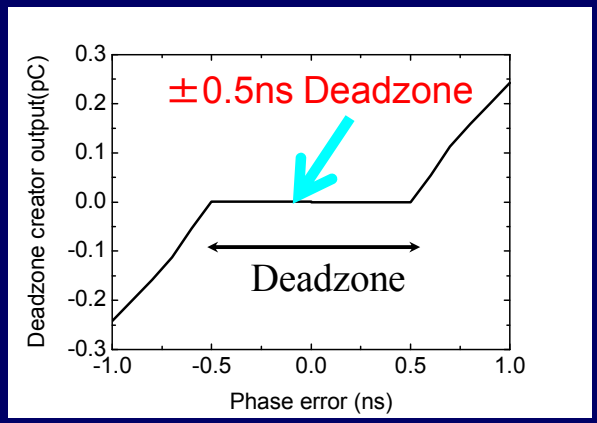
Narrow Dead Zone Creator



PFD with Dead Zone Creator



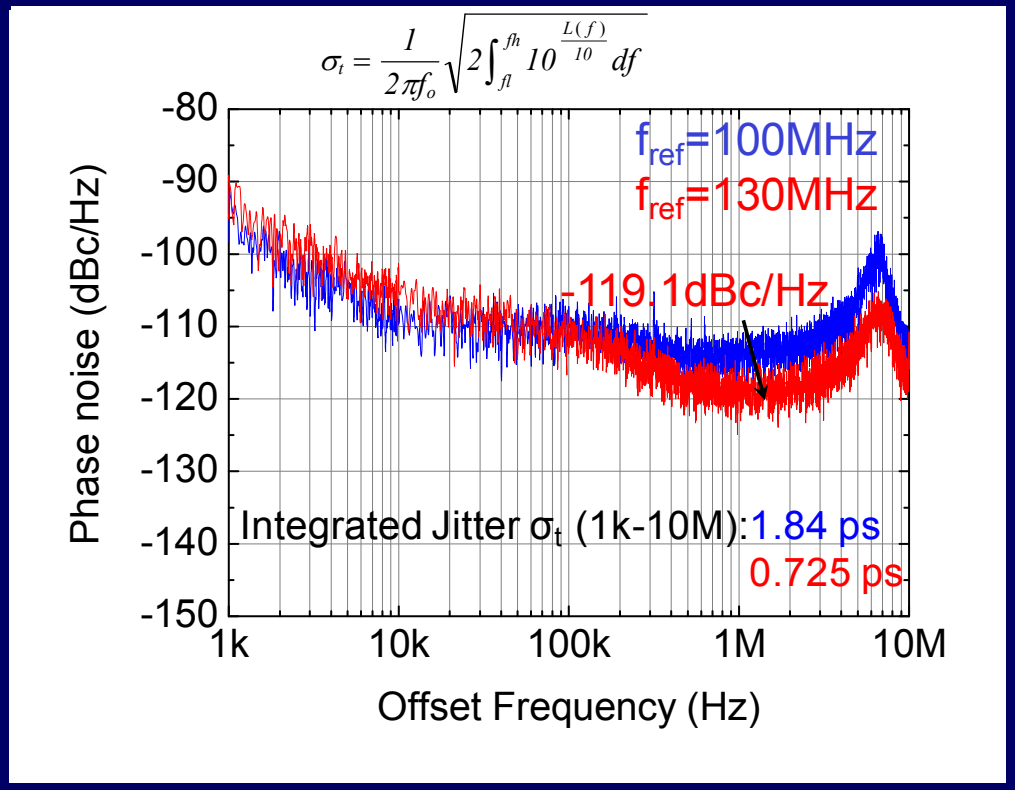
Dead Zone Creator Timing Chart



Dead Zone

Narrow dead zone creator is composed of tunable delay cells and AND gates. When the phase error is greater than 0.5 ns, AND gate output of *UP(delay)* and $\overline{Div}$, generates UP_{dz}, which is equal to *UP(delay)*. When the phase error is narrower than 0.5 ns, AND gate output of *UP(delay)* and $\overline{Div}$ generates zero signal. Consequently, dead zone creator becomes zero when phase error is within 0.5 ns.

Phase Noise and Figure of Merit



Measured PLL output phase noise

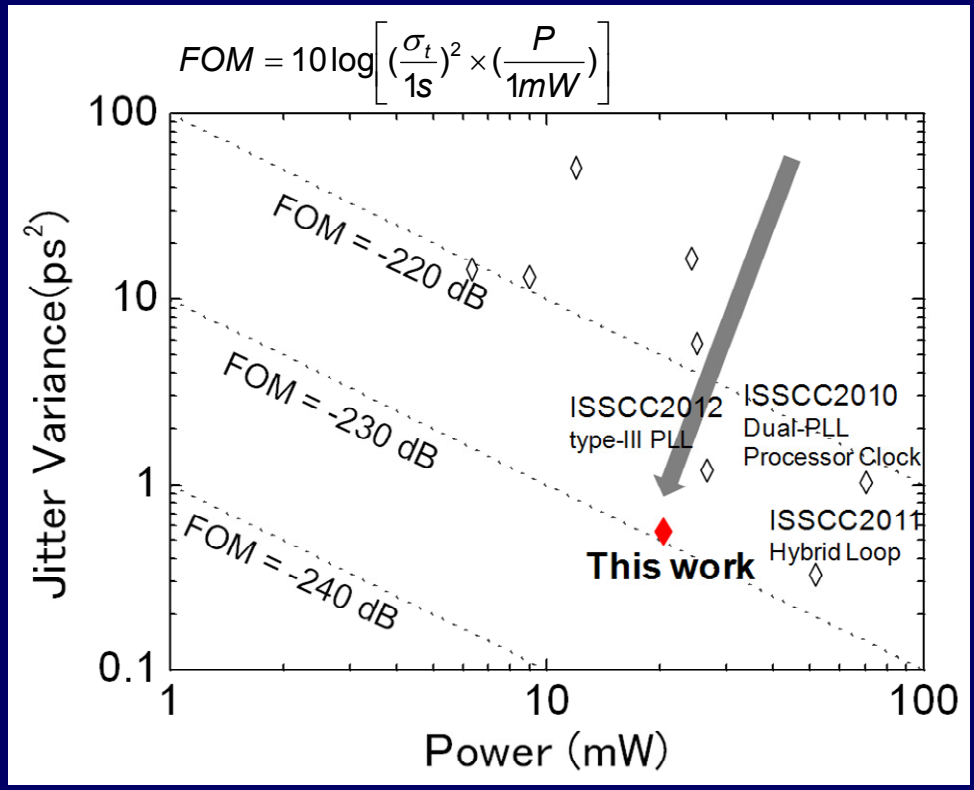


Figure of Merit

The phase noise of a fabricated 65 nm CMOS SS-PLL was measured. By increasing f_{ref} from 100 MHz to 130 MHz, the phase noise decreased so that the integrated jitter decreased from 1.84 ps (1k-10M) to 0.725 ps (1k-10M). The figure of merit using jitter and power product was -229.7 dB that is the lowest value ever reported.

Summary

Performance Comparison with recently reported Ring-VCO-Based PLLs

	This work	ISSCC2011	ISSCC2010	ISSCC2012
Output Frequency	2.08 GHz	1.21 GHz	2.5 GHz	3.1 GHz
Reference Frequency	130 MHz	55 MHz	100 MHz	108 MHz
(In-band) phase noise	-119.1 dBc/Hz @1MHz	-119.6 dBc/Hz @1 MHz	-106.6 dBc/Hz @1 MHz	-
Integrated jitter	0.725 ps (1k - 10M)	0.57 ps (1k - 10M)	0.99 ps (1M - 1.25G)	1.01 ps (1k-40M)
Power	20.4 mW	51.6 mW	70 mW	27.5 mW
FOM	-229.7 dB	-227.7 dB	-221.6 dB	-225.5 dB
Supply Voltage	1.2 V	1.2 V	2.5 V	1.2 V
Technology	65 nm CMOS	65 nm CMOS	45 nm SOI	65 nm CMOS

In-band phase noise of -119.1 dBc/Hz@1 MHz and integrated jitter of 0.725 ps (1kHz-10MHz offset) were obtained with the power consumption of 20.4 mW for ring-VCO-based sub-sampling PLL. The figure of merit was -229.7 dB that is the lowest value ever reported.