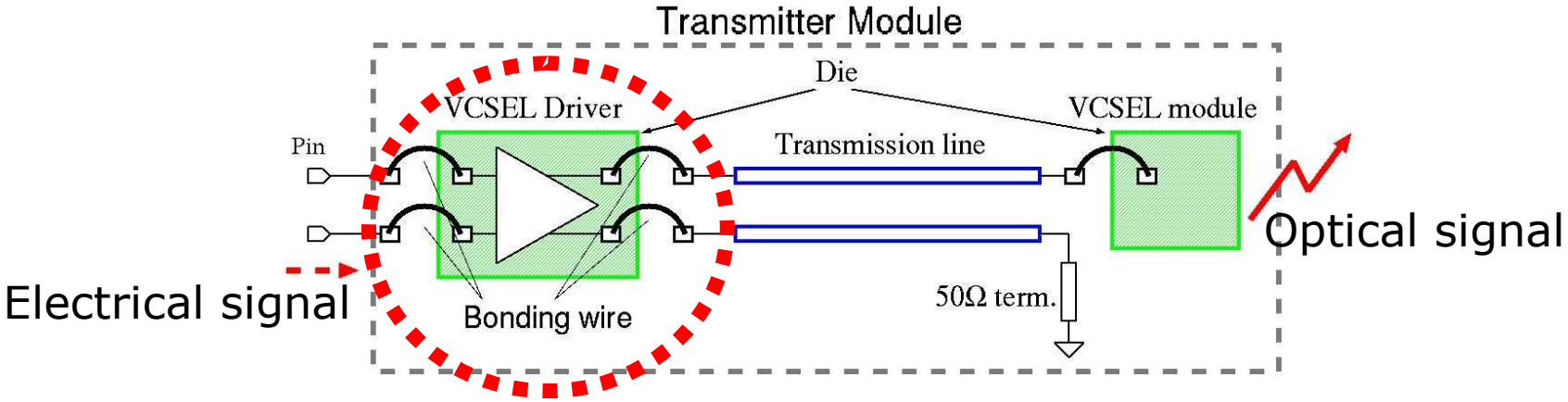
1D-18: A 25-Gb/s LD Driver with Area-Effective Inductor in a 0.18μm CMOS

Takeshi Kuboki, Yusuke Ohtomo,
Akira Tsuchiya, Keiji Kishine and
Hidetoshi Onodera

Kyoto University, NTT Electronics and
University of Shiga Prefecture, Japan

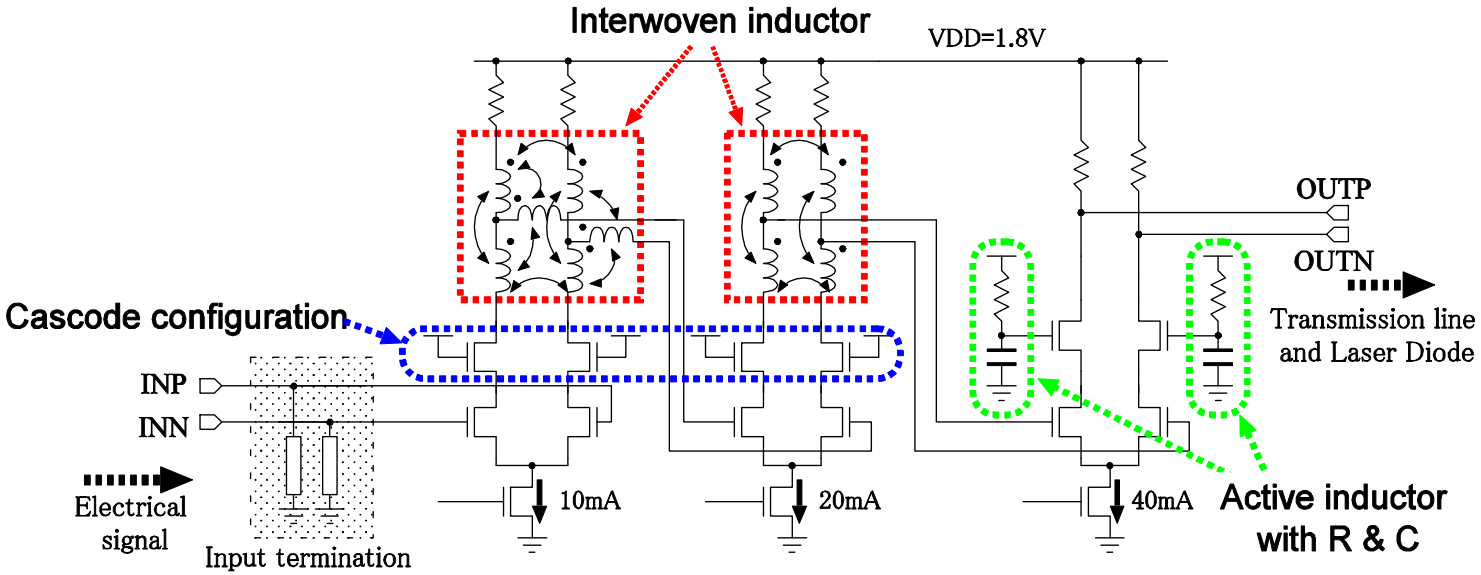
This work

- **CMOS LD driver for VCSEL in Optical communication system**
  - **Smallest and Fastest data rate in 0.18μm CMOS**
- **Feature**
  - **Small area**
    - **Interweave 10 inductors into 2 ➔80% area reduction**
  - **High-speed operation**
    - **Achieved 25 Gb/s operation**



VCSEL: Vertical Cavity Surface Emitting Laser

Design summary

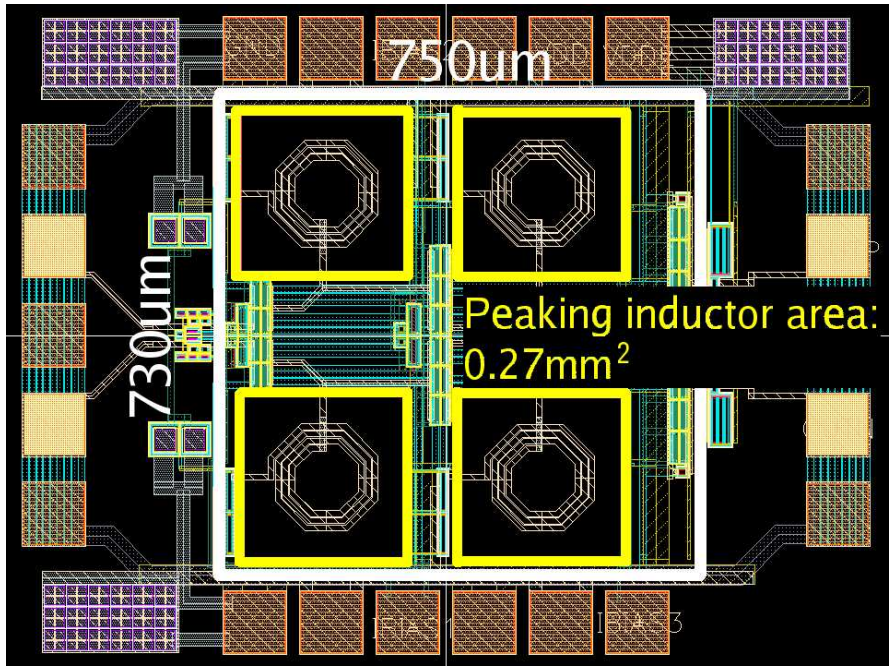


- 0.18μm CMOS
- VDD: 1.8V
- Modulation Current: 40mA
- Power: 126mW

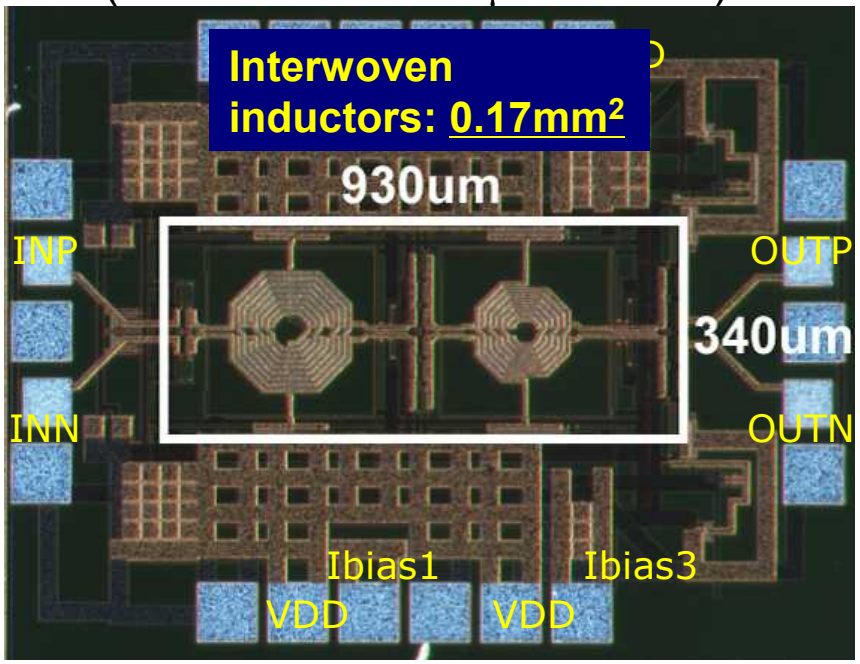
- Cascode configuration
  - Reduce Miller-effect
- Interwoven inductor
  - Reduce inductor's area and routing wires
- Active inductor
  - Enhance bandwidth of output stage and keep output impedance

Area Reduction

Widely used shunt peaking
Single inductor per area



Double shunt-series peaking with mutual L
Interwoven Inductor
(fabricated in 0.18μm CMOS)

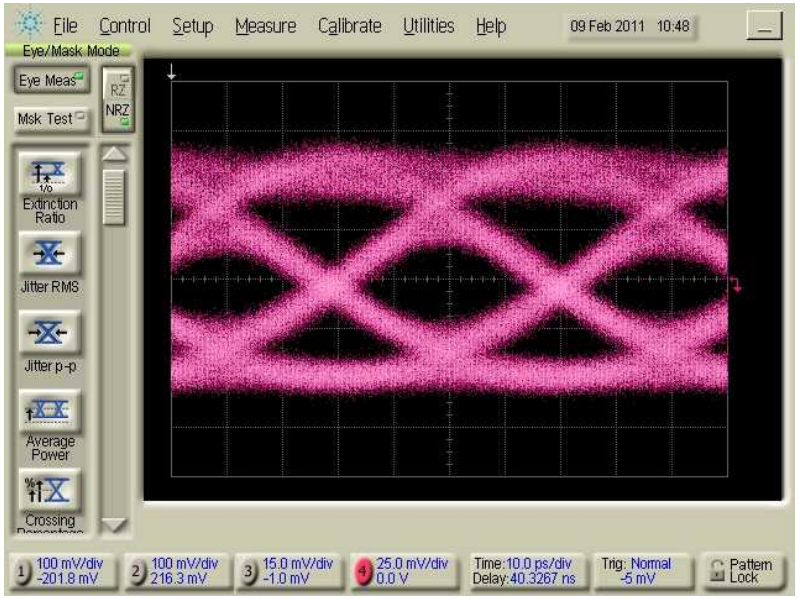


Inductor area	**0.27mm²**	**-37%**	**0.17mm²**
Area / inductor	**0.0675mm²**	**-75%**	**0.017mm²**
Circuit area	**0.55mm²**	**-42%**	**0.32mm²**

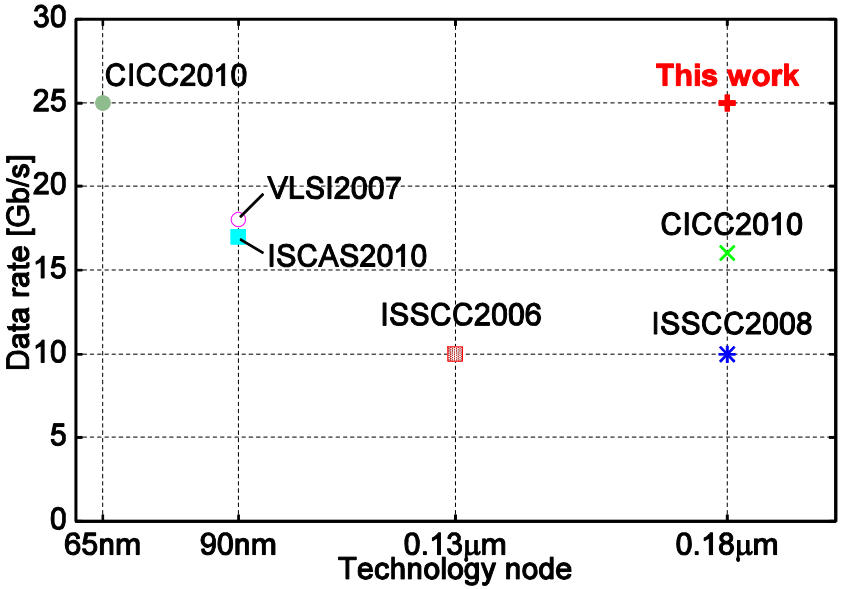
Also interwoven inductor shorten routing wire to inductor.
➔ Parasitics can be minimized.

Measured results and conclusion

•Measured eye-diagram at 25Gb/s



•Comparison to other optical drivers



- Proposed LD driver exhibits **30% smaller chip area and operation at 25Gb/s data rate**.
  - ➔ Achieves the smallest and fastest LD driver in 0.18μm CMOS processes.

Detailed discussion on poster 1D-18