A 24.5-53.6pJ/pixel 4320p 60fps H.264/AVC Intra-Frame Video Encoder Chip in 65nm CMOS

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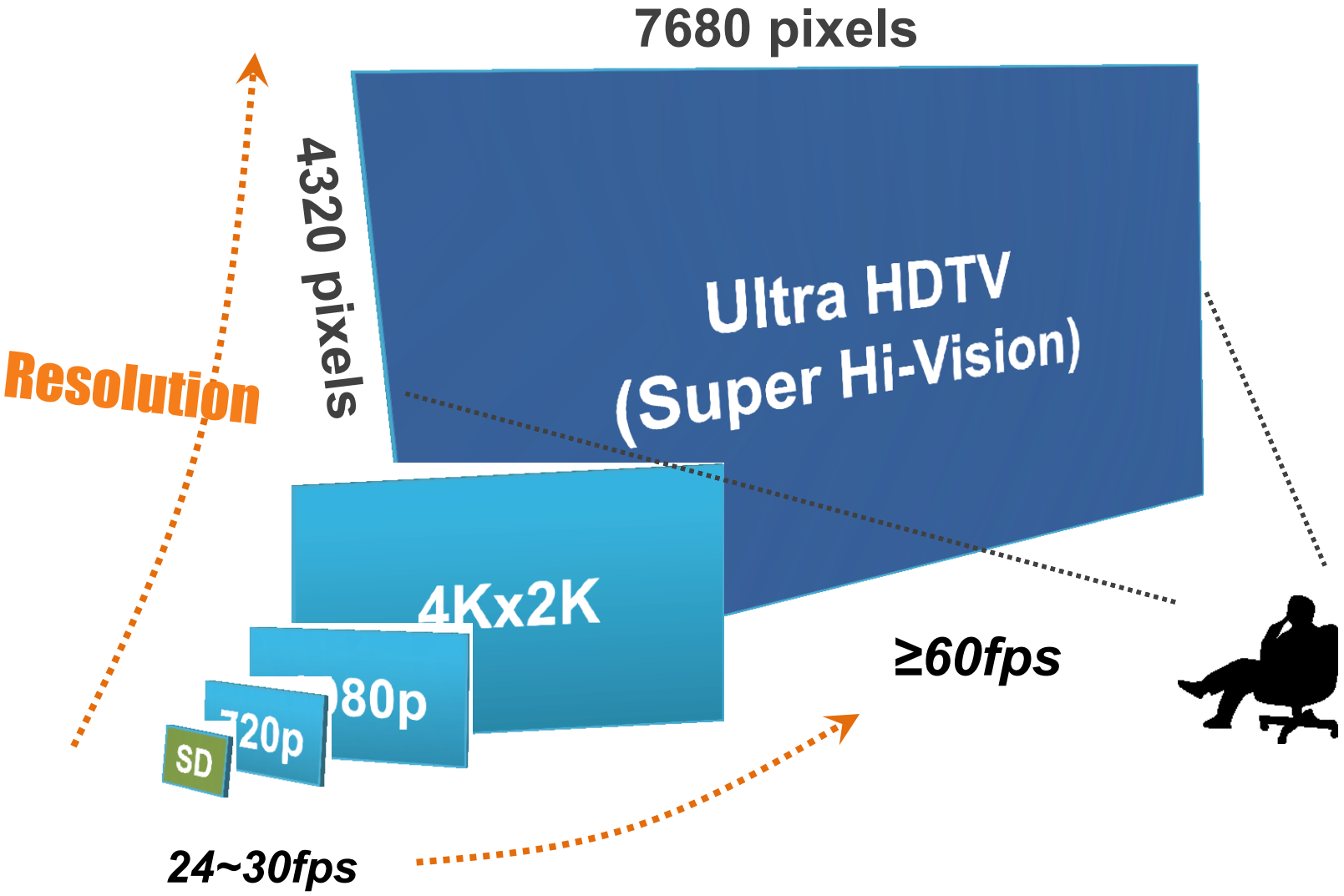
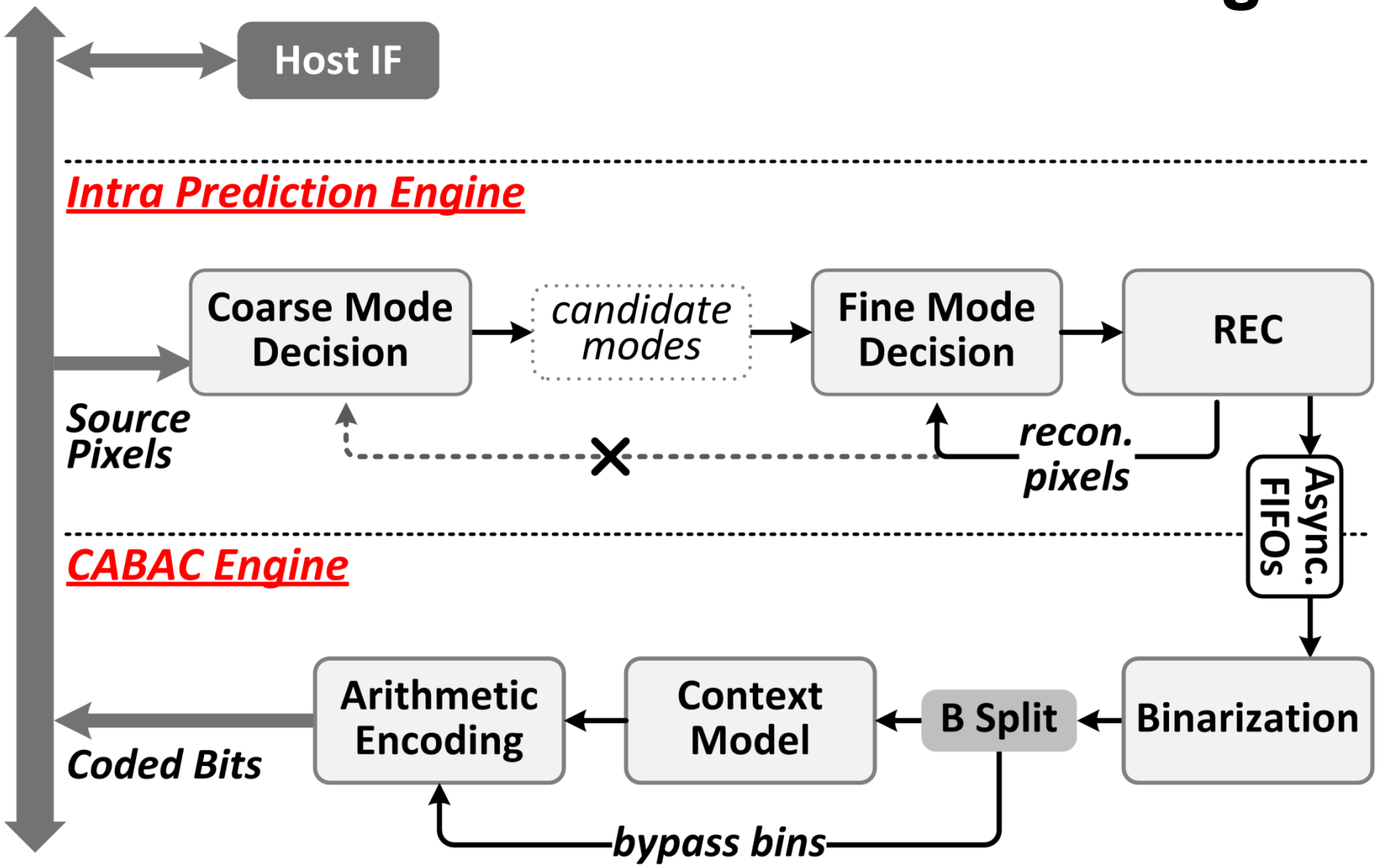
Next-generation HDTV



Block Diagram



Architecture Optimization

- **Intra Prediction**
  - Coarse-to-fine mode decision
  - Interlaced block reordering
  - Probability-based reconstruction
  - 74% overall complexity reduction

- **CABAC**
  - Pre-normalization
  - Hybrid path coverage
  - Bypass bin splitting
  - 31% performance increase

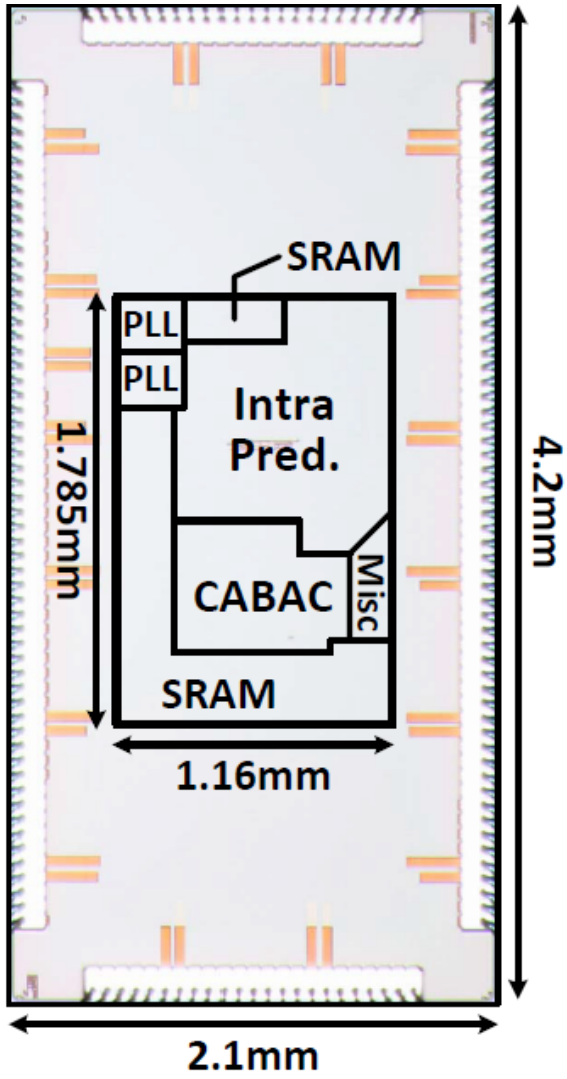
Chip Specification & Photo

Technology	e-Shuttle 65nm CMOS
Die area	8.82mm^2
Core area	2.07mm^2
Density	75.85%
Logic/SRAM	678.8Kgates/27.1KB
Max. resolution	7680x4320p 60fps
Max. pixel rate	1991Mpixels/s
Max. CABAC rate	1.41Gbins/s

Measured core power

106.7mW @ 1.20V, 260MHz/330MHz* (4320p60)
15.1mW @ 0.90V, 65MHz/65MHz* (2160p60)
6.1mW @ 0.80V, 33MHz/33MHz* (2160p30)
2.0mW @ 0.80V, 9MHz/9MHz* (1080p30)

* Freq.$_{INTRA}$/Freq.$_{CABAC}$



Summary

- **UHDTV Intra Encoder for H.264/AVC**
  - 1991Mpixels/s, at least 9.4x faster previous designs
  - 1.41Gbins/s CABAC improved by 31%

- **Power Dissipation**
  - 106.7mW for 4320p60
  - 2mW for 1080p30
  - 24.5~53.6pJ/pixel energy efficiency
  - At least 7x better power efficiency than previous designs (at least 3x better excluding technology factors)