A Low Voltage Buck DC-DC Converter Using On-Chip Gate Boost Technique in 40nm CMOS

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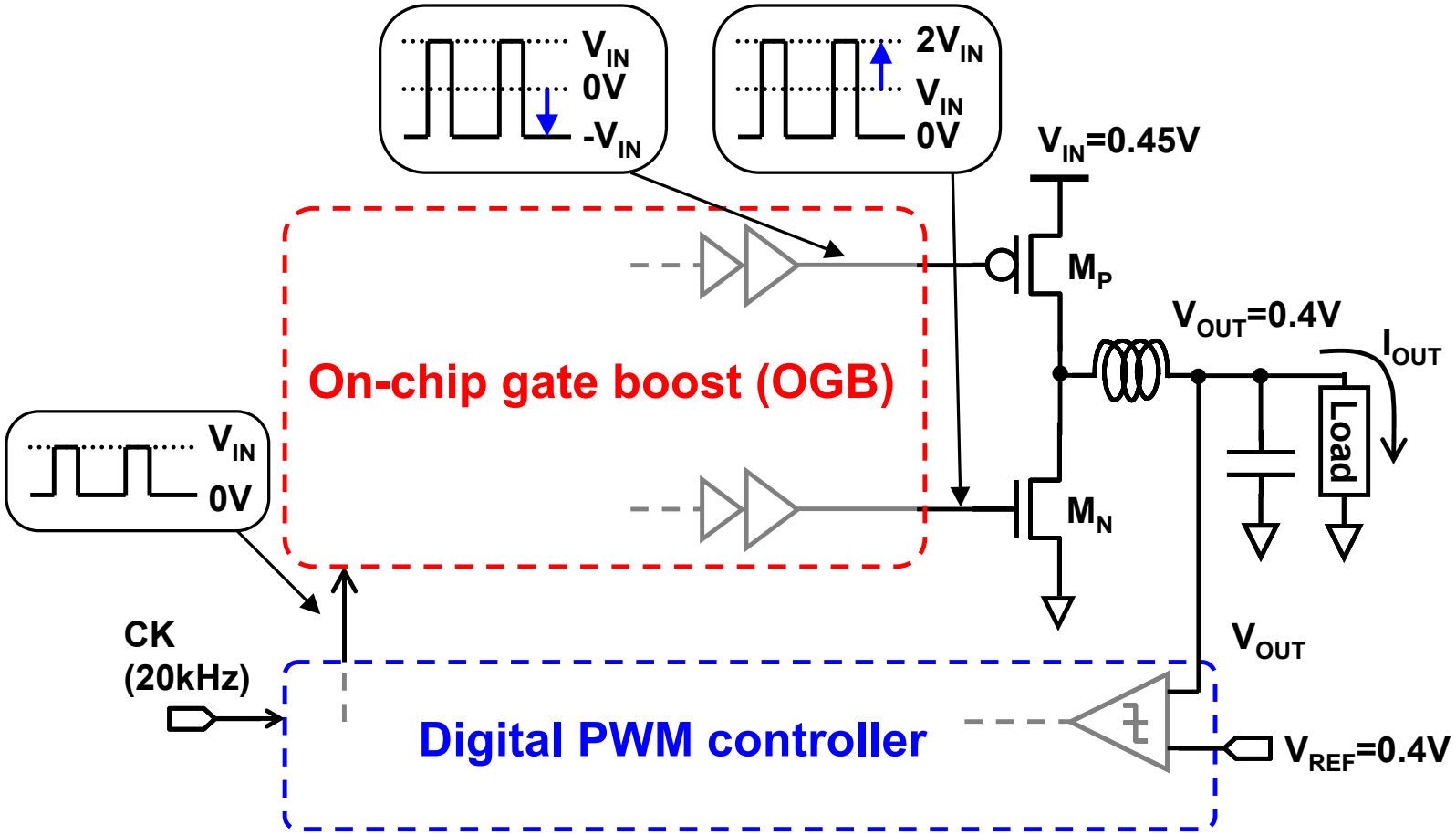
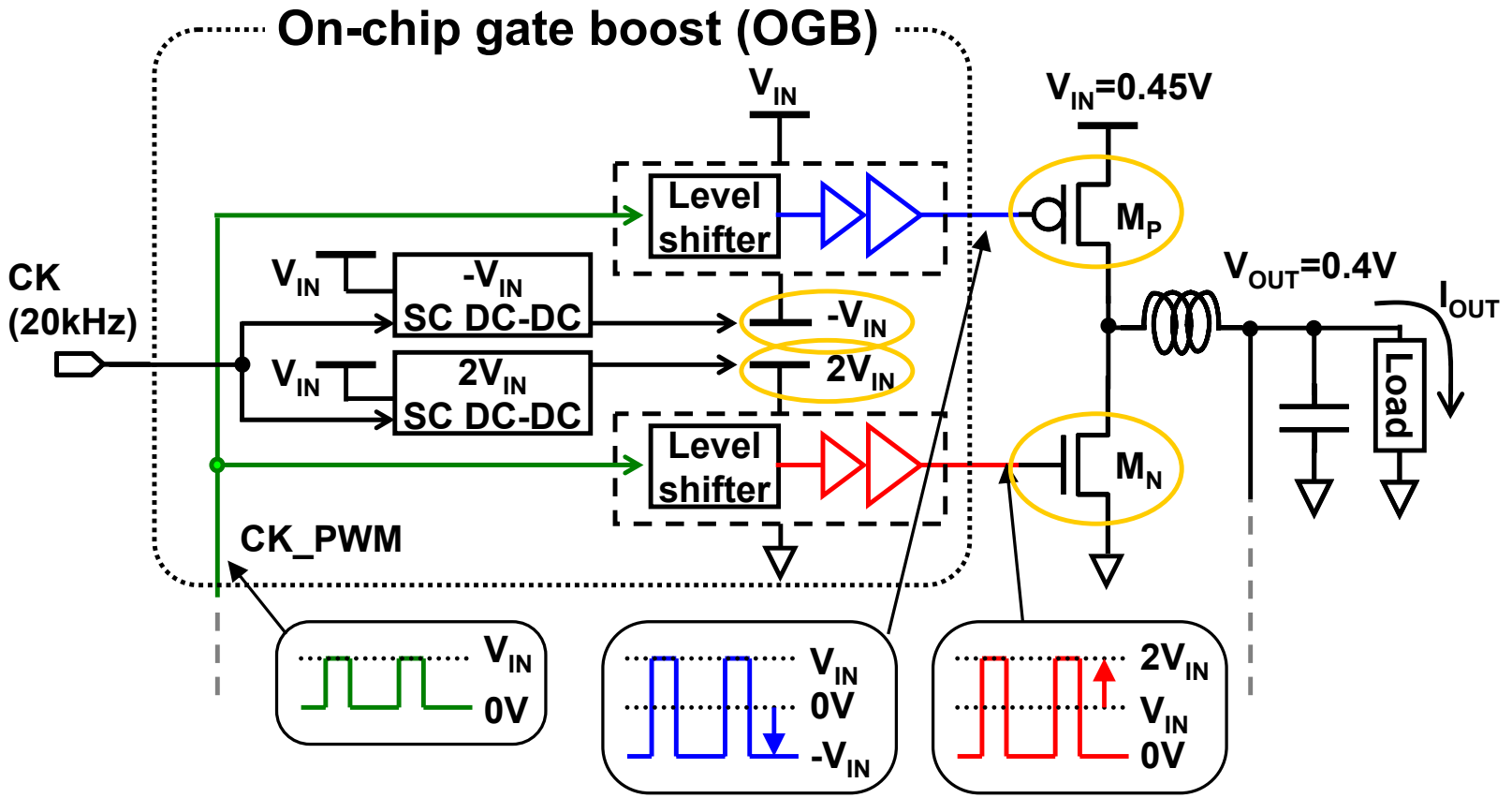
Simplified top level diagram of proposed buck converter



☺ On-Chip Gate Boosting (OGB) for lower R_{ON}.

☺ Digital PWM controller for low quiescent power.

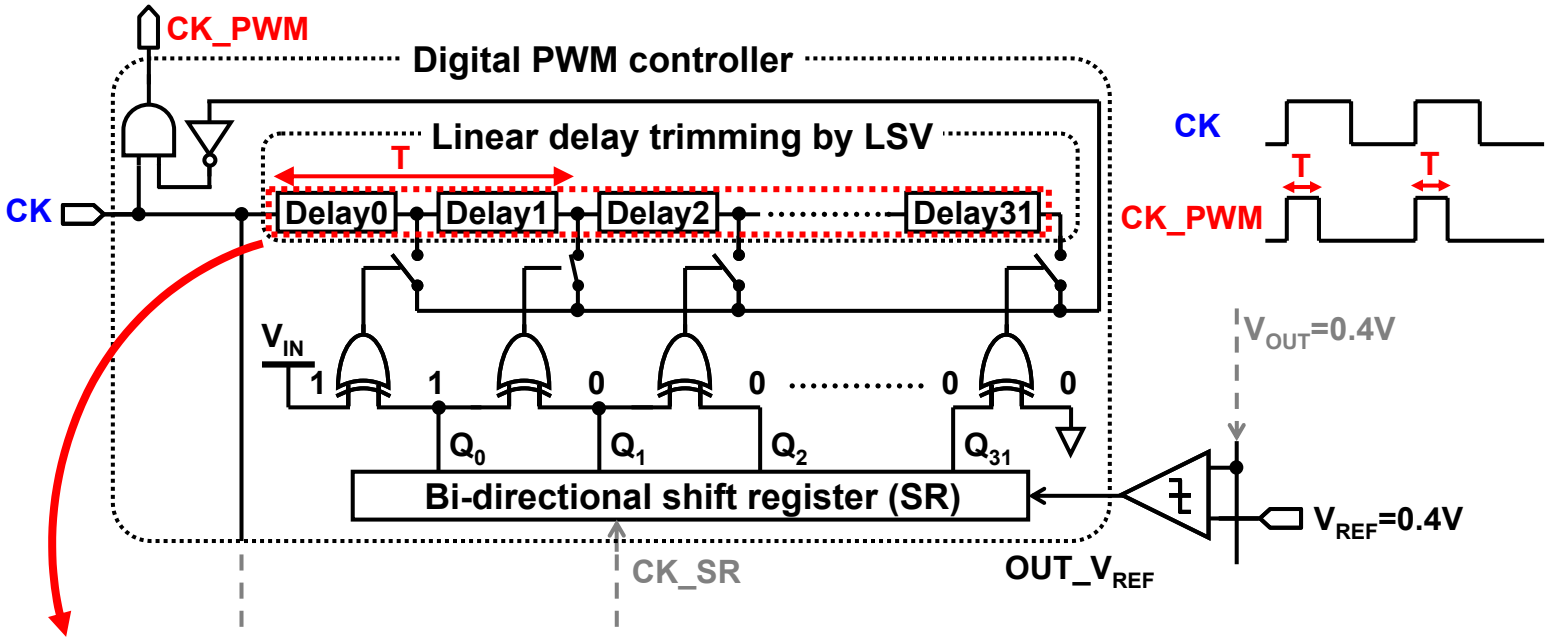
On-chip gate boost for power transistors

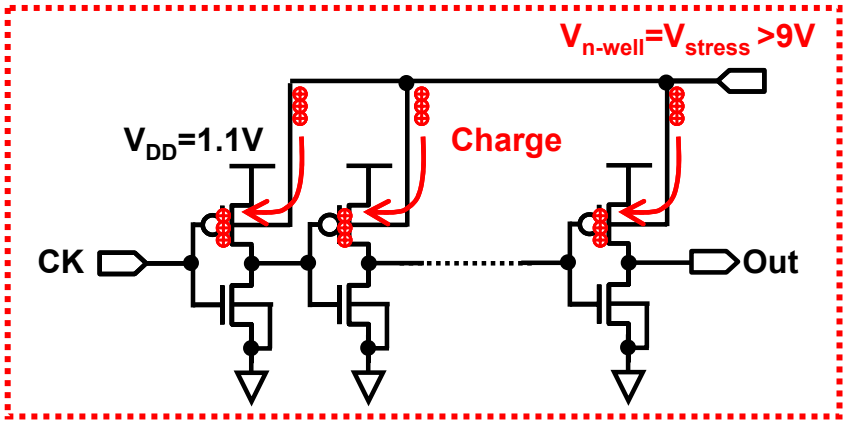


■ 2 power rails are generated by on-chip switched-capacitor (SC) DC-DC converters.

→ Loss in M_P and M_N is reduced.

0.45-V digital PWM controller with delay trimming

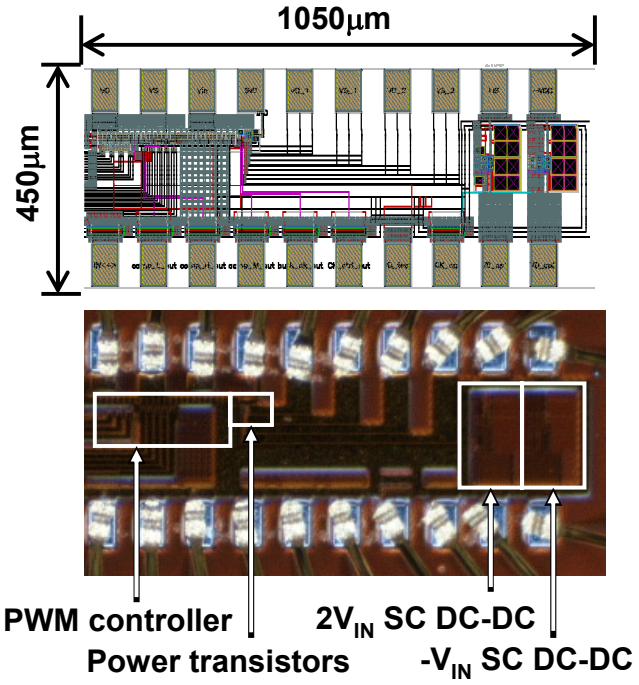


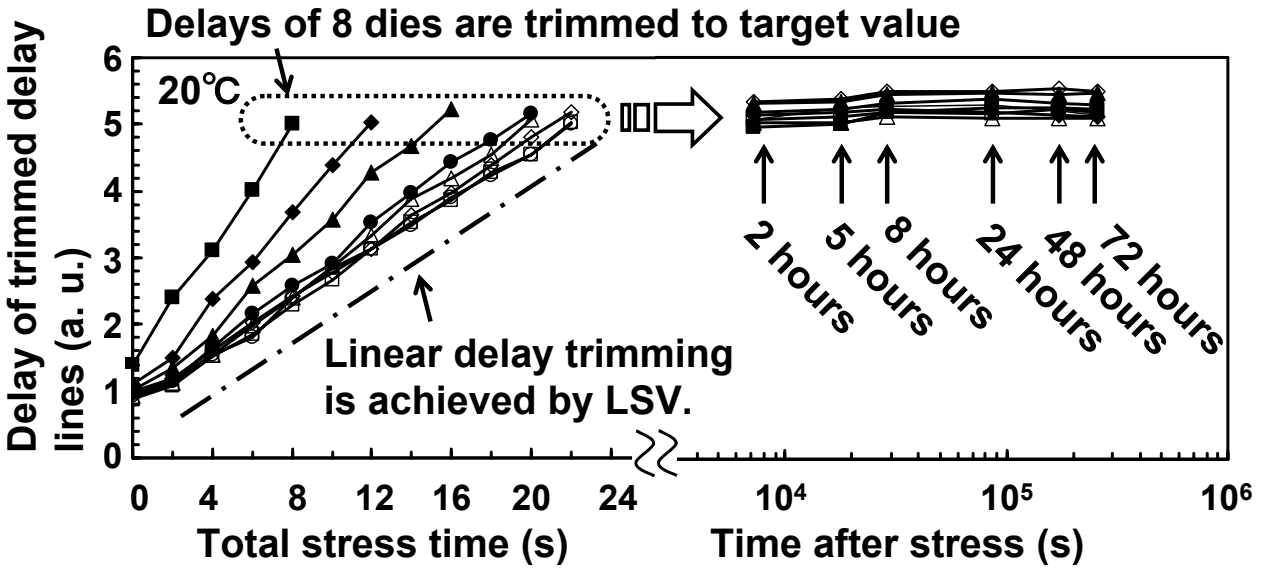


■ Instead of conventional analog feedback control, a delay-line based digital PWM controller has been designed for 0.45-V operation.

■ Delay trimming by charge injection is used to compensate for large die-to-die variations at low VDD.

Chip photo and measured delay trimming





- Chip is fabricated in 40nm CMOS.
- Target delay of delay line is set to 5 times of initial delay to show the controllability.
- Linear trimming is achieved for 8 dies.
- No significant retention degradation is observed.

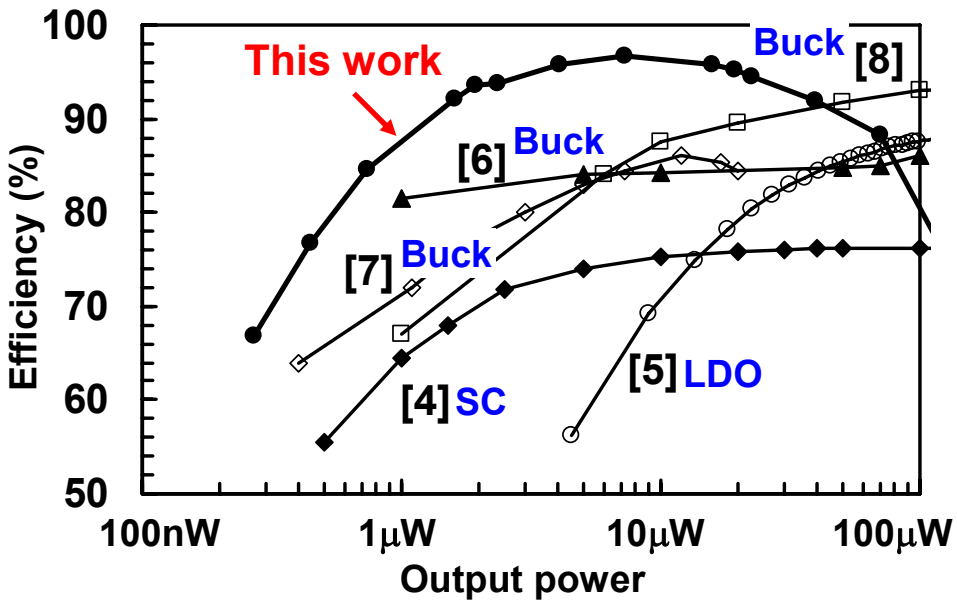
Performance summary & comparison

Performance summary

Technology	40-nm CMOS
Input voltage	0.45V
Output voltage	0.34V~0.44V
Output power	270nW~165μW
Output ripple	<5mV
Max. efficiency	97% at 7μW
Quiescent power at I_{OUT}=0	140nW
Active area	0.043 mm²

Comparison with published DC-DC converters

Reference	[4] ISSCC 2008	[5] CICC 2010	[6] ISSCC 2007	[7] VLSI 2010	[8] VLSI 2011	This work
Type	Switched-capacitor	LDO	Buck	Buck	Buck	Buck
CMOS	65nm	65nm	65nm	130nm	250nm	40nm
Input voltage (V)	1.2	0.5	1.2	1.8	1.2	0.45
Output voltage (V)	0.5	0.45	0.5	0.575	1.0	0.4



■ By virtue of proposed techniques, this buck DC-DC converter achieves:

☺ High peak efficiency of 97%,

☺ Low quiescent power of 140nW,

☺ Lowest input and output voltage,

☺ Highest efficiency to date for output power less than 40μW.