WASEDA University
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A 6.72-Gb/s, 8pJ/bit/iteration WPAN LDPC Decoder in 65nm CMOS

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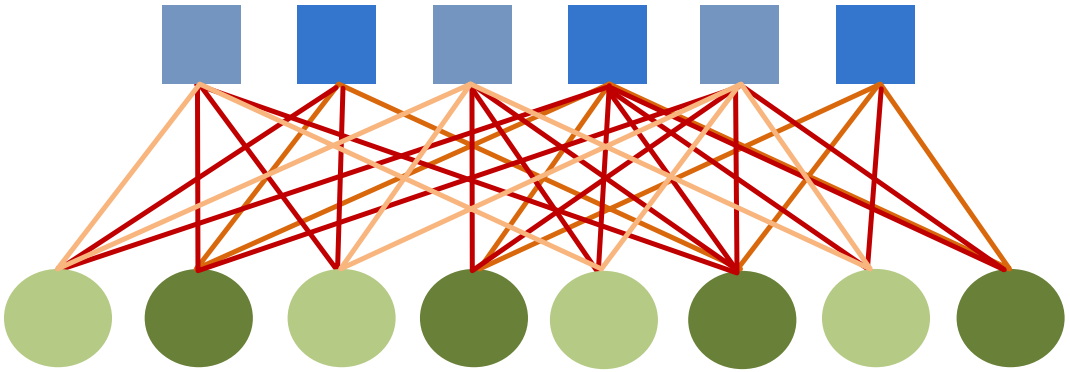
Design Problem

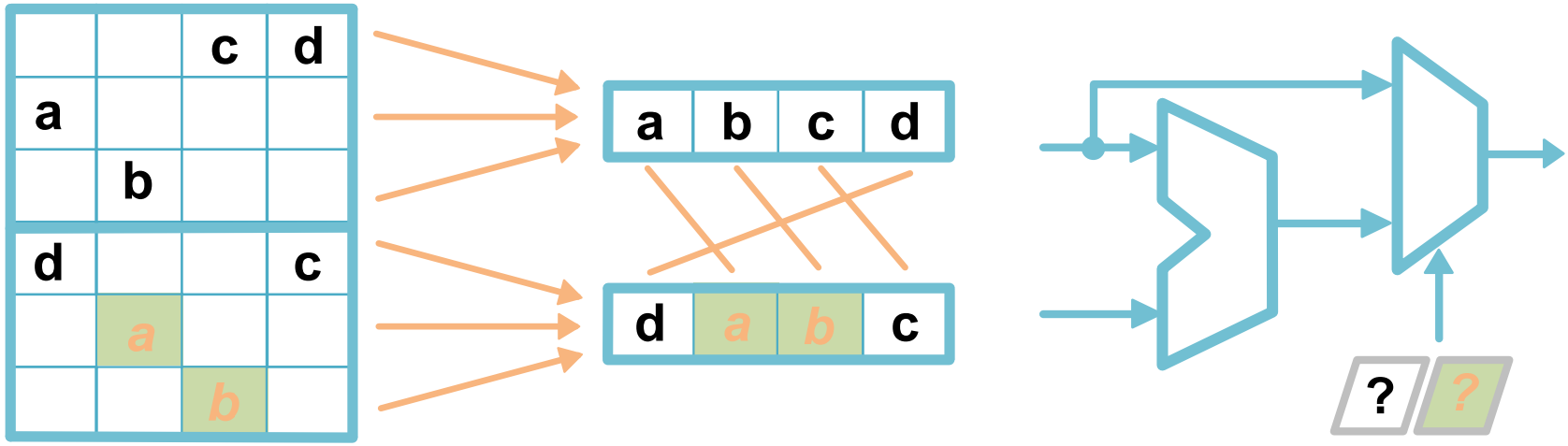
- **Wireless Personal Area Network (WPAN)**
  - *IEEE 802.15.3c Standard (2009)*
  - *Up to 5.75Gbps air throughput*
  - *LDPC codes with 4 code rates*
- **Problem on WPAN LDPC Decoder**
  - *High parallelism decoding*
  - *Multi-code configurability*

Make permutation network (PN) *NOT Implementable*



Proposed Idea

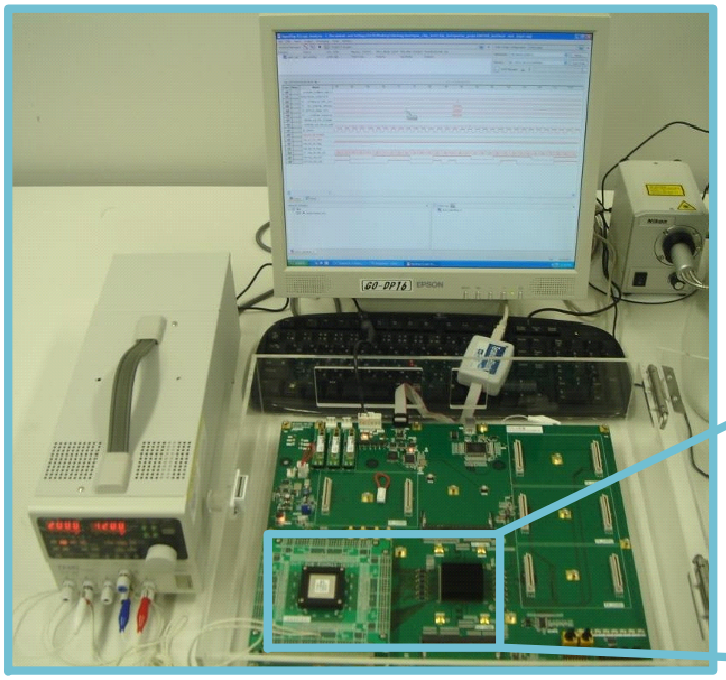
- **Virtual sub-block for enhanced PCM* based data permutation**
  - *Fully reused PN with **zero** logical gate but signal wires only*
- **Bypass data flow for original PCM based decoding**
  - *Two-to-one MUX controlled by an efficient look up table*

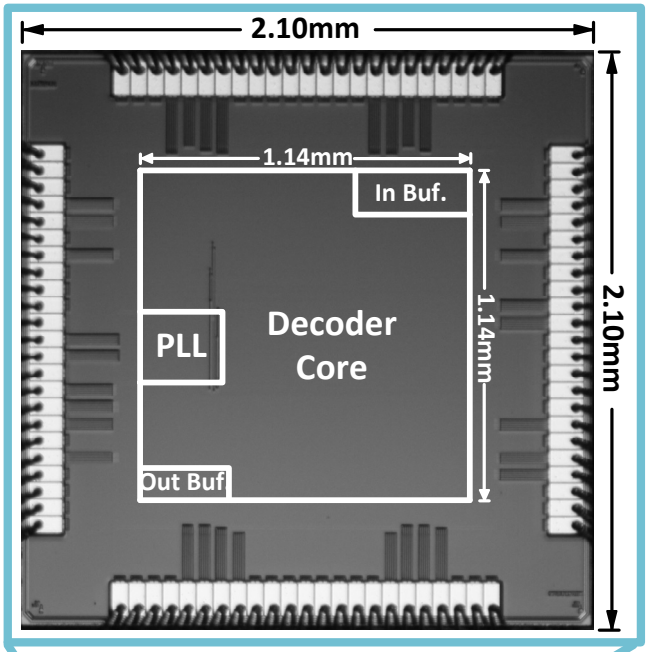


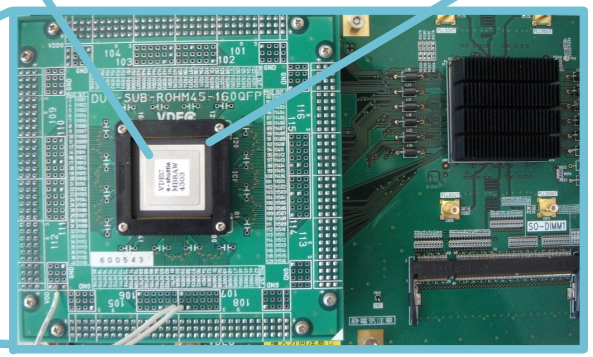
*Parity Check Matrix

Chip Implementation and Test

Technology	E-Shuttle 65nm LVT CMOS
Die Area	2.1mm×2.1mm
Core Area	1.14mm×1.14mm
Density	86.3%
Max. Clock	450MHz @ 1.2V

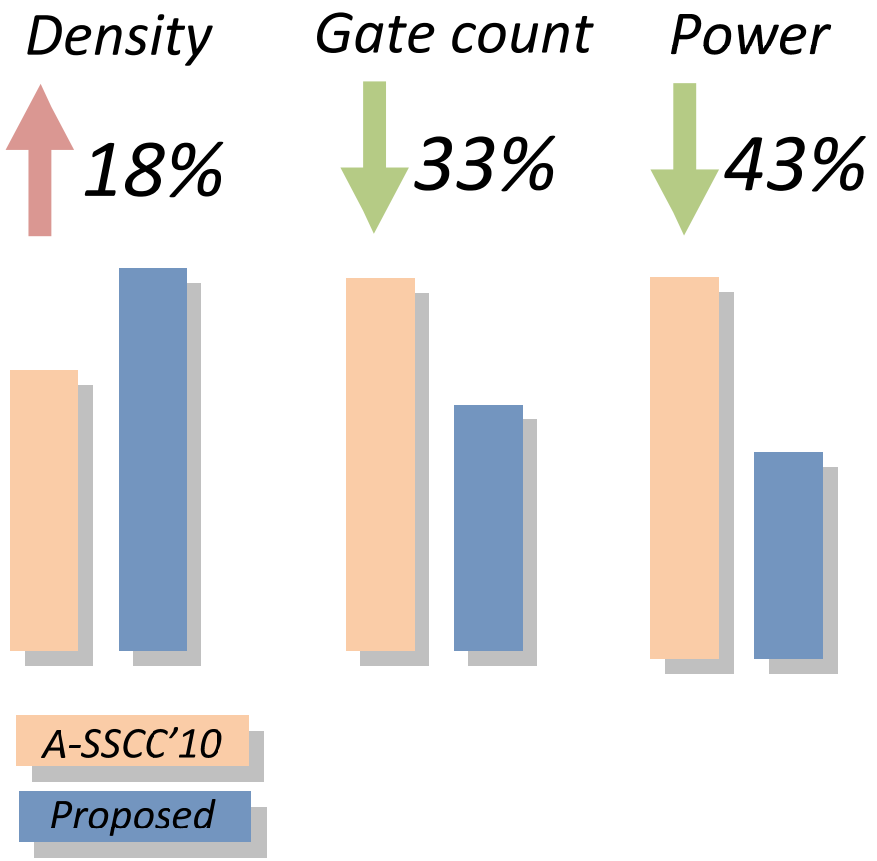






Performance Compare

	Proposed H-profile	Proposed L-profile	Hung A-SSCC'10
Process (nm)	65		65
Area (mm^2)	1.30		1.56
Density	***86.3%***		***73.3%***
Gate Count	***430K***		***647K***
Data rate (Gbps)	6.72		6.6
Voltage (V)	1.2	1.0	1.0
Clock (MHz)	400	200	197
Iteration	10	5	5
Power (mW)	537.6	***209.8***	***361***
Energy eff.	8.0	***6.2***	***10.9***



The End…

Thank you

for your attention!