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ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Statistical Analysis of BTI in the Presence of Process-induced Voltage and Temperature Variations

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Motivation

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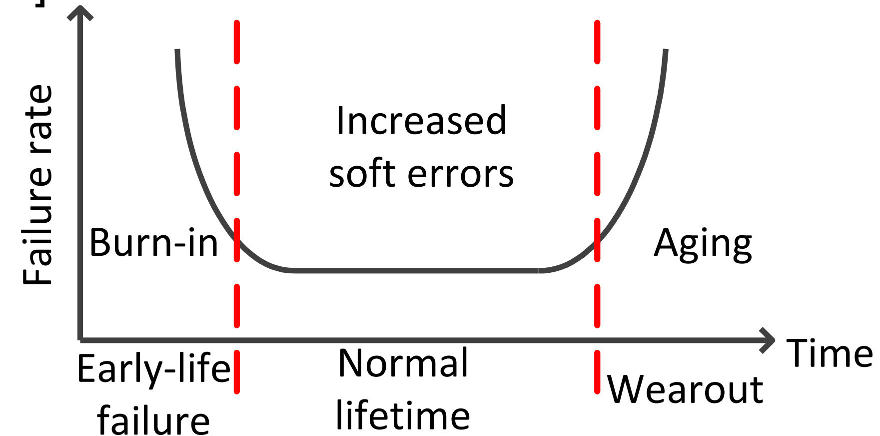
- With CMOS scaling
  - Transient errors [Baumann05TDMR]
  - Aging [Agostinelli05IRPS]
    - Bias Temperature Instability (BTI)
  - Process variation [ITRS]

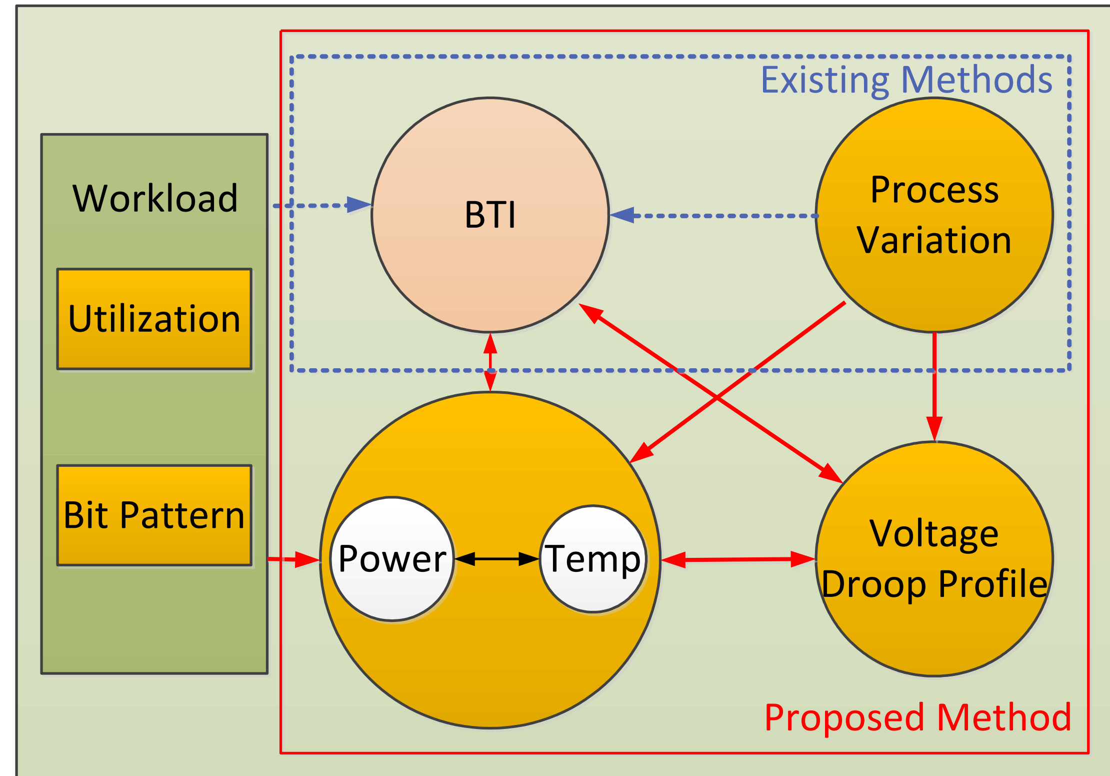


[Mitra11ETCAS]

- Malfunctions in systems [Mitra11ETCAS]
  - Annoying computer crashes
  - Loss of data and services
  - Financial and productivity losses
  - Loss of human life

Motivation

- Variation sources
  - Process Variation
  - Run-time
    - Aging
    - Voltage
    - Temperature



- All these phenomena are tightly coupled
- To accurately predict timing
  - Combined effect of all phenomena on timing has to be considered.

Purpose

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- Voltage, temperature, and aging aware Statistical Static Timing Analysis (SSTA)
  - Combined effect of PVT variations and BTI-induced delay degradation
- Probabilistic method to obtain
  - Thermal and voltage droop profiles in the presence of process variation
  - Effect of BTI-induced threshold voltage shift is considered
- Analytical technique for estimating
  - BTI effect under process variations
  - Voltage-temperature variations → process and workload variations

Outline

- Related work
- Preliminaries and models
- Proposed method
- Experimental results
- Summary and conclusion

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Related work

- [Wang 08CICC]: New V_{th} model
  - To capture variation of BTI in presence of process variation
- [Lu09DAC]: Comprehensive reliability framework
  - Considering both BTI and process variation
- [Siddiqua11ISQED]: Effect of BTI and process variation
  - Register file and Kogge-Stone adder
- [Han11ICCAD]: Transistor level simulation using Monte-Carlo
  - Considering aging and process variation

- Effect of temperature and voltage-droop is neglected
  - Significant inaccuracy in BTI estimation
  - Considerable error in BTI-induced delay degradation

Outline

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  - Bias Temperature Instability (BTI)
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BTI

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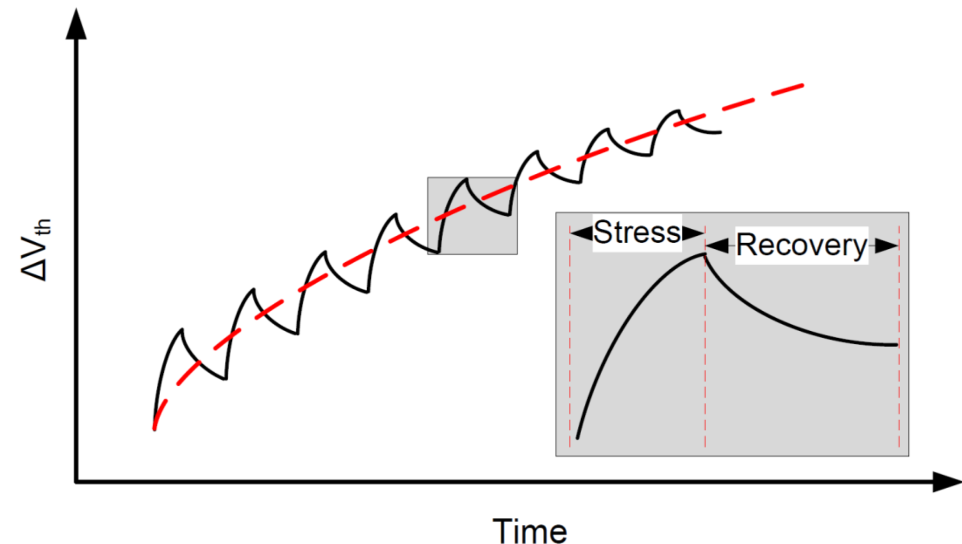
- Bias Temperature Instability (BTI)
  - NBTI: Negative BTI → PMOS threshold ↑
  - PBTI: Positive BTI → NMOS threshold ↑
- Two phases:
  - Stress → V_{TH}↑
    - PMOS (NMOS) transistor is under negative (positive) bias
  - Recovery → V_{TH}↓
    - When the bias is removed



BTI

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- Modelling [Bhardwaj06CICC]:

$$\Delta V_{th}(\delta, T, V_{dd}, t) = \left(\frac{\sqrt{{K_v}^2 \delta T_{clk}}}{1 - \beta(t)^{1/2n}} \right)^{2n}$$

$$K_v = f(V_{dd} - V_{th}, T)$$

  - δ: Duty cycle
  - T: Temperature
  - V_{dd}: Gate supply voltage
  - V_{th} : Transistor threshold voltage
  - Other parameters:
    - Technology and fabrication dependent constants

BTI

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- Intrinsic variation
  - Fluctuation of generated BTI-induced interface traps [Han10ICCAD]
    - Similar to random dopant fluctuation

$$\sigma(\Delta V_{th}(t)) = \sqrt{\frac{K}{L.W}\mu(\Delta V_{th}(t))}$$

- *L*: gate length
- *W*: gate width
- $\mu(\Delta V_{th}(t))$: mean of threshold voltage change
- *K*: constant

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Process variation

- Variation of physical parameters [Xiong07CAD]

$$\Delta P_{total} = \Delta P_{d2d} + \Delta P_{cor} + \Delta P_{rand}$$

  - ΔP_{d2d} : die to die variation
  - ΔP_{cor} : spatially correlated variation
  - ΔP_{rand} : independent random variation
- To keep track of correlations
  - Principal Component Analysis (PCA) is used

$$\Delta L_i = \sum_{j=1}^{n} \alpha_{j,i} PC_j + \mu_i$$

  - $\alpha_{j,i}$:depends on covariance matrix
  - μ_i : mean value of ΔL_i

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  - Statistical profiling
  - Runtime variation aware SSTA
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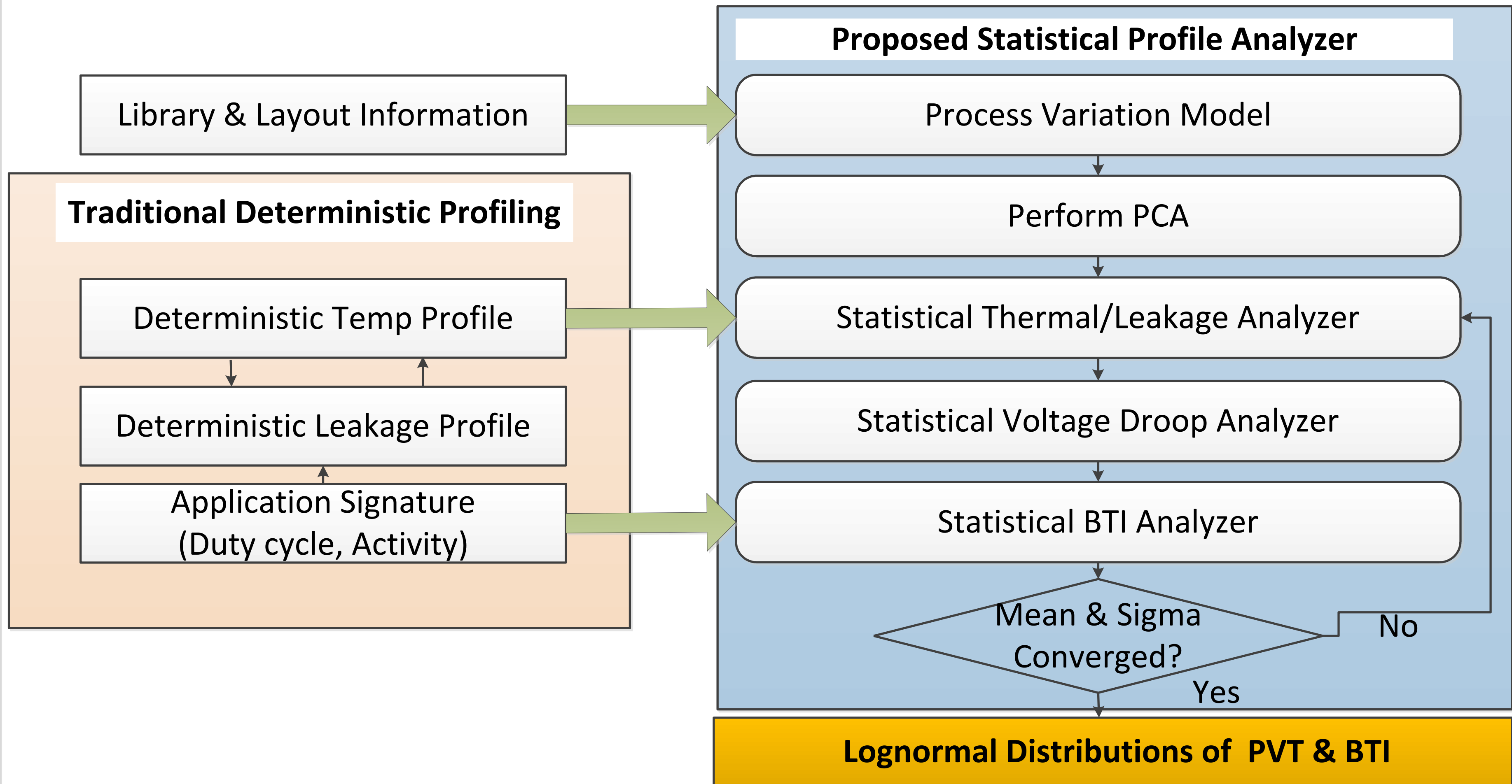
Overall Profiling flow



Overall profiling flow

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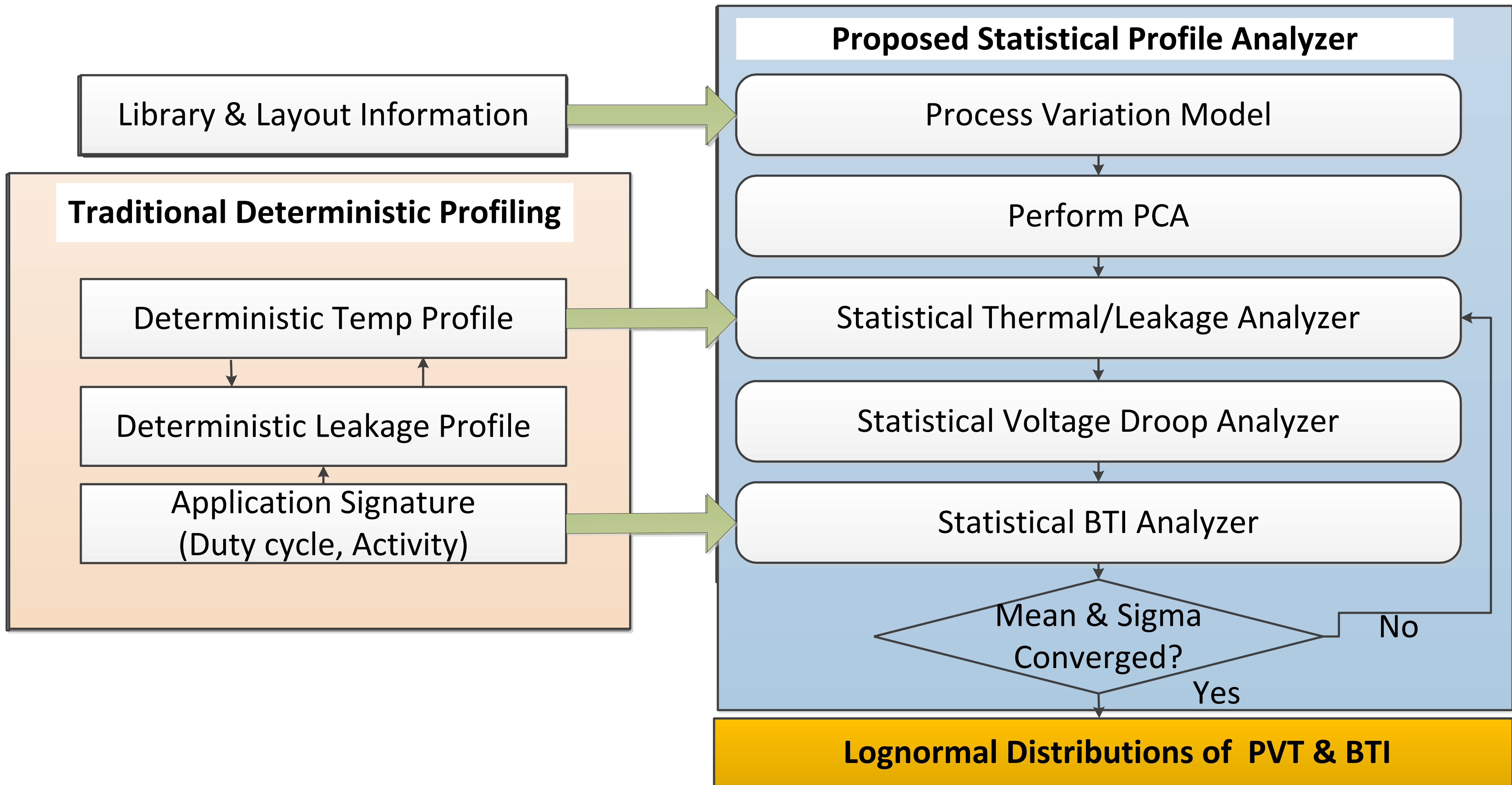
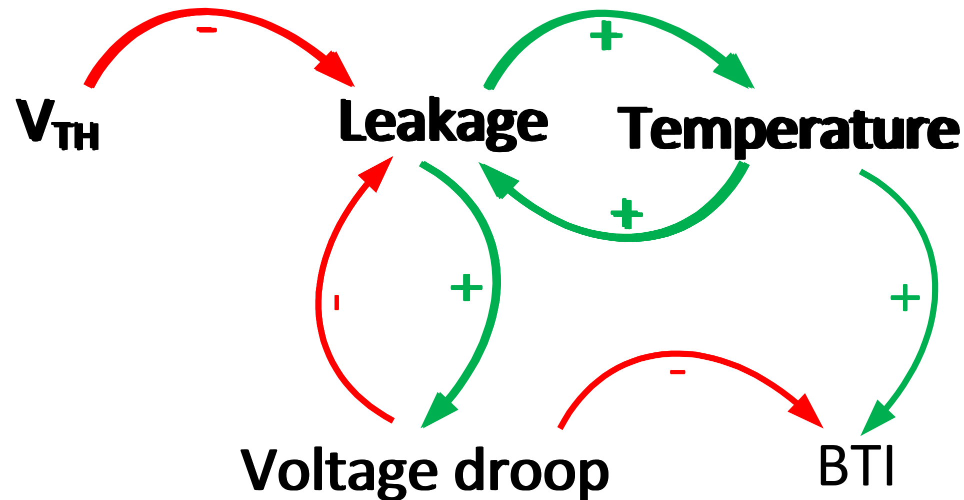


Step1:Removing Correlation among PVT and BTI



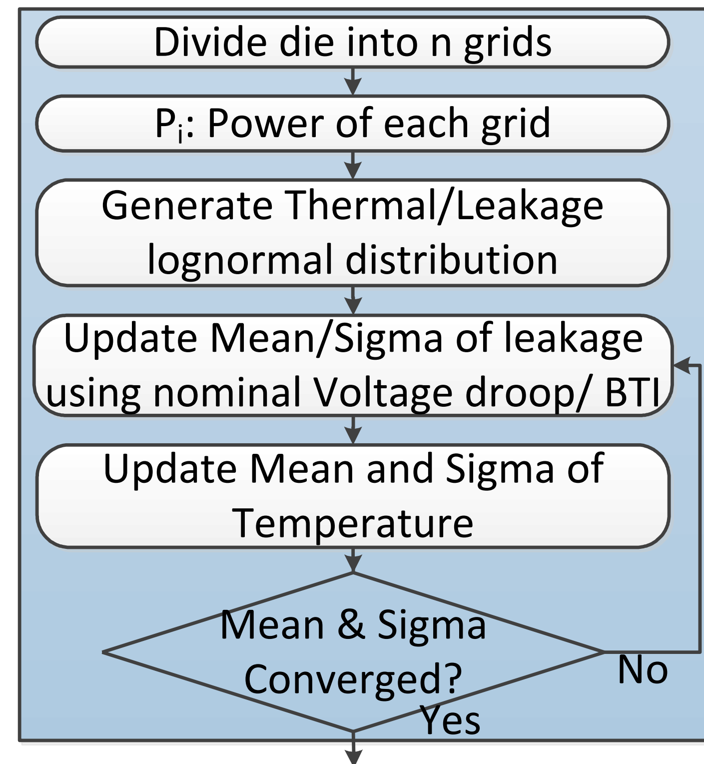
- PCA is used
  - To keep track of the correlations
  - By converting spatial correlated variables
    - Set of uncorrelated orthogonal variables

Step2: Statistical Thermal Profile

- Leakage and temperature: lognormal distributions

$$L_A = \exp(A), \qquad A = \mu_A + \sum_{i}^{n} a_i . X_i$$

- Convergence
  - Less than 10 iteration



Step2: Statistical Thermal Profile

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- Leakage

$$P_{leakage} = P_{leakage}^{nominal}(1+\alpha_1 T + \alpha_2 T^2)(1+\alpha_3 V + \alpha_4 V^2)(1+\alpha_5 \Delta V_{th} + \alpha_6 \Delta V_{th}^2)\exp(\beta \Delta L)$$

  - $P_{leakage}^{nominal}$ nominal leakage without process variation at *T=0°C*
  - α_i fitting parameter
  - Verified by SPICE simulation ($R^2>0.996$)
    - For a 7-stage ring oscillator in 45 nm technology
- Temperature

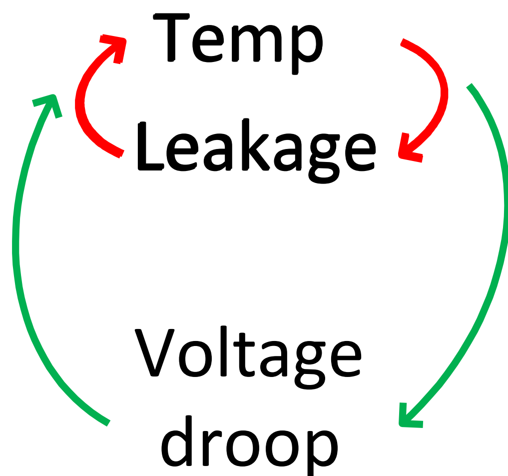
$$T_i = \sum_{j=1}^{n} \alpha_{ij} P_j + \alpha_{im} P_m$$

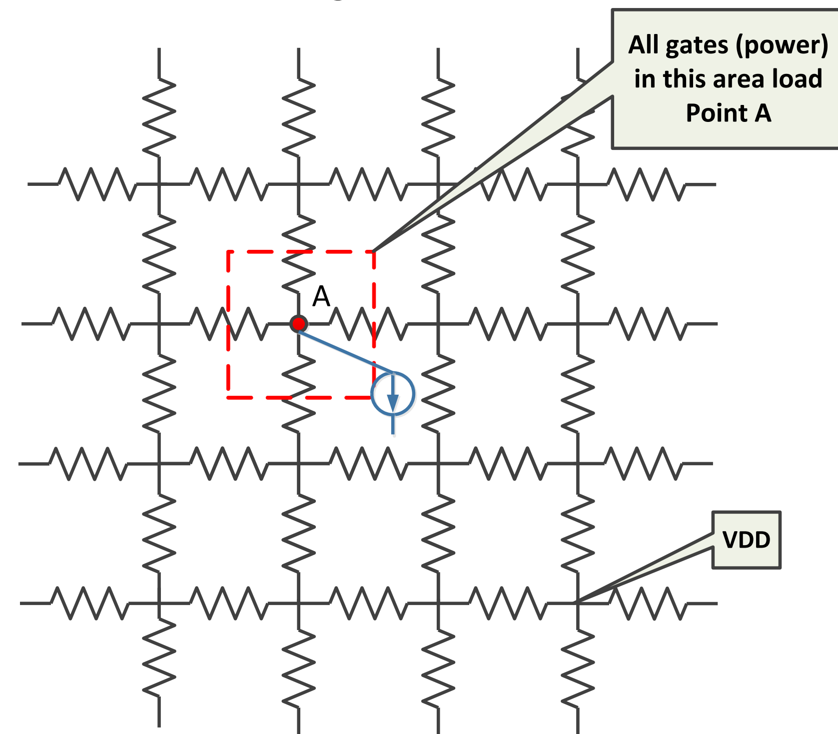
  - P_j power of grid j
  - P_m chip to ambient removing power

Step3: Statistical voltage droop profile

$$V = G^{-1} I$$

- New flow consists of two nested loops
  - Temperature-leakage loop
  - Outer loop to find lognormal distribution of voltage droop
- Convergence
  - Less than 10 iterations

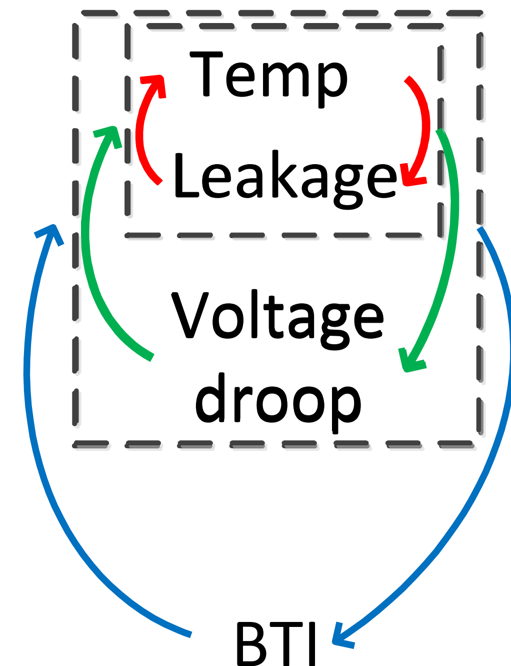




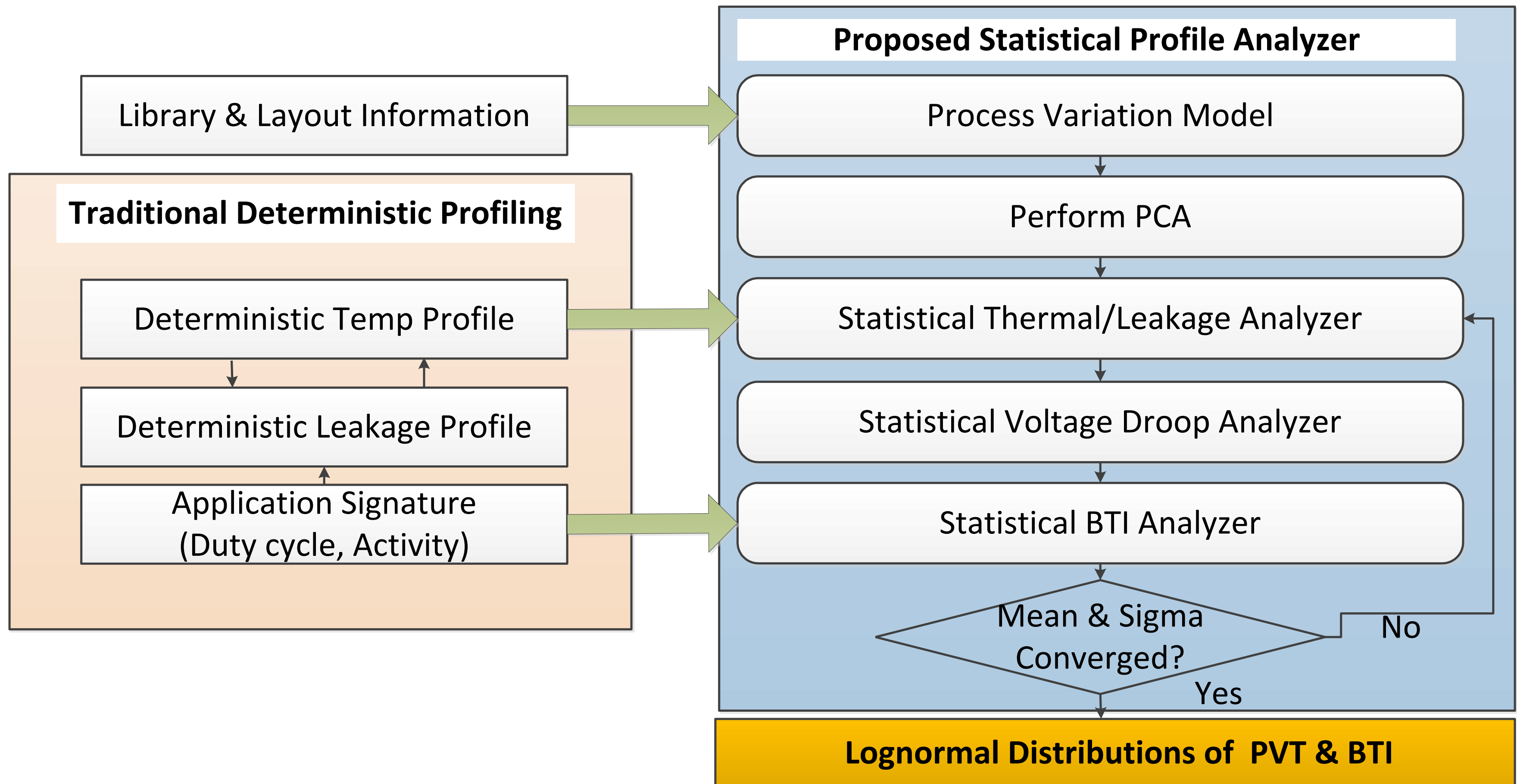
Step4: Statistical BTI Analysis

- BTI effect strongly depends
  - Thermal profile & Voltage droop profile
- BTI affects leakage by V_{th} change
  - Temperature &Voltage droop

- BTI is modeled as lognormal distribution
- BTI profiling consists of three nested loops
  - Two inner nested loops for extracting
    - leakage, thermal, and voltage droop profiles
  - The outer loop for obtaining the BTI profile
- Convergence
  - Less than 10 iteration



Overall flow



Time Scale and Workload Variation

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- Different variations have different time scales
  - Short term effects (ms)
    - temperature and voltage droop variations
  - Long term effects
    - BTI
    - Function of duty cycle → workload dependent
- Operational lifetime of the chip
  - is divided into some equal time intervals
- For each of these time intervals
  - PVT/BTI profiles are calculated
  - BTI is estimated based on previous interval
    - Temperature, voltage droop, and duty cycle

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Aging-aware timing analysis

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- Delay of the gate at time *t* can be expressed

$$D(t) = D_0 + \Delta D_0 + \Delta D_{BTI}(t)$$

- Suppose the gate length is the only source of variation

$$\Delta D(t) = \Delta D_0 + \Delta D_{BTI}(t)$$

$$= \left(\frac{\partial D}{\partial L} \Delta L + \frac{\partial D}{\partial V_{th}} \frac{\partial V_{th}}{\partial L} \Delta L \right) + \left(\frac{\partial D}{\partial V_{th}} \left(\Delta V_{th}^{BTI}(t) + \frac{\partial V_{th}^{BTI}(t)}{\partial L} \Delta L \right) \right)$$

- According to [Chen09ICCAD]

$$\Delta D_0 = \alpha.\Delta PP + \beta.\Delta T + \gamma.\Delta V$$

- ΔD_{BTI} can be written

$$\Delta D_{BTI}(t) = A_{BTI} \delta^n t^n \left(1 + \alpha_{BTI} \Delta L + \beta_{BTI} \Delta T + \gamma_{BTI} \Delta V\right).$$

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Experimental setup

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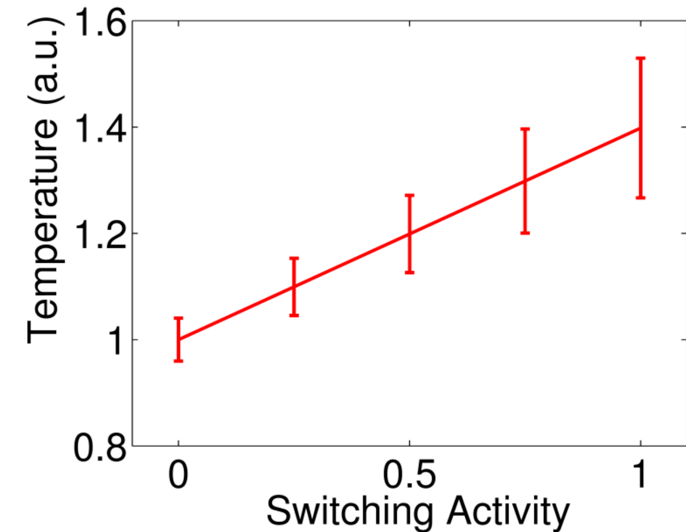
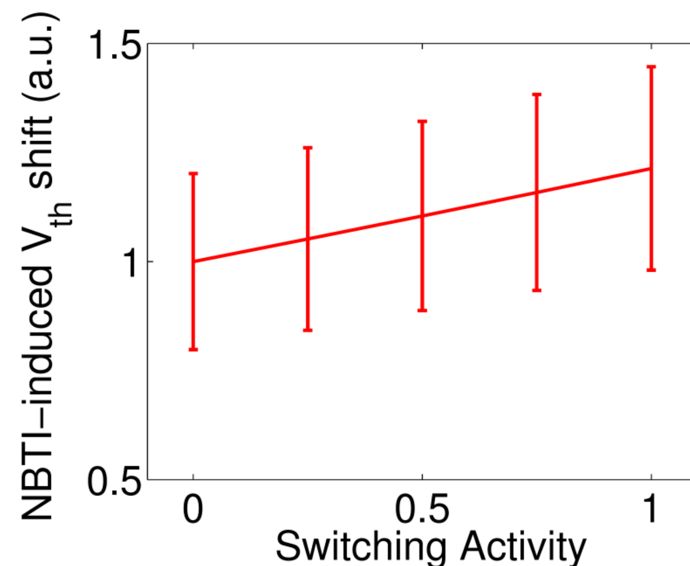
- Circuits
  - ISCAS85
  - Illinois Verilog Model (IVM) processor
- Synthesized by Synopsys Design Compiler
  - Using Nangate 45 nm library
- Total amount of variation
  - $\frac{3\sigma}{\mu} = 20\%$
- Sensitivity of leakage and delay to different parameters
  - SPICE simulation

Workload variation

- Different workload
  - Dynamic power
  - Temperature
  - Duty cycle
  - BTI



- Workload in 7-stage inverter chain
  - Up to 40% temperature
  - Up to 15% NBTI-induced ΔV_{th}



Statistical thermal/BTI profiling

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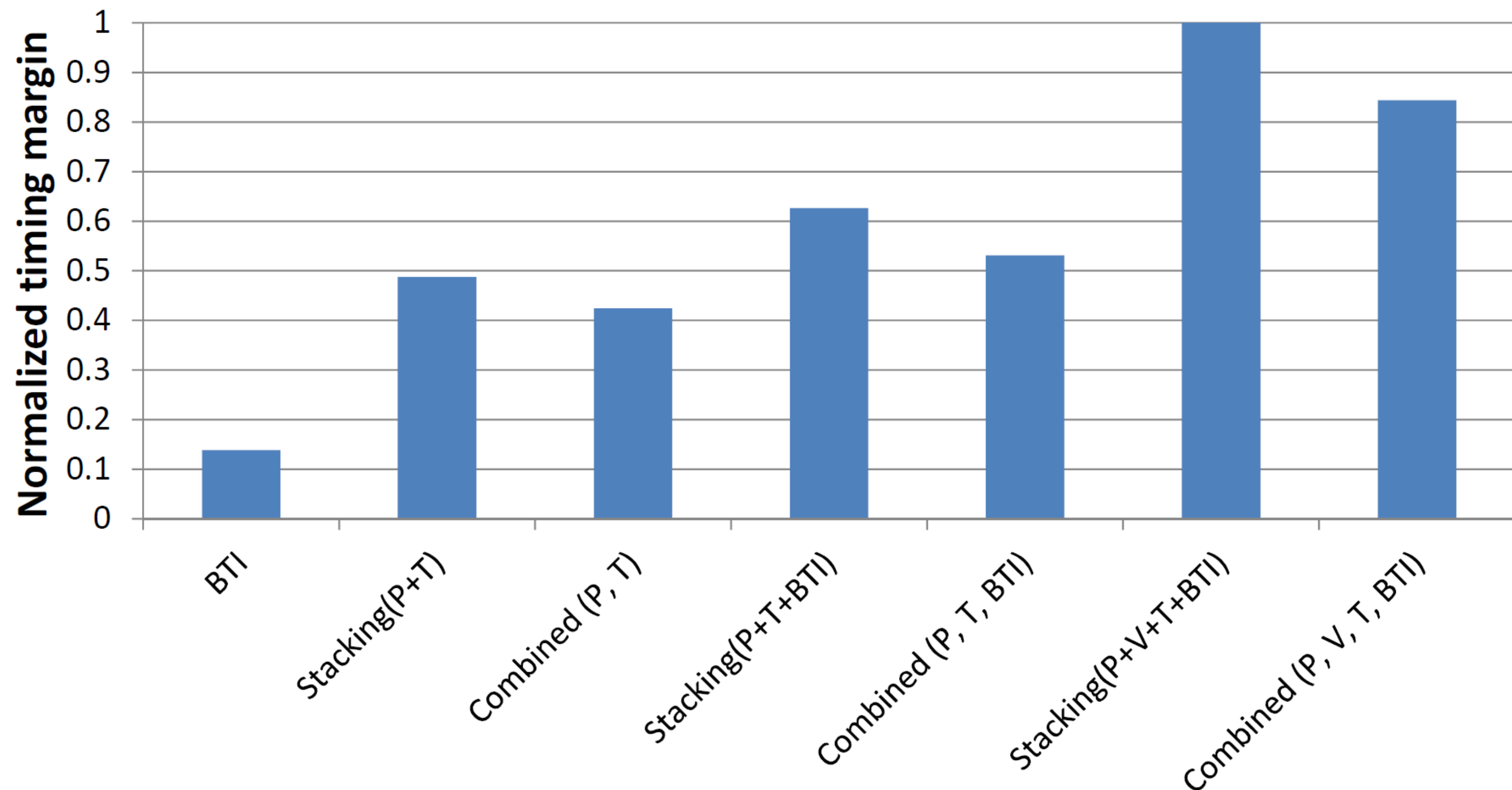
- Error of incomplete consideration of
  - Interdependence among PVT and BTI
  - Compared with $+T+V+B$
  - For a 7-stage inverter chain

	$Temp_{max}$	μ_{Temp}	σ_{Temp}	$\mu_{\Delta Vth}$	$\sigma_{\Delta Vth}$
$+T-V-B$	89.23%	2.38%	67.00%	8.54%	14.54%
$+T+V-B$	14.09%	0.50%	13.60%	0.00%	1.03%
$+T-V+B$	38.07%	1.61%	38.40%	8.54%	12.14%

- T: temp
- V: voltage droop
- B: BTI
- +/- : consideration/ignorance

Timing margins

- Simple margin addition method for *ALU* of *IVM*
  - Results in about 16% overestimation of timing margin



Proposed VTA-SSTA accuracy/runtime

- Previous work
  - Effect of temperature/voltage droop on BTI is ignored
- 100,000 Monte-Carlo samples

Circuit	Monte-Carlo			Previous work		Proposed method		
	μ	σ	Runtime (sec)	μ	σ	μ	σ	Runtime improvement
C2670	157.21	17.47	374	1.28%	12.95%	0.20%	5.15%	137x
C3540	456.02	45.39	1074	1.22%	12.51%	0.69%	6.65%	205x
C5315	216.48	23.07	1446	1.24%	12.92%	0.34%	4.37%	540x
C7552	157.59	17.14	2906	1.29%	13.26%	0.34%	3.76%	681x
S13207	878.66	81.79	10173	1.23%	11.31%	0.41%	4.53%	1027x
S35932	238.42	21.41	51407	1.41%	14.01%	0.43%	5.62%	1570x
S38417	817.04	90.43	48730	1.35%	13.04%	0.37%	4.51%	1315x
Average				1.25%	12.25%	0.38%	4.85%	576x

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Summary and conclusion

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- Analytical methodology
  - Model the correlation between PVT and BTI-induced aging
- Voltage, temperature, and aging aware
  - Statistical Static Timing Analysis (VTA-SSTA)
- Neglecting interaction among different sources of variation
  - Considerable error in thermal-voltage profiling
  - Unnecessary design margin (16% overdesign)
    - Performance loss

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- Thanks for your attention
- Any question?