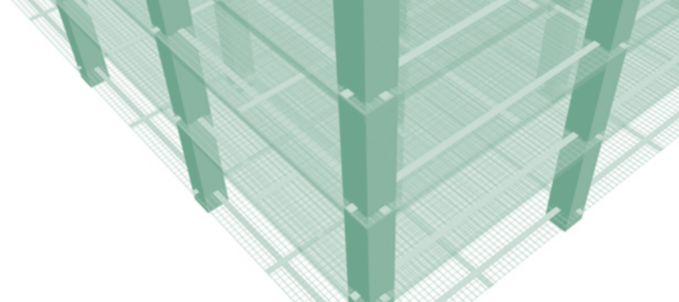
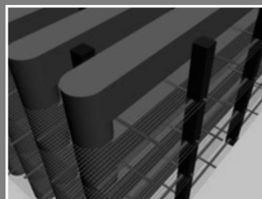
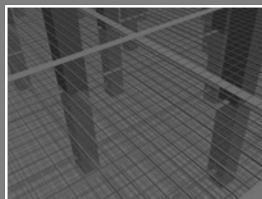
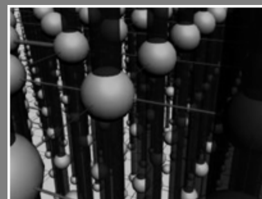


Block-level Designs of Die-to-Wafer Bonded 3D ICs and Their Design Quality Tradeoffs







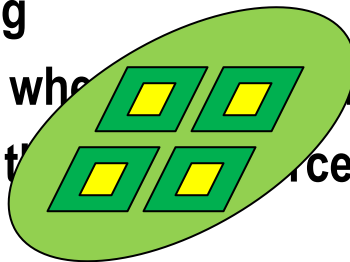
Krit Athikulwongse, Dae Hyun Kim, Moongon Jung, and Sung Kyu Lim
Speaker: Shreepad Panth
School of ECE, Georgia Institute of Technology, Atlanta, GA

ASPDAC 2013 (Jan 25, 2013)

Near Future 3D ICs

- Wafer-to-wafer bonding is a low cost process, but it requires that all dies have the same size

- In several cases, die-to-wafer bonding is more practical than wafer-to-wafer bonding and still low-cost
  - Memory + logic stacking
  - Logic-to-logic stacking whe re from different companies
  - Designs with IP blocks t ce different size of dies in the stack



- In near future, block-level designs are likely to be early 3D ICs on the market because the methodology allows the reuse of optimized IP blocks

Related Work

- **TSV position is an important design factor that limits the quality of 3D ICs in terms of:**
  - **Performance: area, wirelength, delay, and power**
  - **Reliability: temperature and mechanical stress**

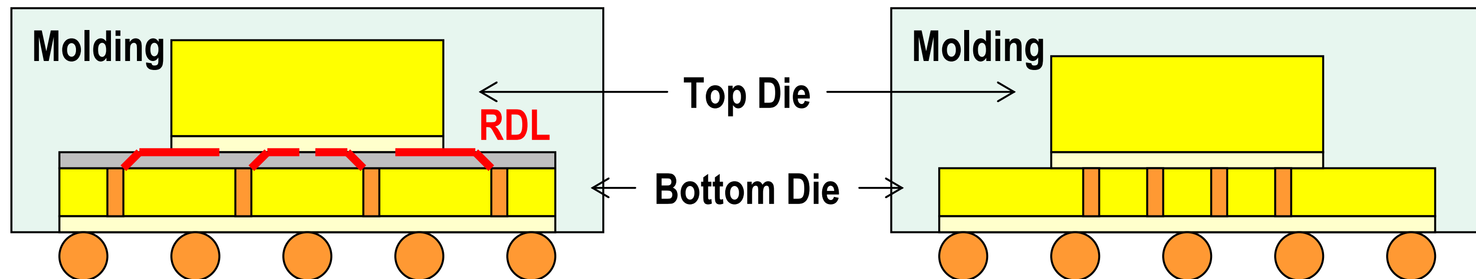
- **No previous work has studied the quality trade-offs between different styles of block-level layout of die-to-wafer bonded 3D ICs in a holistic manner**

Problem Statement (I)

- **A 2-tier 3D IC is focused in this work**
- **Both dies are facing down**
  - **Compatibility with popular flip-chip packaging**
  - **Heat sink attached on back side of the top die for good cooling**
- **Bottom die has larger footprint than top die**
  - **Large area available for C4 bumps for good power delivery**

Problem Statement (II)

- Redistribution layer (RDL)
  - Necessary if some TSVs in bottom die are outside the footprint of top die
  - Not needed if all TSVs in bottom die are inside the footprint of the top die



Problem Statement (III)

- **Layout of the top die is fixed**

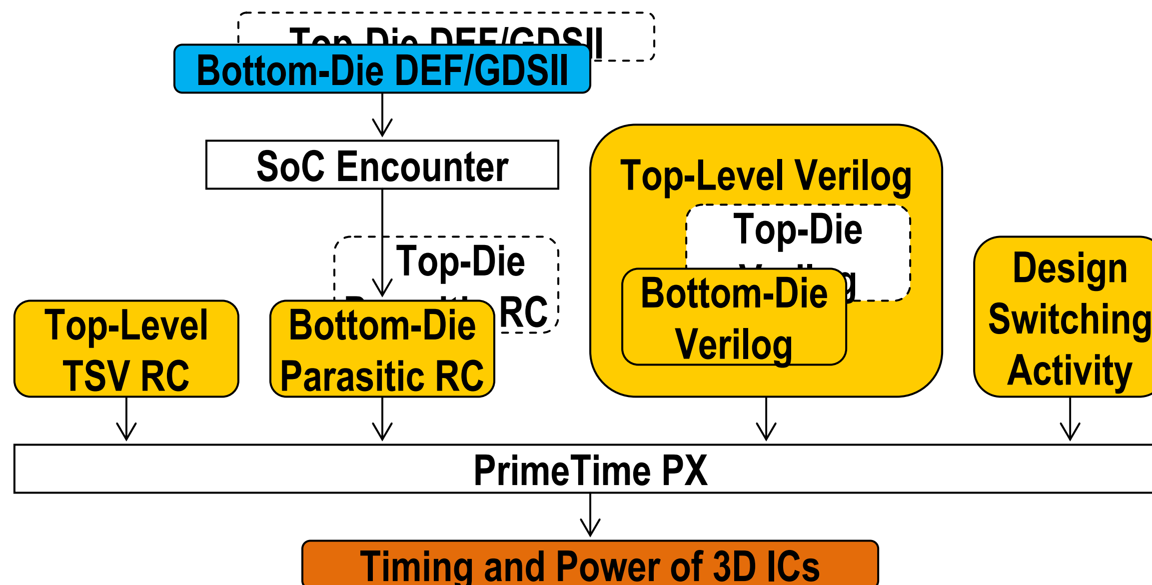
- **Study three different design styles of the bottom die**
  - **TSV-farm: dense array of TSVs in the middle of bottom die (no need for RDL)**
  - **TSV-distributed: arrays of TSVs distributed across bottom die**
  - **TSV-whitespace: TSVs inserted in whitespace nearby connecting pins**

Design Flow

- **Partitioning:**
  - Use same partition in all design styles for fair comparison
- **Floorplanning:**
  - Preplace TSVs (TSV-farm and TSV-distributed)
  - Postplace TSVs (TSV-whitespace)
- **Timing optimization:**
  - Set timing constraints of each die according to [Y.-J. Lee, 3DIC 2010]
  - Insert buffers to meet the constraints of each die separately
- **Routing**
  - Routing on each die
  - RDL routing (TSV-distributed and TSV-whitespace)

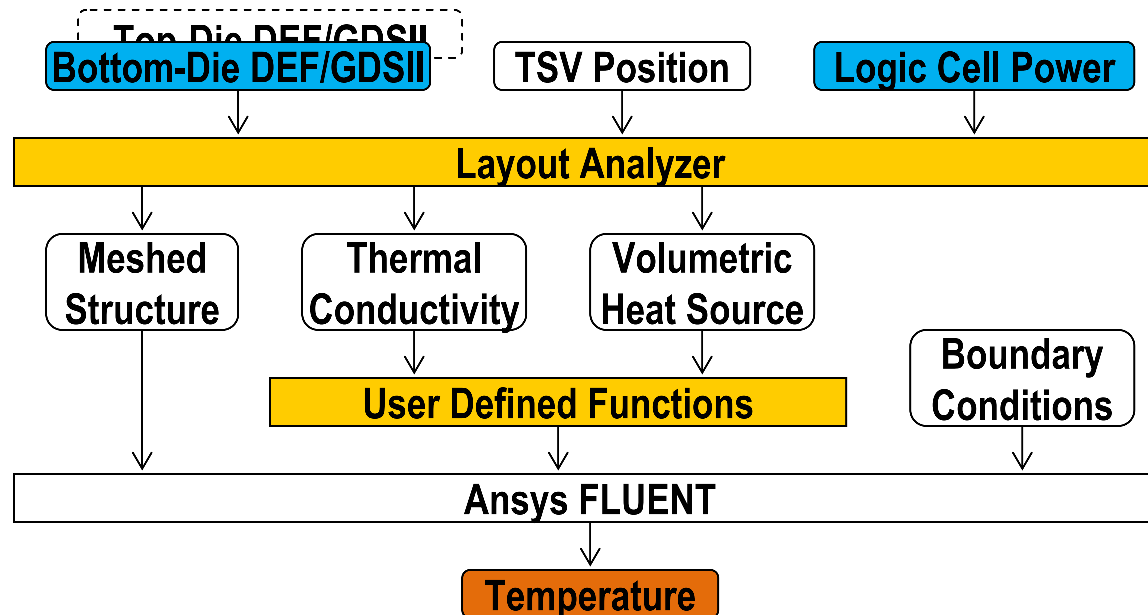
Evaluation – Traditional Metrics

- Area and wirelength are directly obtained from the layout of both bottom and top dies
- Delay and power are analyzed using the following flow:

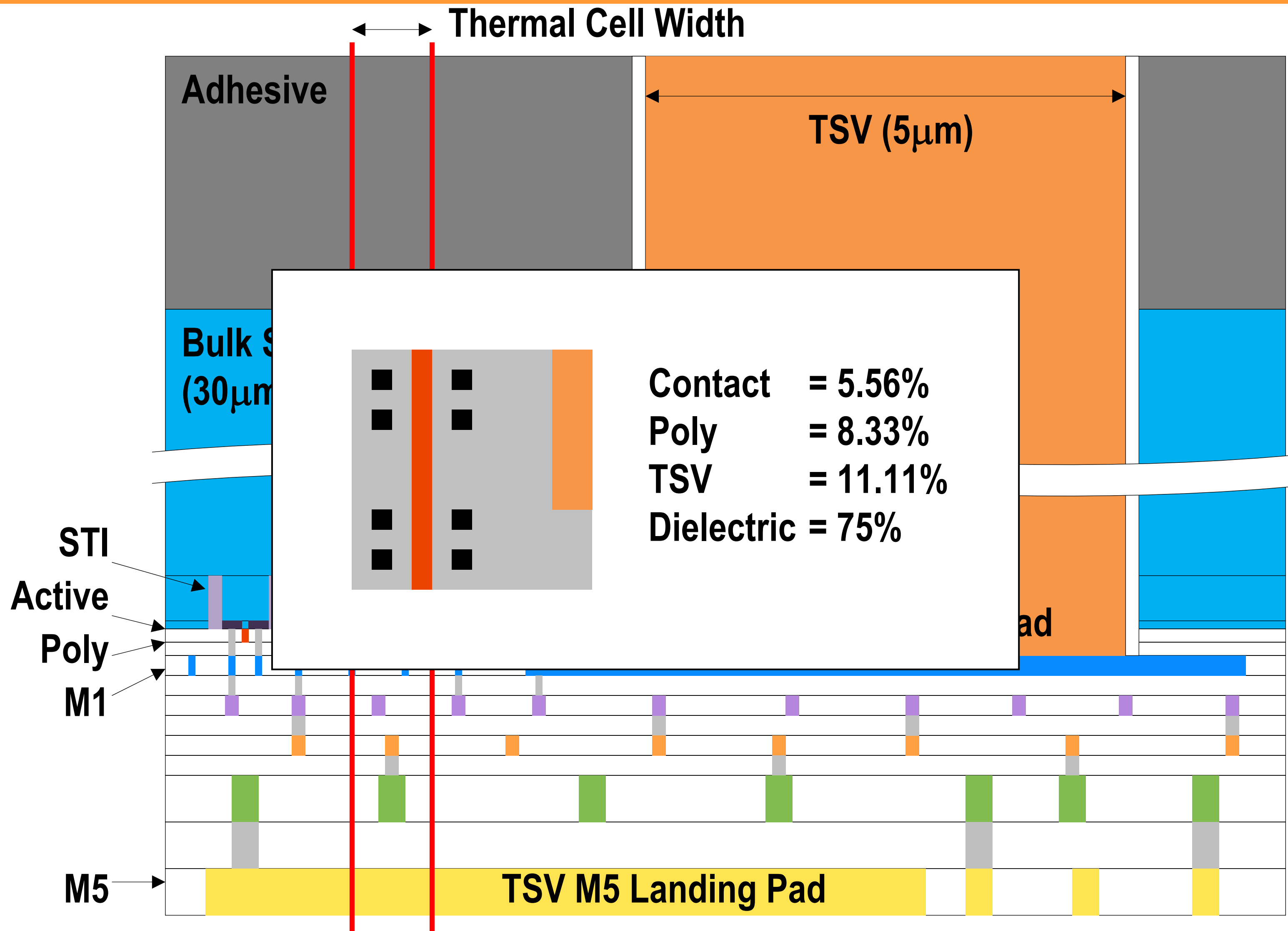


Evaluation – Reliability Metrics Temperature (I)

- **Temperature is analyzed using the following flow:**



Evaluation – Reliability Metrics Temperature (II)



Evaluation – Reliability Metrics Mechanical Stress [M. Jung, DAC 2011] (I)

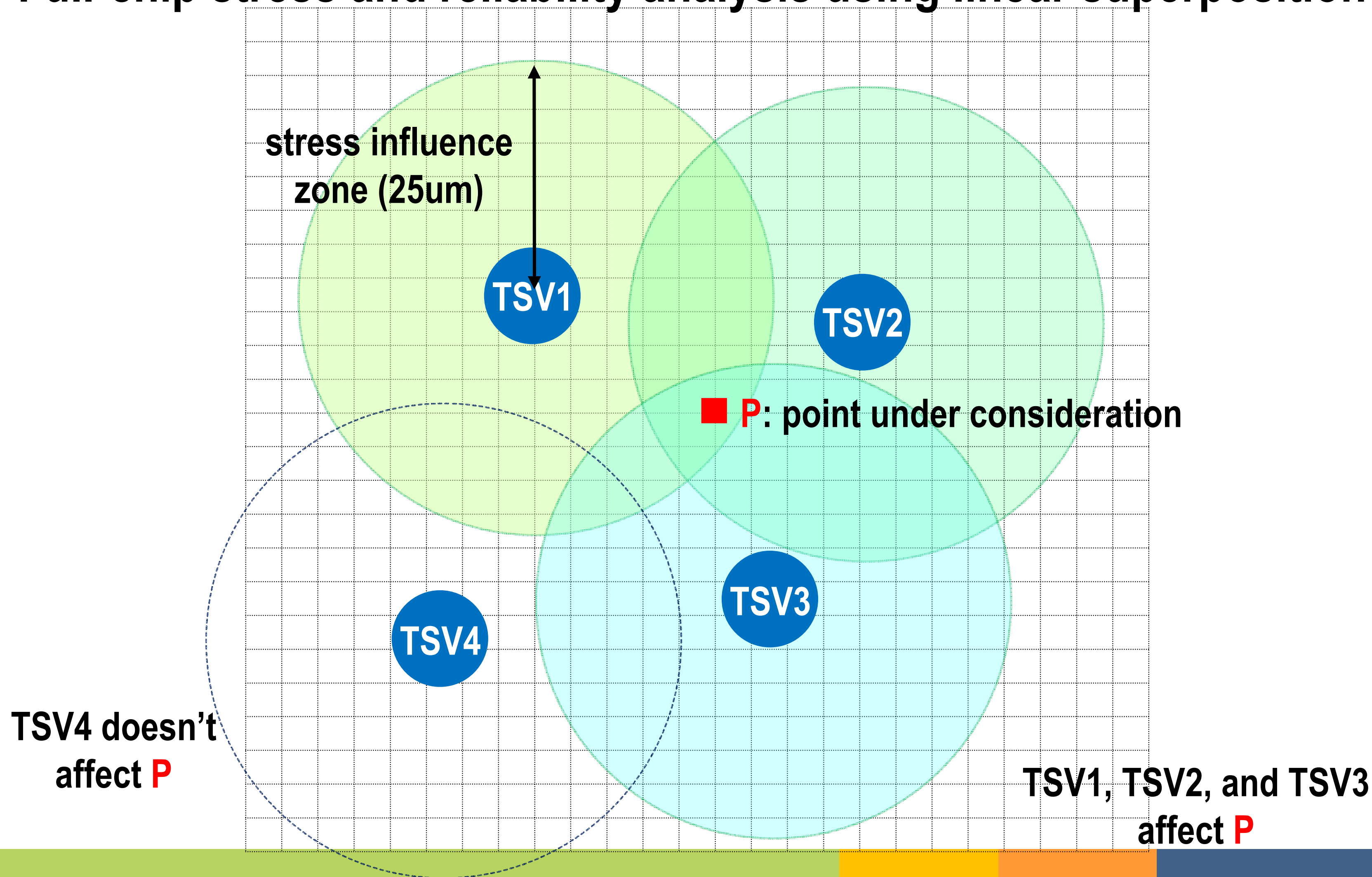
- **Baseline TSV stress model from FEA simulation**
  - **Model realistic TSV structures: TSV, liner, landing pad**
  - **Obtain stress tensor from simulation result**
  - **Convert to Cartesian coordinate**

$$S_{xyz} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\ \sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\ \sigma_{zr} & \sigma_{z\theta} & \sigma_{zz} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

Stress tensor from FEA simulation

Evaluation – Reliability Metrics Mechanical Stress [M. Jung, DAC 2011] (II)

- Full-chip stress and reliability analysis using linear superposition



The Test Circuit

- A reconfigurable computing array obtained from OpenCores

Total #gates	1,363,536
#Interblock nets	1,853
#TSVs	312
Total #blocks	95
#Blocks on top die	26
#Blocks on bottom die	69

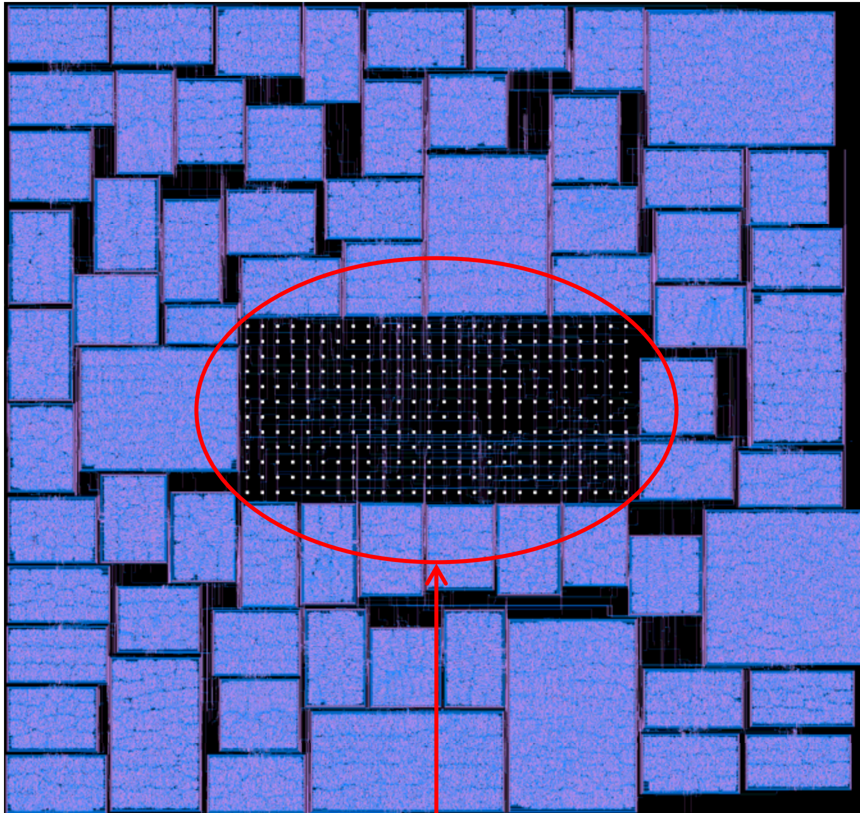
Experiments

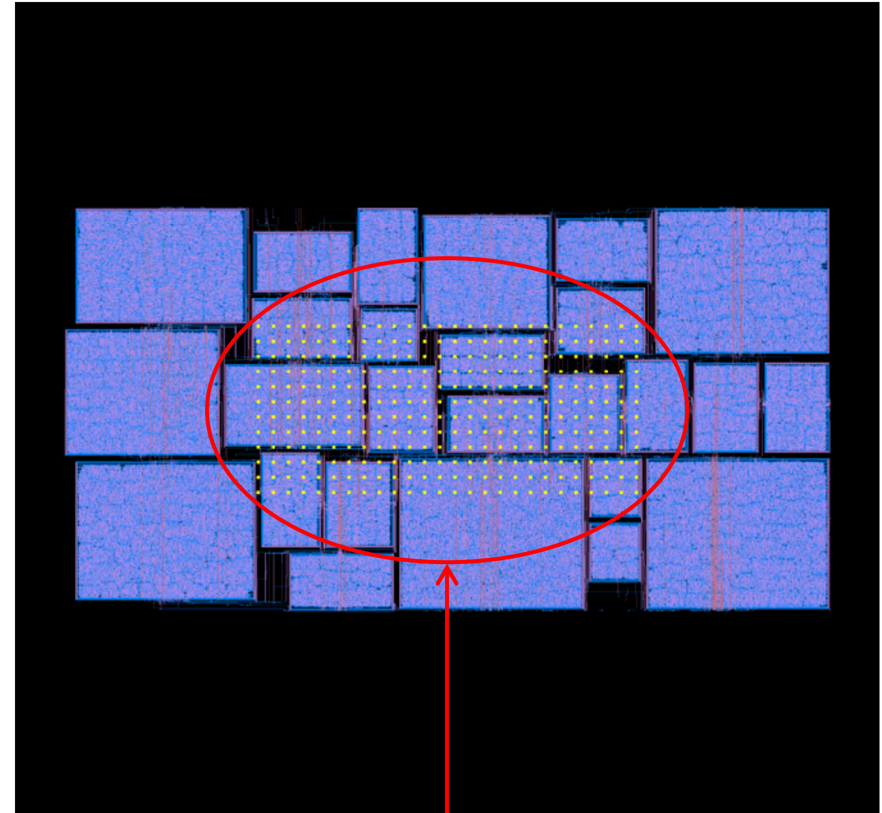
- **Baseline designs**
  - TSV size: 10 μm
  - TSV pitch: 30 μm

- **Small TSV (Small TSV size)**
  - TSV size: 5 μm
  - TSV pitch: 30 μm

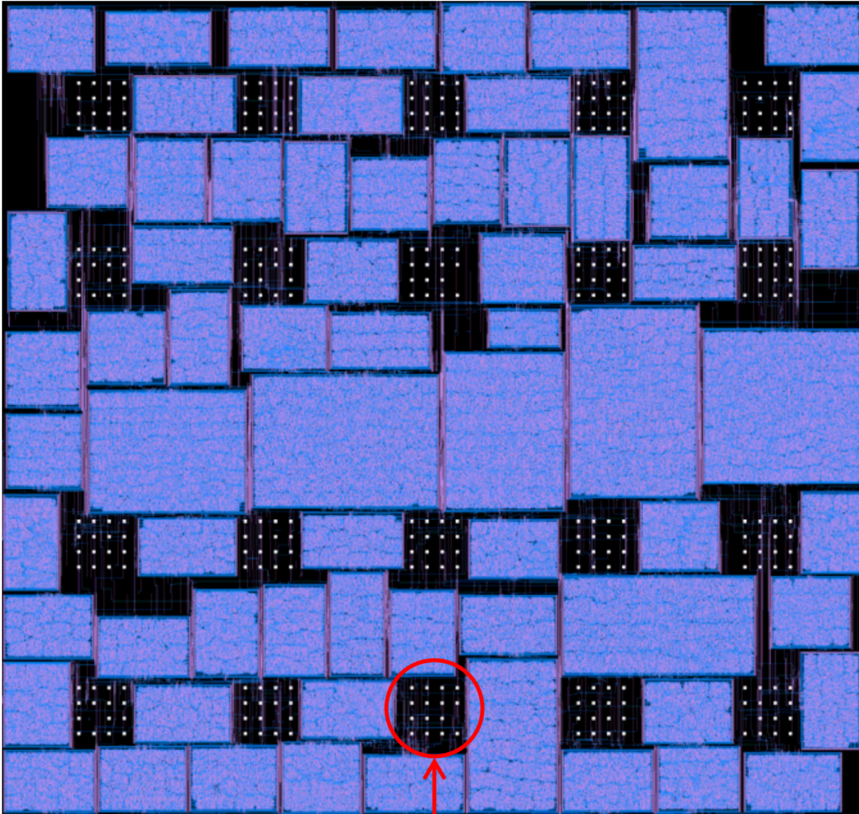
- **Dense TSV (Small TSV size + narrow TSV pitch)**
  - TSV size: 5 μm
  - TSV pitch: 15 μm

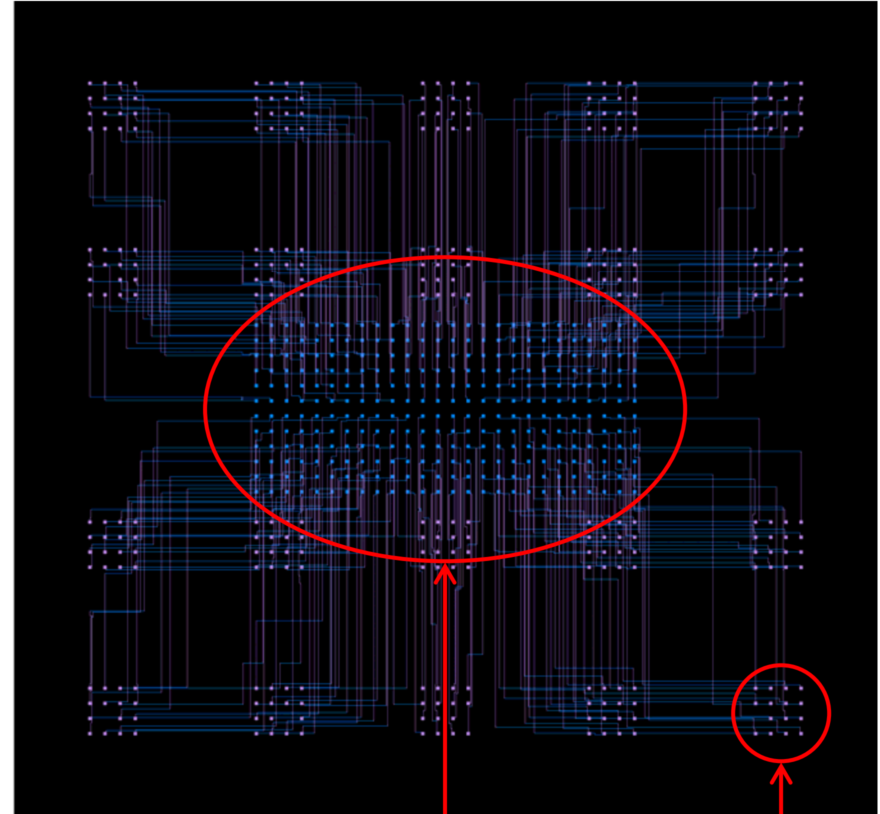
Baseline – Layout in TSV-farm Style





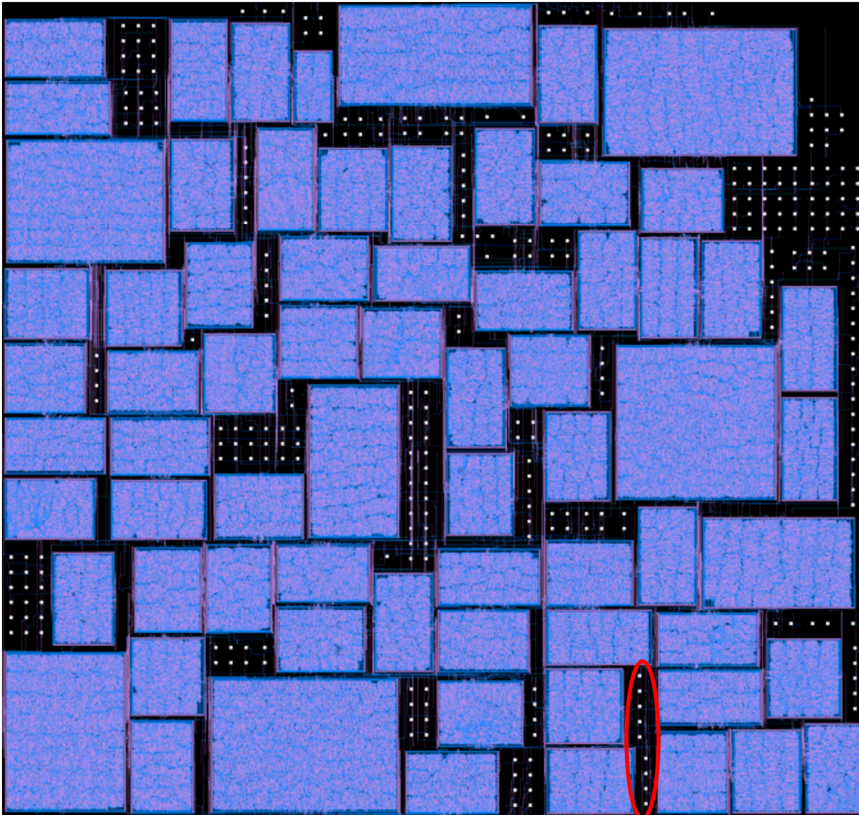
Baseline – Layout in TSV-distributed Style



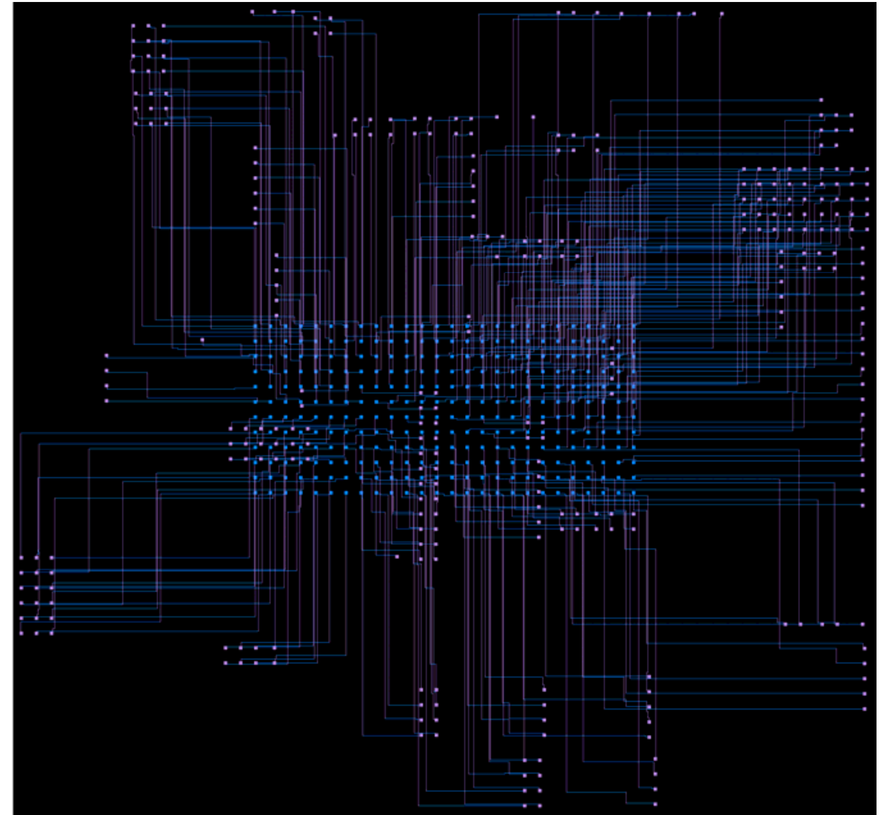


Baseline – Layout in TSV-whitespace Style

Bottom Die

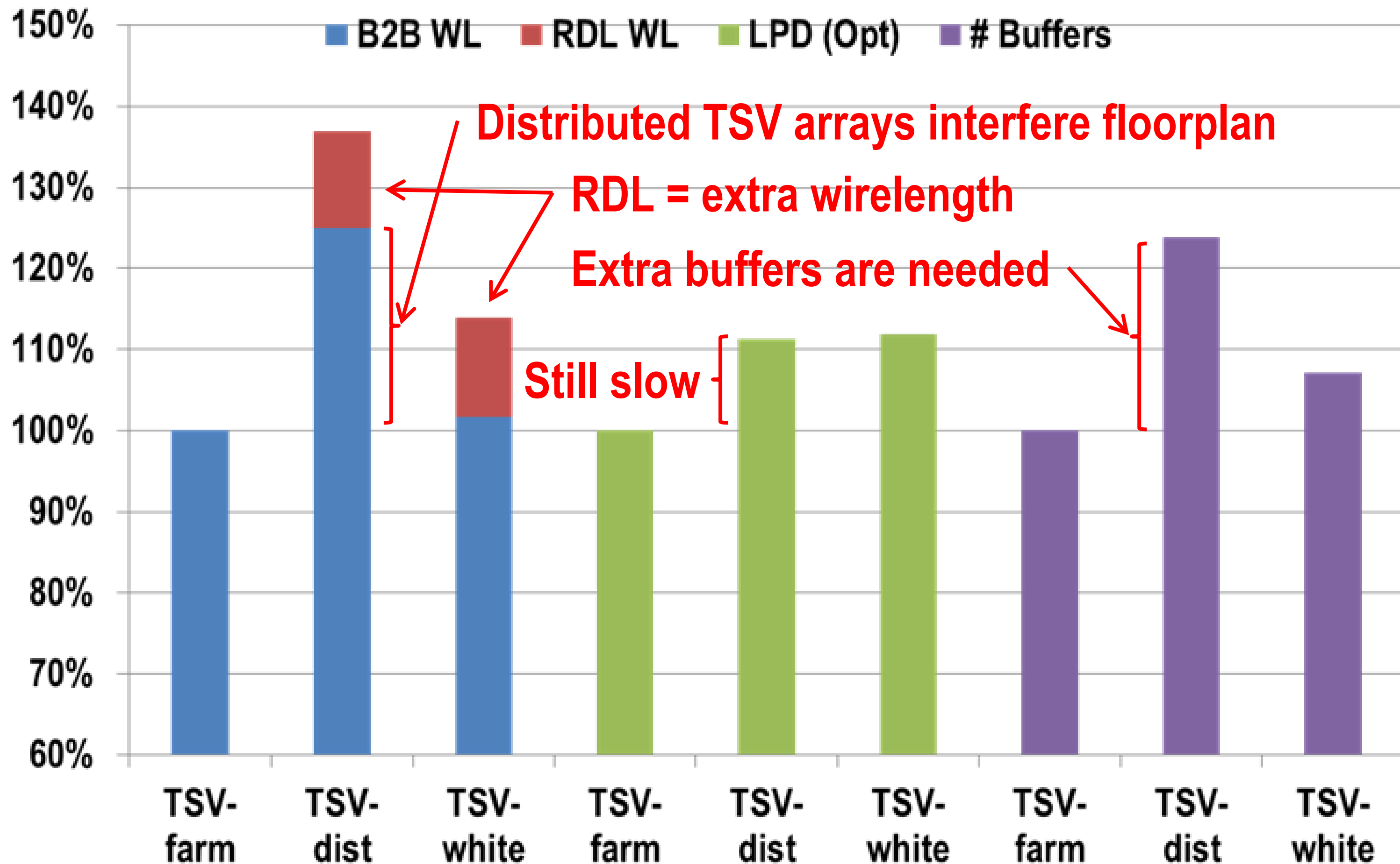


RDL

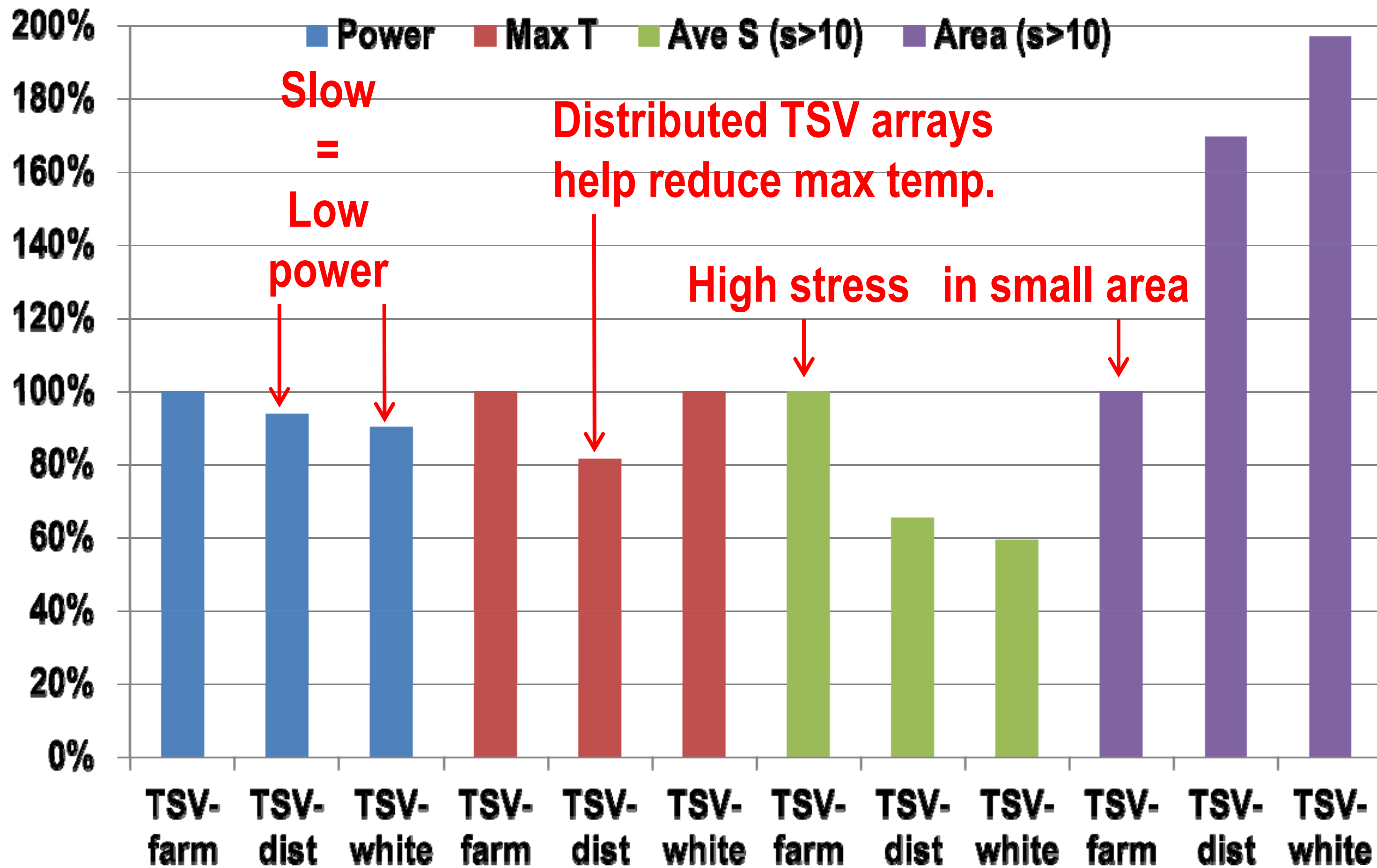


Most TSVs are in whitespace

Baseline – Wirelength, Delay, and Buffers

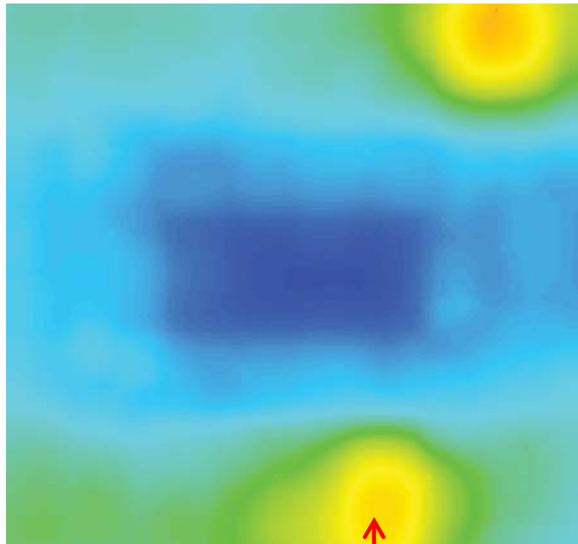


Baseline – Power, Temperature, and Stress



Baseline – Temperature Map of Bottom Die

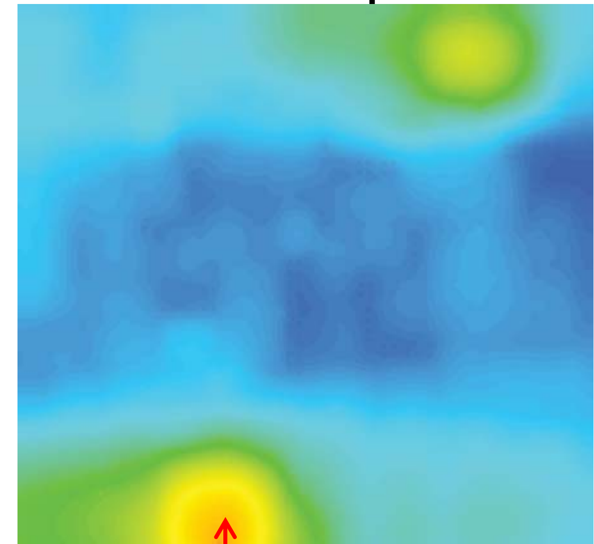
TSV-farm



Hot spot far from TSV farm

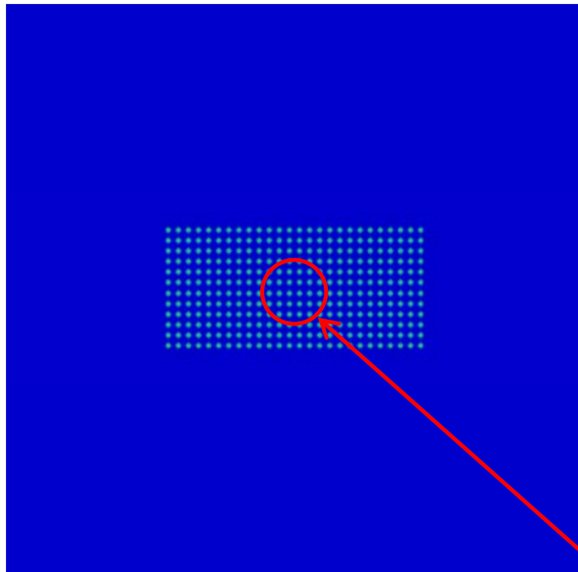
TSV-distributed

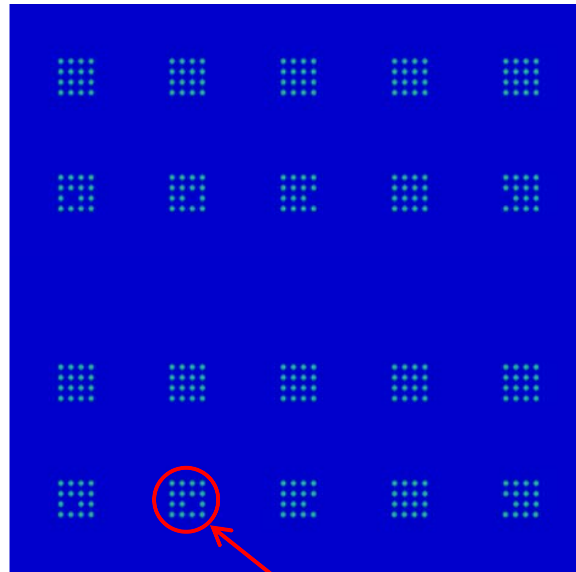
TSV-whitespace

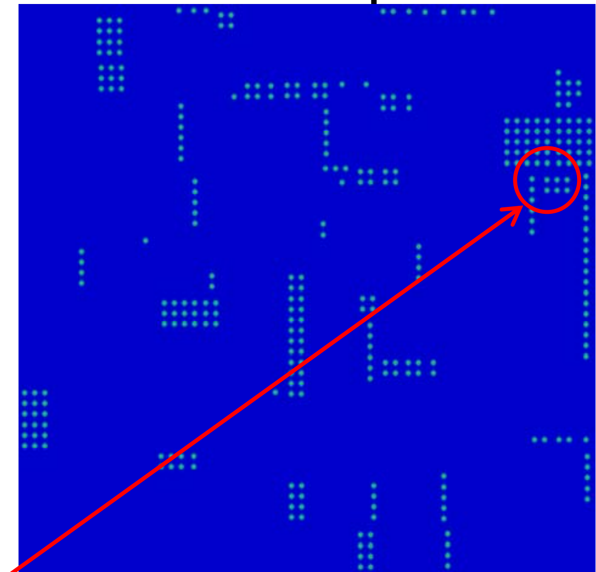


Only few TSVs nearby hot spot

Baseline – Stress Map of Bottom Die





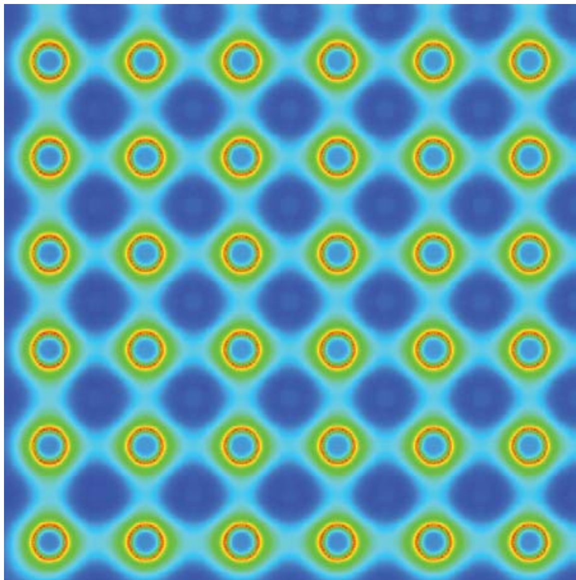


Zoom up these areas

TSV stress impacts area nearby the TSV

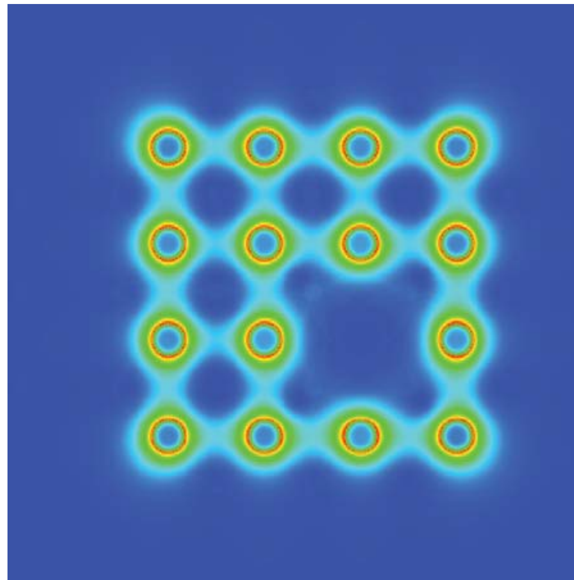
Baseline – Stress Map of Bottom Die (Zoom-up)

TSV-farm

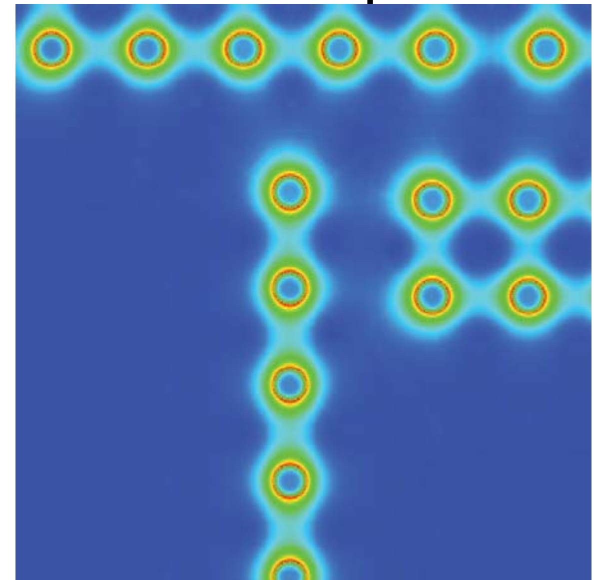


Stress from nearby TSVs adds up

TSV-distributed

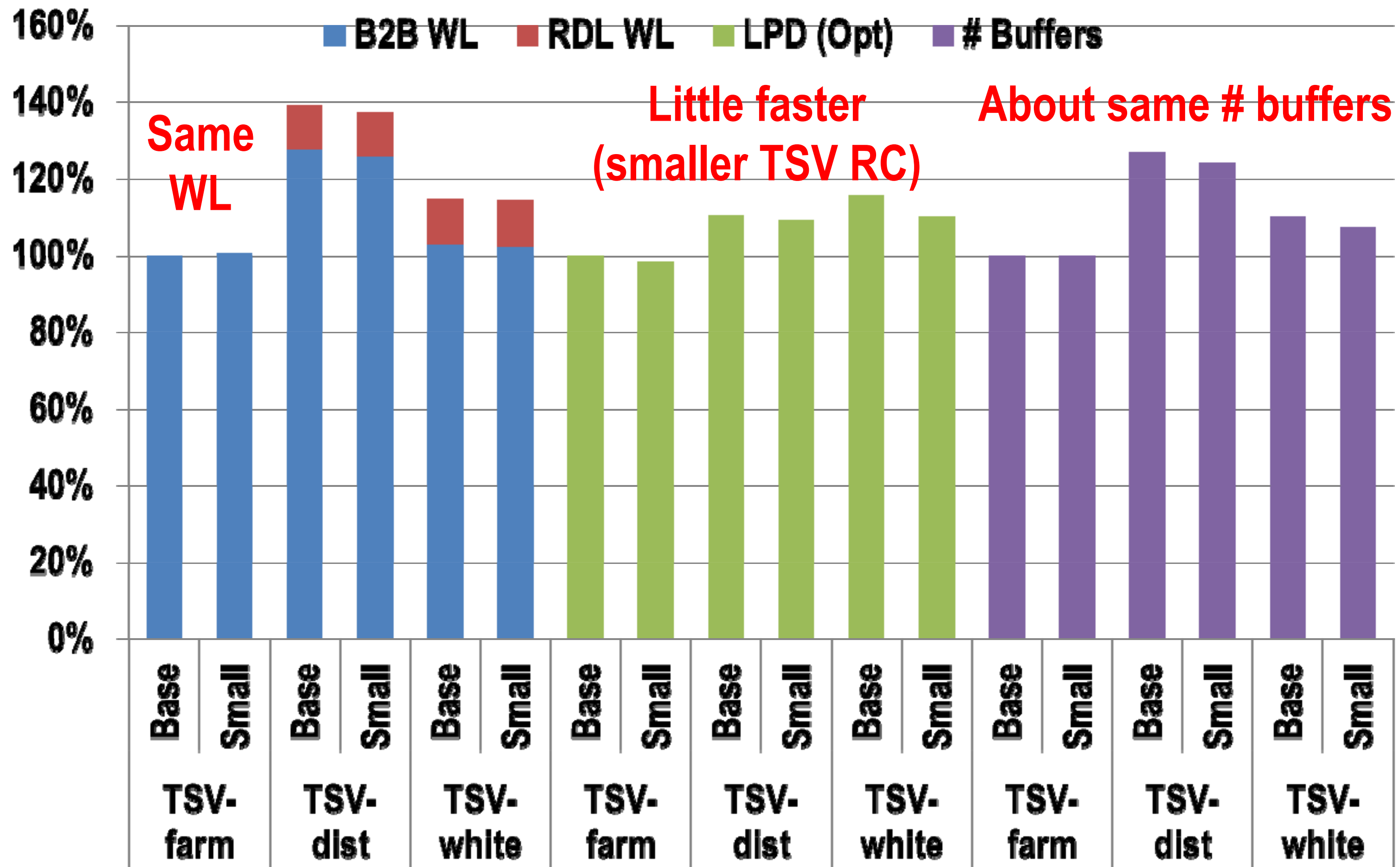


TSV-whitespace

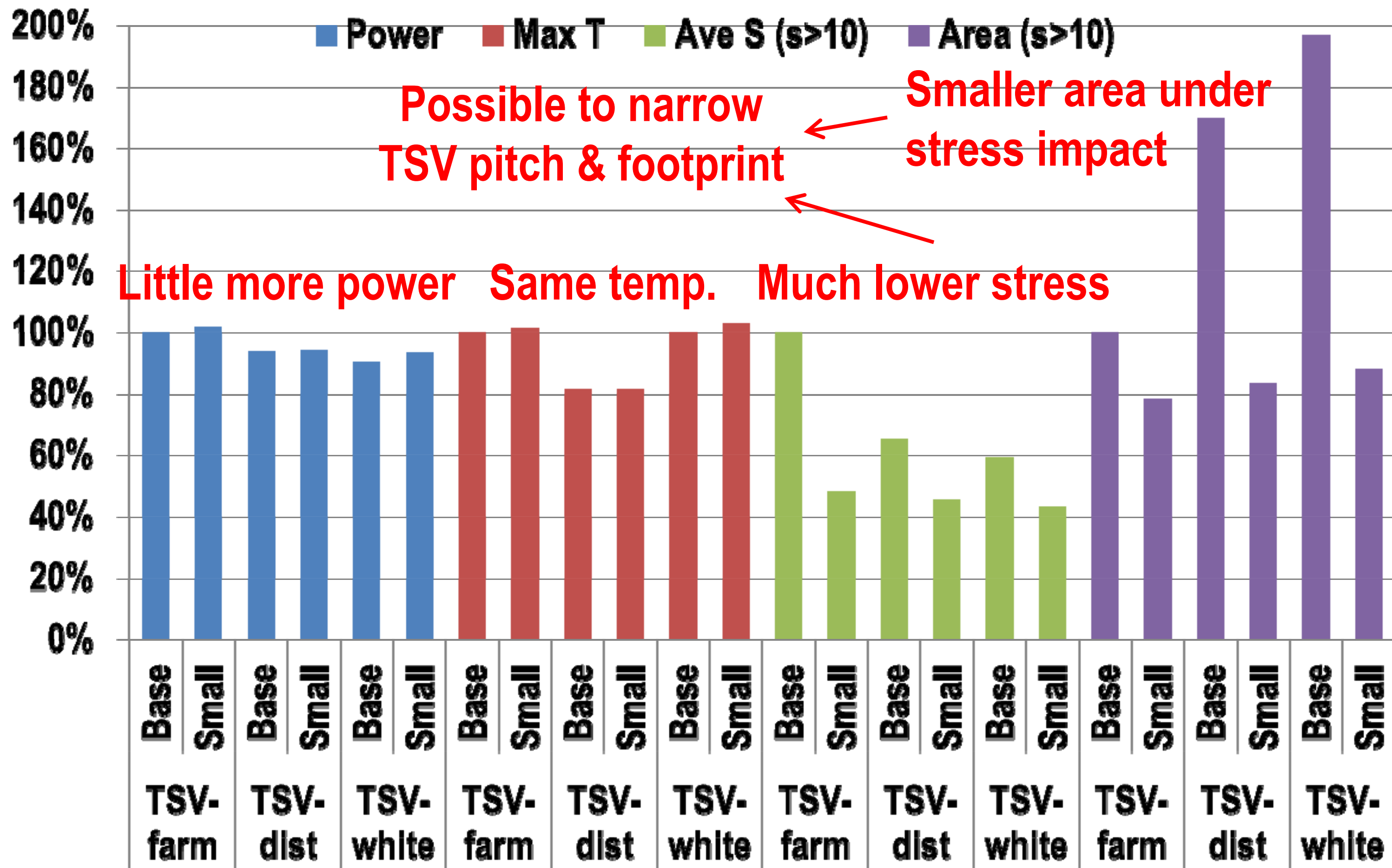


Areas impacted by TSV stress do not overlap much

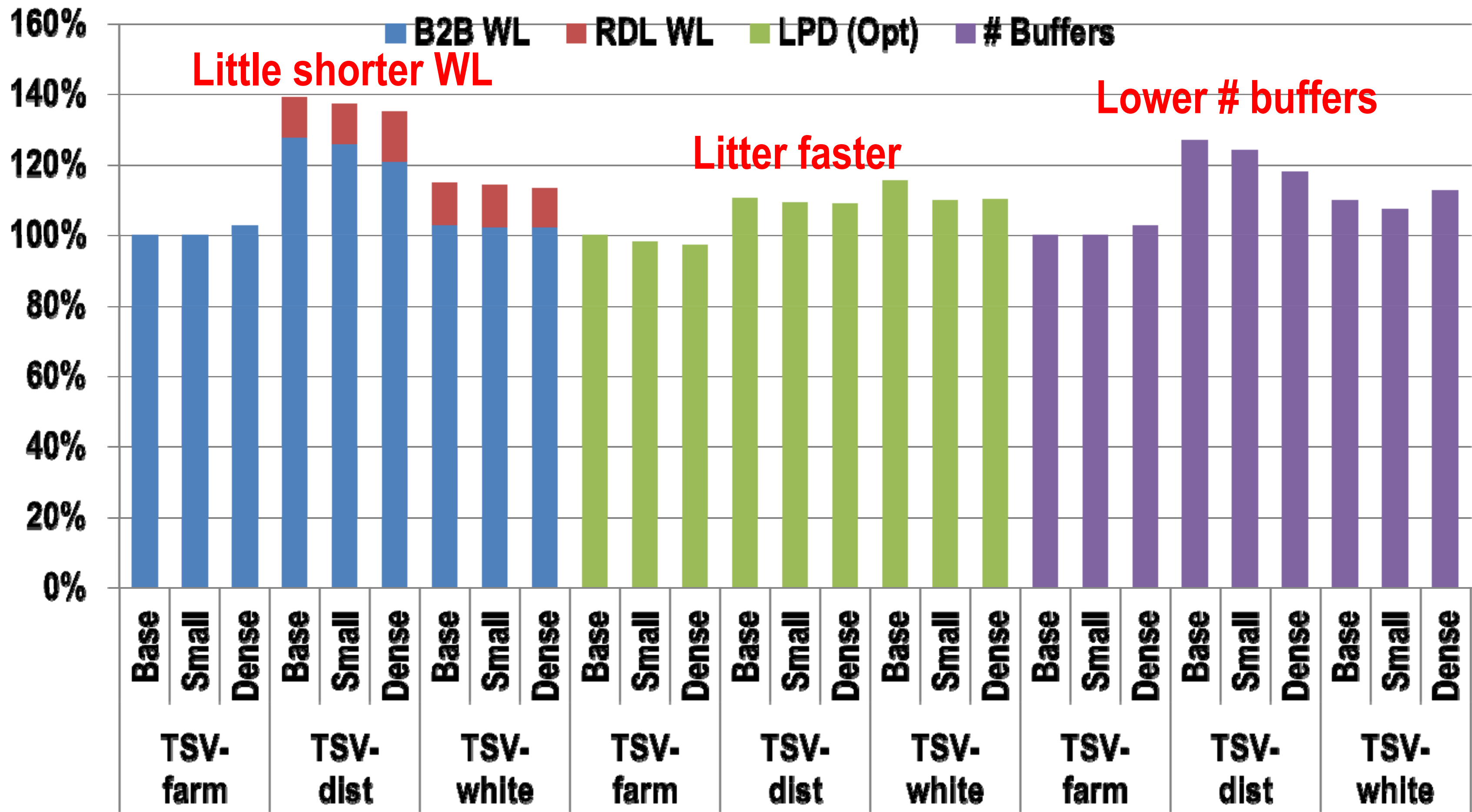
Small TSV – Wirelength, Delay, and Buffers



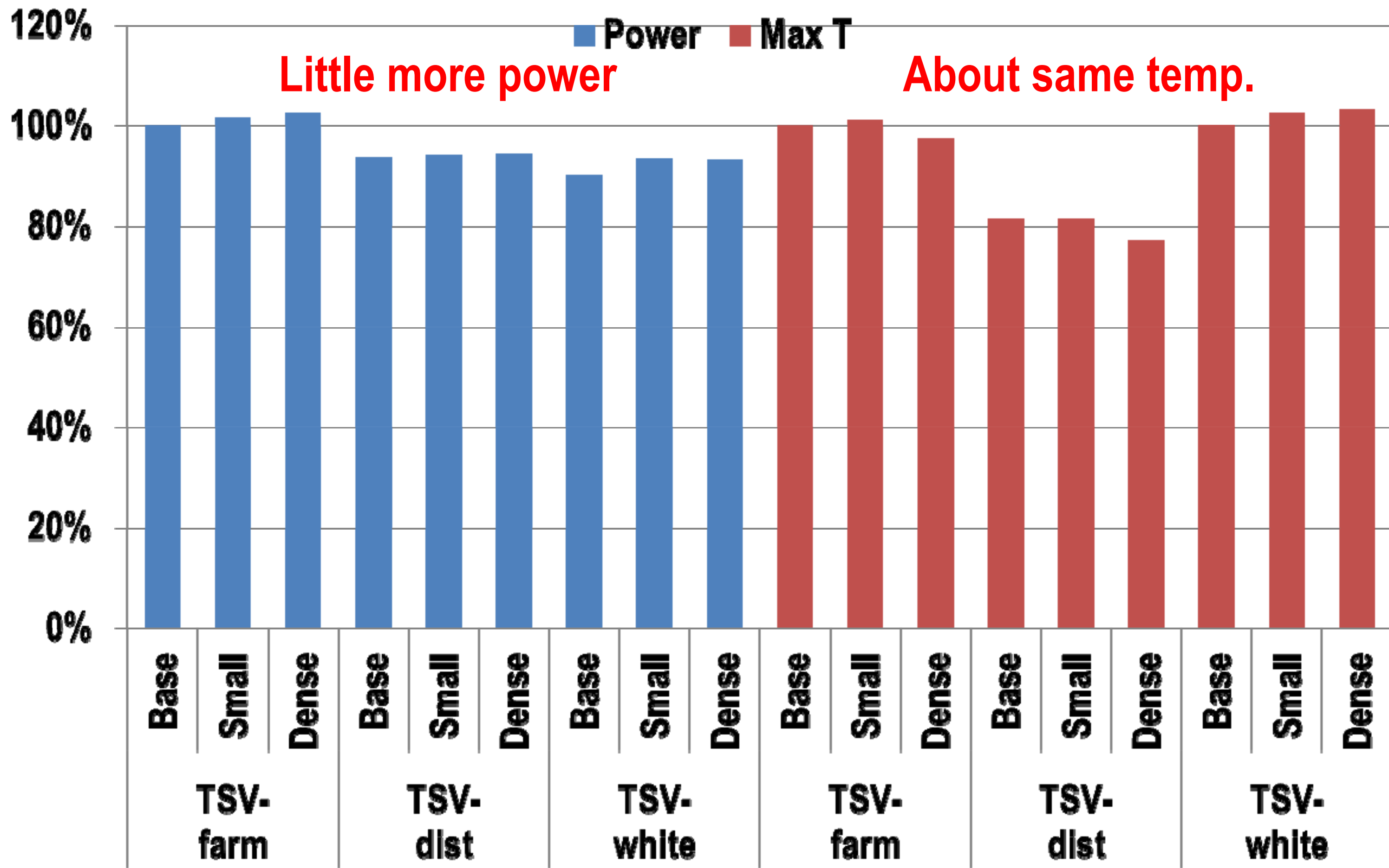
Small TSV – Power, Temperature, and Stress



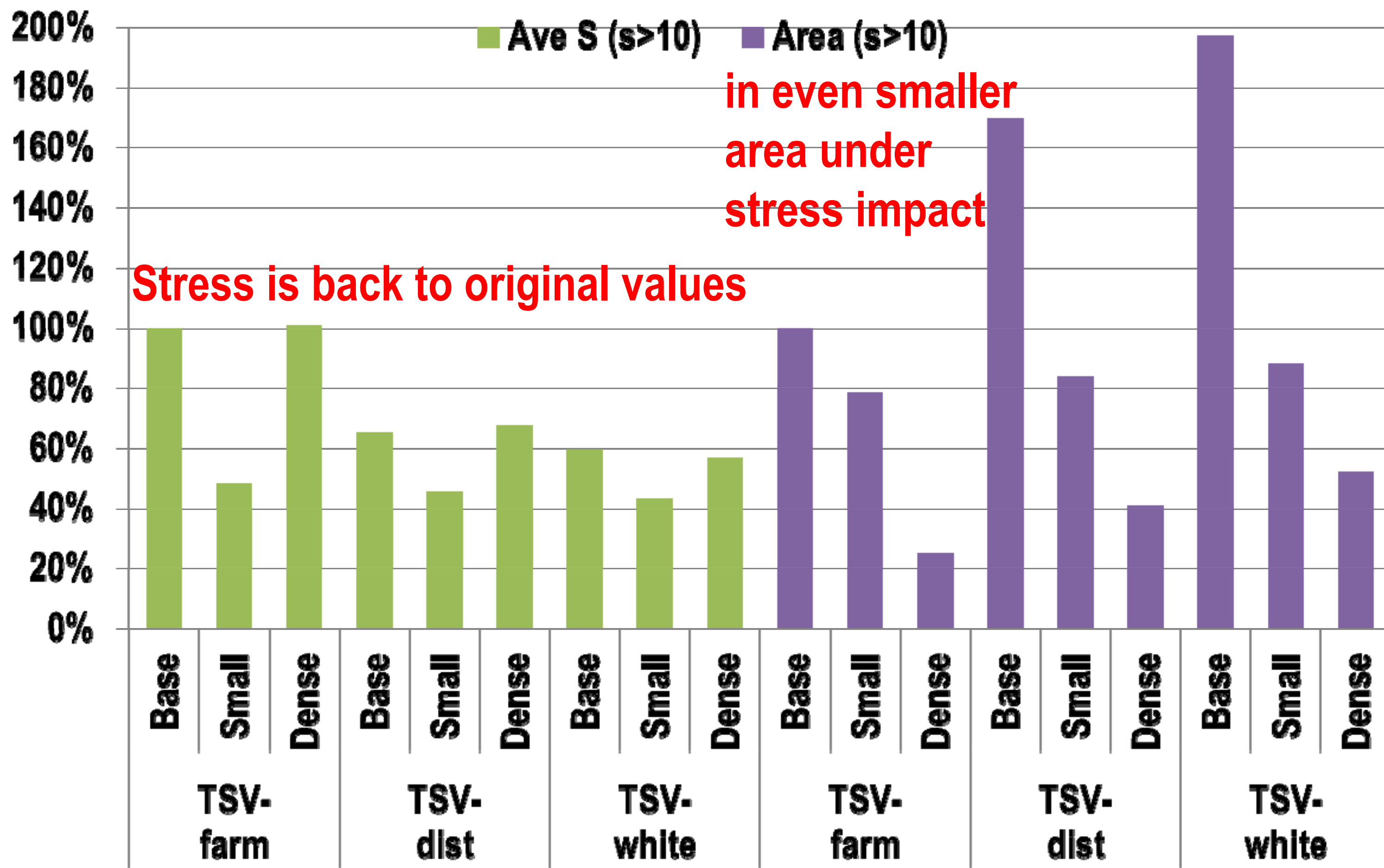
Dense TSV – Wirelength, Delay, and Buffers



Dense TSV – Power and Temperature



Dense TSV – Stress



Conclusions

- A circuit is manually designed in three different styles to study trade-offs of the quality of the layouts
- TSV-farm style
  - Shortest wirelength and best timing
  - Highest average stress, but smallest impacted area
- TSV-distributed style
  - Longest wirelength (TSVs interfere placement)
  - Lowest temperature (TSVs help reduce temperature)

Thank you

Questions?