ASP-DAC 2014

19th Asia and South Pacific Design Automation Conference (ASP-DAC)

FINAL PROGRAM

Date: January 20-23, 2014
Place: Suntec, Singapore

Sponsored by

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CEDA® IEEE Council on Electronic Design Automation

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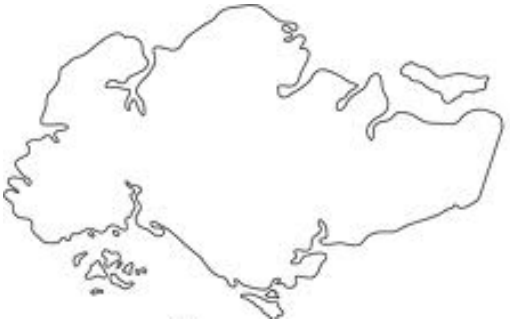


http://www.aspdac.com

ASP-DAC 2014

Contents

Highlights

Opening and Keynote I

Tuesday, January 21, 2014, 08:30 – 10:00

Ivo Bolsens (Senior VP & CTO, Xilinx, U.S.A.) "*All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure*"

Keynote II

Wednesday, January 22, 2014, 08:30 – 09:30

Georges Gielen (Katholieke Univ. Leuven, Belgium) "*Designing Analog Functions without Analog Transistors*"

Keynote III

Thursday, January 23, 2014, 08:30 – 09:30

Kaushik Roy (Purdue Univ., U.S.A.) "*Beyond Charge-Based Computing"*

Banquet Keynote

Wednesday, January 22, 2014, 18:30 – 21:00

Ulf Schneider (Managing Director, Lantiq Asia Pacific Pte/President, SSIA, Singapore) "*The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies*"

Special Sessions

1A: (Presentation + Poster Discussion) University Design Contest

Tuesday, January 21, 2014, 10:40 – 12:20

1S: (Invited Talks) Normally-Off Computing: Towards Zero Stand-by Power Management

Tuesday, January 21, 2014, 10:40 – 12:20

2S: (Invited Talks) EDA for Energy

Tuesday, January 21, 2014, 13:50 – 15:30

3S: (Invited Talks) Neuron Inspired Computing using Nanotechnology

Tuesday, January 21, 2014, 15:50 – 17:30

4S: (Invited Talks) Design Automation Methods for Highly-Complex Multimedia Systems

Wednesday, January 22, 2014, 10:10 – 12:15

5S: (Invited Talks) Billion Chips of Trillion Transistors

Wednesday, January 22, 2014, 13:50 – 15:30

6S: (Invited Talks) Overcoming Major Silicon Bottlenecks: Variability, Reliability, Validation, and Debug

Wednesday, January 22, 2014, 15:50 – 17:30

7S: (Invited Talks) Brain Like Computing: Modelling, Technology, and Architecture

Thursday, January 23, 2014, 10:10 – 12:15

8S: (Invited Talks) Design Flow for Integrated Circuits using Magnetic Tunnel Junction Switched by Spin Orbit Torque

Thursday, January 23, 2014, 13:50 – 15:30

9S: (Invited Talks) The Role of Photons in Harming or Increasing Security

Thursday, January 23, 2014, 15:50 – 17:30

Tutorials

ASP-DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and one in the afternoon. For each session, four options are available – two in the physical-design (PD) domain and two in the system-design (SD) domain.

Tutorial-PD1: Energy-Efficient Datacenters

Monday, January 20, 2014, 09:00 – 12:00

Organizer:

Massoud Pedram (Univ. of Southern California, U.S.A.)

Speaker:

Massoud Pedram (Univ. of Southern California, U.S.A.)

Tutorial-PD2: Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyber-Physical System Integration

Monday, January 20, 2014, 14:00 – 17:00

Organizer:

Tsung-Yi Ho (National Cheng Kung Univ, Taiwan)

Speakers:

Tsung-Yi Ho (National Cheng Kung Univ, Taiwan)

Krishnendu Chakrabarty (Duke Univ., U.S.A.)

Tutorial-PD3: On Variability and Reliability; Dynamic Margining and Low Power"

Monday, January 20, 2014, 9:00 – 12:00

Organizer:

Fadi Kurdahi (Univ. of California, Irvine, U.S.A.)

Speakers:

Fadi Kurdahi (Univ. of California, Irvine, U.S.A.)

Greg Taylor (Intel Research Lab, U.S.A.)

Ahmed Eltawil (Univ. of California, Irvine, U.S.A.)

Amin Khajeh (Intel Research Lab, U.S.A.)

Tutorial-PD4: Architecture Level Thermal Modeling, Prediction and Management for Multi-Core and 3D Microprocessors

Monday, January 20, 2014, 14:00 – 17:00

Organizer:

Sheldon Tan (Univ. of California, Riverside, U.S.A.)

Speakers:

Sheldon Tan (Univ. of California, Riverside, U.S.A.)

Hai Wang (Univ. of Electronic Science & Technology, China)

Tutorial-SD1: High-Level Specifications to Cope with Design Complexity

Monday, January 20, 2014, 14:00 – 17:00

Organizer:

Gunar Schirner (Northeastern Univ., U.S.A.)

Speakers:

Gunar Schirner (Northeastern Univ., U.S.A.)

Wolfgang Müller (Univ. of Paderborn, Germany)

Eugenio Villar (Univ. of Cantabria, Spain)

Rainer Dömer (Univ. of California, Irvine, U.S.A.)

Tutorial-SD2: Many-core and Heterogeneous System-Level Verification Methodology

Monday, January 20, 2014, 09:00 – 12:00

Organizer:

Alex Goryachev (IBM Research - Haifa, Israel)

Speakers:

Alex Goryachev (IBM Research - Haifa, Israel)

Ronny Morad (IBM Research - Haifa, Israel)

Tutorial-SD3: The Formal Specification Level: Bridging the Gap between the Spec and its Implementation

Monday, January 20, 2014, 14:00 – 17:00

Organizer:

Robert Wille (Univ. of Bremen, Germany)

Speakers:

Robert Wille (Univ. of Bremen, Germany)

Rainer Findenig (Intel Mobile Communications, Austria)

Rolf Drechsler (DFKI GmbH, Germany)

Tutorial-SD4: High-Level Synthesis for Low-Power Design

Monday, January 20, 2014, 09:00 – 12:00

Organizer:

Deming Chen (Univ. of Illinois, U.S.A.)

Speakers:

Zhiru Zhang (Cornell Univ., U.S.A.)

Deming Chen (Univ. of Illinois, U.S.A.)

Social Events:

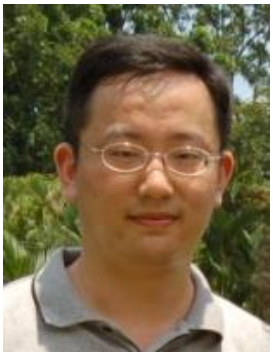
Welcome Reception

Monday, January 20, 2014, 18:00 – 20:00 @ Suntec (Room 309 and Room 310)

Conference Banquet

Wednesday, January 22, 2014, 18:30 – 21:00 @ Flower Field Hall, Gardens by the Bay

Welcome to ASP-DAC 2014



On behalf of the ASP-DAC 2014 Organizing Committee, we would like to invite all colleagues from academia and industry working on the LSI design and design automation areas to the 19th Asia and South Pacific Design Automation Conference (ASP-DAC 2014). ASP-DAC 2014 will be held from 20th January (Monday) to 23rd January (Thursday), 2014 at Suntec City Singapore.

Even for frequent visitors to Singapore, this island city country is keeping on transforming its landscape and attracting visitors with new wonders. The conference site is Suntec City, which is designed to be a 'city within a city'. It is the single largest integrated commercial development in Singapore with an international convention and exhibition centre, a shopping mall, five office towers, and a fountain all connected to each other by street level plazas, walkways and courtyards. The conference banquet will be in the nearby Flower Field Hall of Gardens by The Bay, a newly developed oasis where over 250,000 rare plants greet you in full bloom. We believe you will enjoy your stay in Singapore, a truly world-class modern city in Southeast Asia with over 5 million people and diverse culture like no other.

ASP-DAC 2014 attracted 343 submissions from 29 countries from our worldwide colleagues in academic, industry and government institutions. Under the leadership of Technical Program Co-Chairs, Nagisa Ishiura, Naehyuck Chang, and Tulika Mitra, the Technical Program Committee members conducted rigorous and thorough reviews and a full-day face-to-face meeting to select excellent papers for the technical program of ASP-DAC 2014. 108 papers have been accepted for regular presentation that cover key topics from system design to physical design. 9 Special Sessions have also been organized based on invited talks by the Technical Program Committee to discuss up-to-date topics.

We are happy to report that we have invited 4 distinguished keynote speakers from both academia and industry to discuss topics with programmable platform, analog, digital, and local focuses. The first keynote speaker Dr. Ivo Bolsens is Senior Vice President and CTO from Xilinx, USA. He will give a talk on how programmable platforms can contribute to big data applications. The second keynote speaker Prof. Georges Gielen is from Katholieke Universiteit Leuven, Belgium. He will give a talk on the building analog functions without analog transistors. The third Keynote speaker Prof. Kaushik Roy is from Purdue University. He will give a talk on the usage of spin instead of charge as state variable to achieve high density memory and ultra-low voltage/power logic. The fourth keynote speaker Mr. Ulf Schneider is Managing Director from Lantiq Asia Pacific. He is currently also serving as the President of Singapore Semiconductor Industry Association (SSIA). He will give us the stories of past, current and future Singapore Semiconductor industry.

Eight tutorials have been arranged on 20th January (Monday), 2014. This year, we have changed the tutorial style: instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and the other in the afternoon. For each session, four options are available – two in the physical-design (PD) domain and two in the system-design (SD) domain. In addition, as an important annual event of ASP-DAC, 10 designs were selected by the University Design Contest for presentation on 21st January (Tuesday), 2014.

ASP-DAC 2014 offers you an ideal opportunity to touch the recent technologies and the future directions on the LSI design and design automation areas. The success of ASP-DAC 2014 is indebted to the support of authors and the Organizing Committee members. Without authors' contributions, we would not have the opportunity to form the excellent technical program of ASP-DAC 2014. Every member of the Organizing Committee have devoted countless volunteering hours and days to ensure the success of conference.

Thank you very much for coming to Singapore for ASP-DAC 2014. We extend a warm welcome to all participants!

Yong Lian, Yajun Ha
General Co-Chairs, ASP-DAC 2014

Message from Technical Program Committee



On behalf of the Technical Program Committee of the Asia and South Pacific Design Automation Conference (ASP-DAC) 2014, we would like to welcome all of you to the conference scheduled from January 20 to 23, 2014 at Suntec City, Singapore.

This year, we received 343 submissions from 29 countries/regions, with the majority of them from Asia, North America, and Europe. Paper selection was really a challenge.

To support the selection process, we organized the Technical Program Committee consisting of 110 leading experts on EDA, IC design, and system design, who are from 15 countries/regions. The TPC was organized into 15 subcommittees. All committee members contributed to in-depth and thorough reviews, through a rigorous double-blind review process that involved vigorous discussions. Through a full day face-to-face discussion at the TPC Meeting held on September 2, 2013, at Kyoto Research Park in Japan, 108 high-quality papers were accepted, resulting in a very competitive acceptance rate of 31.5%.

Along with the selection of the regular papers, invitation of keynote speeches and special sessions were done. Then all the presentations were compiled into a three-day, four parallel-session program.

Each day, technical session starts with a keynote address. This year, we have also an extra keynote speech during the banquet. We have 9 special sessions on Track S (1S through 9S), which consists of invited talks on the state-of-the-art topics, including EDA and methodologies for ultra-large scale, ultra-low power, and high reliability design, emerging technologies and applications such as magnetoresistive memories, brain and neuron inspired computing, quantum devices, and EDA for energy. On the first day, we have a University LSI Design Contest session (1A). Regular papers are presented in 26 sessions on tracks A, B, and C.

Among the accepted regular papers, 13 were nominated for the Best Paper from each subcommittee. These Best Paper candidates went through a thorough evaluation process by the Best Paper Award Committee composed of 15 TPC members, and finally one of the candidate papers was selected for the ASP-DAC 2014 Best Paper Award.

The Technical Program of ASP-DAC 2014 is the fruit of the hard work of many people. We would like to thank all the people who have contributed to the technical program. In particular, we thank all the authors who submitted excellent papers that continue to make ASP-DAC a very vibrant conference and a premier forum for exchanging ideas and results. We would also like to thank TPC Secretaries and TPC members for their hard work. Finally, we also would like to thank the members of the Organizing Committee for their excellent services.

We hope that you will enjoy the ASP-DAC 2014 technical program.

Nagisa Ishiura
TPC Chair, ASP-DAC 2014

Naehyuck Chang
TPC Vice Chair, ASP-DAC 2014

Tulika Mitra
TPC Vice Chair, ASP-DAC 2014

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IT Secretariat	**Joseph Lim** (ELITE, Singapore)

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Secretary

Hyung Gyu Lee (Daegu Univ., Republic of Korea)
Yasuhiro Takashima (Univ. of Kitakyushu, Japan)
Shigeru Yamashita (Ristumeikan Univ., Japan)

Subcommittee Chairs and Subcommittees (*: Subcommittee Chairs)

[01] System-Level Modeling and Simulation/Verification

* **Derek Chiou** (Univ. of Texas at Austin, U.S.A.)
Shih-Hao Hung (National Taiwan Univ., Taiwan)
Makoto Sugihara (Kyushu Univ., Japan)
Yosinori Watanabe (Cadence Design Systems, U.S.A.)
Dongrui Fan (Chinese Academy of Sciences, China)
Atushi Ike (Fujitsu Laboratories, Japan)
Lei Wang (Univ. of Connecticut, U.S.A.)

[02] System-Level Synthesis and Optimization

*** Yun (Eric) Liang** (Peking Univ., China)
Paolo Ienne (EPFL, Switzerland)
Farhad Mehdipour (Kyushu Univ., Japan)
Sri Parameswaran (Univ. of New South Wales, Australia)
Unmesh Bordoloi (Linkoping Univ., Sweden)
Sungchan Kim (Chonbuk National Univ., Republic of Korea)
Alexandros Papakonstantinou (Nvidia, U.S.A.)
Jiang Xu (Hong Kong Univ. of Science and Technology, Hong Kong)

[03] System-Level Memory/Communication Design and Networks on Chip

*** TingTing Hwang** (National Tsing-Hua Univ., Taiwan)
Li-Pin Chang (National Chiao Tung Univ., Taiwan)
Yinhe Han (Chinese Academy of Sciences, China)
Chung-Ta King (National Tsing Hua Univ., Taiwan)
Jin Ouyang (Nvidia, U.S.A.)
Hiroyuki Tomiyama (Ritsumeikan Univ., Japan)
Paul Bogdan (Univ. of Southern California, U.S.A.)
Masoud Daneshtalab (Univ. of Turku, Finland)
Koji Inoue (Kyushu Univ., Japan)
Hsien-Hsin Lee (Georgia Institute of Technology, U.S.A.)
Muhammad Shafique (Karlsruhe Institute of Technology, Germany)

[04] Embedded and Real-Time Systems

*** Jian-Jia Chen** (Karlsruhe Institute of Technology, Germany)
Sudipta Chattopadhyay (National Univ. of Singapore, Singapore)
Song Han (Univ. of Connecticut, U.S.A.)
Kyungsoo Lee (Kyoto Univ., Japan)
Hyunok Oh (Hanyang Univ., Republic of Korea)
Jason Xue (City Univ. of Hong Kong, Hong Kong)
Philip Brisk (Univ. of California, Riverside, U.S.A.)
Nan Guan (Northeastern Univ., China)
Shinpei Kato (Nagoya Univ., Japan)
Hiroki Matsutani (Keio Univ., Japan)
Sebastian Steinhorst (TUM CREATE, Singapore)

[05] High-Level/Behavioral/Logic Synthesis and Optimization

*** Robert Wille** (Univ. of Bremen, Germany)
Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)
Kiyoung Choi (Seoul National Univ., Republic of Korea)
Yuko Hara-Azumi (Nara Institute of Science and Technology, Japan)
Christian Haubelt (Univ. of Rostock, Germany)
Yusuke Matsunaga (Kyushu Univ., Japan)
Zhiru Zhang (Cornell Univ., U.S.A.)

[06] Validation and Verification for Behavioral/Logic Design

*** Miroslav Velev** (Aries Design Automation, U.S.A.)
Charles H.-P. Wen (National Chiao Tung Univ., Taiwan)
Kiyoharu Hamaguchi (Shimane Univ., Japan)
Tsuyoshi Iwagaki (Hiroshima City Univ., Japan)

[7a] Physical Design (Placement)

*** Ting-Chi Wang** (National Tsing Hua Univ., Taiwan)
Hung-Ming Chen (National Chiao Tung Univ., Taiwan)
Guojie Luo (Peking Univ., China)
Shigetoshi Nakatake (Univ. of Kitakyushu, Japan)
Jia Wang (Illinois Institute of Technology, U.S.A.)

[7b] Physical Design (Routing)

*** Evangeline Young** (Chinese Univ. of Hong Kong, Hong Kong)
Mark Po-Hung Lin (National Chung Cheng Univ., Taiwan)
Wen-Hao Liu (National Tsing Hua Univ., Taiwan)
Gi-Joon Nam (IBM Research, U.S.A.)
Toshiyuki Shibuya (Fujitsu Laboratories, Japan)

[08] Timing, Power, Thermal Analysis and Optimization

*** Masanori Hashimoto** (Osaka Univ., Japan)
Mango Chia-Tso Chao (National Chiao Tung Univ., Taiwan)
Lih-Yih Chiou (National Cheng Kung Univ., Taiwan)
Mineo Kaneko (Japan Advanced Intistute of Science and Technology, Japan)
Bing Li (Technical Univ. of Munich, Germany)
Takashi Sato (Kyoto Univ., Japan)
Yiyu Shi (Missouri Univ. of Science and Technology, U.S.A.)
Youngsoo Shin (Korea Advanced Institute of Science and Technology, Republic of Korea)

[09] Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation

*** Ram Achar** (Carleton Univ., Canada)
Luca Daniel (Massachusetts Institute of Technology, U.S.A.)
Dipanjan Gope (Indian Institute of Science, India)
Rung-Bin Lin (Yuan Ze Univ., Taiwan)
Fan Yang (Fudan Univ., China)
Wenjian Yu (Tsinghua Univ., China)

[10] Design for Manufacturability/Yield and Statistical Design

*** Xuan Zeng** (Fudan Univ., China)
Steven (Chien-Wen) Chen (TSMC, Taiwan)
Puneet Gupta (Univ. of California, Los Angeles, U.S.A.)
Shigeki Nojima (Toshiba Corporation, Japan)
Martin Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)
Jae-seok Yang (Samsung, Republic of Korea)
Hai Zhou (Northwestern Univ., U.S.A.)

[11] Test and Design for Testability

*** Tomokazu Yoneda** (NAIST, Japan)
Jiun-Lang Huang (National Taiwan Univ., Taiwan)
Kohei Miyase (Kyushu Institute of Technology, Japan)
Yu Hu (Chinese Academy of Sciences, China)
Yu Huang (Mentor Graphics, U.S.A.)
Dong Xiang (Tsinghua Univ., China)

[12] Analog, RF and Mixed Signal Design and CAD

*** Sheldon Tan** (Univ. of California, Riverside, U.S.A.)
Shi Guoyong (Shanghai Jiaotong Univ., China)
Hai Wang (Univ. of Electronic Science and Technology of China, China)
Hideki Asai (Shizuoka Univ., Japan)
Wong Ngai (Univ. of Hong Kong, Hong Kong)

[13a] EDA and Design Methodologies for Emerging Technologies

*** Hai (Helen) Li** (Univ. of Pittsburgh, U.S.A.)
Jae-Joon Kim (Pohang Univ. of Science and Technology, Republic of Korea)
Guangyu Sun (Peking Univ., China)
Danghui Wang (Northwestern Polytechnical Univ., China)
Ik-Joon Chang (Kyunghee Univ., Republic of Korea)
Yongpan Liu (Tsinghua Univ., China)
Yvain Thonnart (CEA-LETI, France)

[13b] Emerging Applications

*** Tsung-Yi Ho** (National Cheng Kung Univ., Taiwan)
Shanq-Jang Ruan (National Taiwan Univ. of Science and Technology, Taiwan)
Yu Wang (Tsinghua Univ., China)
Dajiang Zhou (Waseda Univ., Japan)
Jongsun Park (Korea Univ., Republic of Korea)
Yasushi Sugama (Fujitsu Laboratories, Japan)
Xiaoyang Zeng (Fudan Univ., China)

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Tony Kim (Nanyang Technological Univ., Singapore)
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University LSI Design Contest

The University LSI Design Contest has been conceived as a unique program at ASP-DAC. The purpose of the contest is to encourage research in LSI design at universities and its realization on a chip by providing opportunities to present and discuss the innovative and state-of-the-art design. The scope of the contest covers circuit techniques for (1) Analog / RF / Mixed-Signal Circuits, (2) Digital Signal Processer, (3) Microprocessors, (4) Custom Application Specific Circuits / Memories, and methodologies for (a) Full-Custom / Cell-Based LSIs, (b) Gate Arrays, (c) Field Programmable Devices.

This year, the University LSI Design Contest Committee received 19 designs from five countries/areas, and selected 10 designs out of them. The selected designs will be disclosed in Session 1A with four-minute presentations, followed by live discussions in front of their posters. For the two outstanding designs, The Best Design Award and The Special Feature Award will be presented in the banquet. We sincerely acknowledge the other contributions to the contest, too. It is our earnest belief to promote and enhance research and education in LSI design in academic organizations. Please come to the University LSI Design Contest and enjoy the stimulating discussions.

Last but not least, we would like to express our sincere gratitude to the Council on Electronic Design Automation (CEDA) for their generous sponsorship of this design contest. We would also like to thank all committee members within the UDC review panel for their efforts in reviewing and selecting the papers.

Date: Tuesday, January 21, 2014, 10:40 – 12:20
Location: Suntec City, 3rd level floor

Oral Presentation Room: Room 300
Poster Presentation Room: Room 304

University LSI Design Contest Committee Chair

Chun-Huat Heng
(National Univ. of Singapore, Singapore)

Best Paper Award

Award Winner

2B-1: **"Flexible Packed Stencil Design with Multiple Shaping Apertures for E-Beam Lithography"**
Chris Chu (Iowa State Univ., U.S.A.), Wai-Kei Mak (National Tsing Hua Univ., Taiwan)

Candidates

1B-1: **"Analytical Placement of Mixed-Size Circuits for Better Detailed-Routability"**
Shuai Li, Cheng-Kok Koh (Purdue Univ., U.S.A.)

1C-1: **"Prefetching Techniques for STT-RAM Based Last-Level Cache in CMP Systems"**
Mengjie Mao (Univ. of Pittsburgh, U.S.A.), Guangyu Sun (Peking Univ., China), Yong Li, Alex K. Jones, Yiran Chen (Univ. of Pittsburgh, U.S.A.)

2A-1: **"Bounding Buffer Space Requirements for Real-Time Priority-Aware Networks"**
Hany Kashif, Hiren D. Patel (Univ. of Waterloo, Canada)

2C-1: **"Statistical Analysis of Random Telegraph Noise in Digital Circuits"**
Xiaoming Chen, Yu Wang (Tsinghua Univ., China), Yu Cao (Arizona State Univ., U.S.A.), Huazhong Yang (Tsinghua Univ., China)

3B-1: **"A Network-Flow-Based Optimal Sample Preparation Algorithm for Digital Microfluidic Biochips"**
Trung Anh Dinh, Shigeru Yamashita (Ritsumeikan Univ., Japan), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)

4A-1: **"Physical-Aware Task Migration Algorithm for Dynamic Thermal Management of SMT Multi-Core Processors"**
Bagher Salami (Ferdowsi Univ. of Mashhad, Iran), Mohammadreza Baharani (Univ. of Tehran, Iran), Hamid Noori (Ferdowsi Univ. of Mashhad, Iran), Farhad Mehdipour (Kyushu Univ., Japan)

5B-1: **"Redundant-Via-Aware ECO Routing"**
Hsi-An Chien, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

5C-1: **"Symbolic Computation of SNR for Variational Analysis of Sigma-Delta Modulator"**
Jiandong Cheng, Guoyong Shi (Shanghai Jiao Tong Univ., China)

6A-1: **"Efficient Synthesis of Quantum Circuits Implementing Clifford Group Operations"**
Philipp Niemann (Univ. of Bremen, Germany), Robert Wille (Univ. of Bremen/Cyber Physical Systems DFKI GmbH/Technical Univ. Dresden, Germany), Rolf Drechsler (Univ. of Bremen/Cyber Physical Systems DFKI GmbH, Germany)

6C-2: **"Walking Pads: Fast Power-Supply Pad-Placement Optimization"**
Ke Wang (Univ. of Virginia, U.S.A.), Brett Meyer (McGill Univ., Canada), Runjie Zhang, Kevin Skadron, Mircea Stan (Univ. of Virginia, U.S.A.)

7A-1: **"No△: Leveraging Delta Compression for End-to-End Memory Access in NoC Based Multicores"**
Jia Zhan, Matt Poremba (Pennsylvania State Univ., U.S.A.), Yi Xu (AMD Research, China), Yuan Xie (AMD, China/Pennsylvania State Univ., U.S.A.)

7C-4: **"Suppressing Test Inflation in Shared-Memory Parallel Automatic Test Pattern Generation"**
Jerry C. Y. Ku, Ryan H.-M. Huang, Louis Y. -Z. Lin, Charles H.-P. Wen (National Chiao Tung Univ., Taiwan)

University LSI Design Contest Awards

Best Design Award

1A-1: **"A Dual-loop Injection-locked PLL with All-digital Background Calibration System for On-chip Clock Generation"**

Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Special Feature Award

1A-7: **"A Single-Inductor 8-Channel Output DC-DC Boost Converter with Time-limited Power Distribution Control and Single Shared Hysteresis Comparator"**

Jungmoon Kim, Chulwoo Kim (Korea Univ., Republic of Korea)

10-Year Retrospective Most Influential Paper Award

Award Winner

(ASP-DAC 2004)

2E-2: **"Design Diagnosis Using Boolean Satisfiability"**
Alexander Smith, Andreas Veneris, Anastasios Viglas (Univ. of Toronto, Canada)

Candidates

1D-1: **"Register Binding and Port Assignment for Multiplexer Optimization"**

Deming Chen, Jason Cong (Univ. of California, Los Angeles, USA)

1E-1: **"TranGen: A SAT-Based ATPG for Path-Oriented Transition Faults"**

Kai Yang, Kwang-Ting Cheng, Li-C. Wang (Univ. of California, Santa Barbara, U.S.A.)

3D-1: **"Efficient Translation of Boolean Formulas to CNF in Formal Verification of Microprocessors"**

Miroslav N. Velev (Carnegie Mellon Univ., U.S.A.)

Invitation to ASP-DAC 2015

On behalf of the Organizing Committee, it is my great pleasure to invite all of you to ASP-DAC 2015, which is the 20th event of this Conference series. The Conference will be held from January 19 to 22, 2015 at Makuhari Messe, Chiba, Japan. Makuhari Messe is one of the biggest international convention complexes in Japan and a memorable place where the first ASP-DAC was held in 1995. Hundreds of companies are accumulated around the complex, and big events on various industrial fields including semiconductor and electronics are held every year. As Makuhari Messe is close to Tokyo, about 30 minutes by train, you can easily access the venue from Narita or Haneda international airport. Joining the conference and participating in technological discussions, you can also enjoy many attractions in Tokyo area, such as Tokyo Disneyland, the world-highest tower called Tokyo Sky Tree, Akihabara, etc.

This time, Technical Program Committee (TPC) will be chaired by Professor Naehyuck Chang of Seoul National University. Under his direction, TPC will select qualified papers. The research fields of the conference cover almost all the main technical aspects of LSI-related design methodologies from system to physical level, and please take into consideration of submitting your papers to ASP-DAC 2015. In order to make this conference more attractive and successful, we really need your help and cooperation. The conference has traditionally a strong impact on both industries and academia. We hope the excellent tradition can be deepened and carried forward through this conference. Taking the opportunity of ASP-DAC 2014, we sincerely welcome the attendees from various countries and regions to visit Japan to further carry out technology and academic exchange. ASP-DAC 2015 is waiting for you!

Kunio Uchiyama
General Chair, ASP-DAC 2015

Opening & Keynote I

Tuesday, January 21, 08:30 – 10:00
Venue: Rooms 300 + 301 + 302 (Suntec)

"All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure"

Dr. Ivo Bolsens
Senior VP and CTO, Xilinx, U.S.A.

Abstract: Today's FPGAs have become 'All Programmable SOC Platforms' that integrate in one single device multi-core CPU's, programmable DSP functions, programmable IO and programmable logic, all immersed in a rich and configurable interconnect network. These programmable platform FPGA's allow for the implementation of heterogeneous multi-core architectures that combine traditional CPU's with application-specific processing cores and dedicated data transfer and storage functions. This is enabled by tools that guide designers during the partitioning and mapping of high-level specifications onto a combination of software running on embedded processors and hardware implemented in programmable logic.

FPGAs are well placed to continue to benefit from Moore's law. Advances in process scaling will be augmented with new circuit and architectural improvements along with innovations in system-in-package technology to solve IO challenges and integrate heterogeneous technologies. These innovations will allow designers to build higher performance and lower power systems that optimally exploit the programmable FGPA architecture.

As FPGA platforms continue to deliver more performance at lower cost and lower power, they are becoming the heart of embedded applications such as complex packet processing for networks with line rates of 400+ Gbps; high performance digital signal processing in novel wireless baseband and radio functions; and high flexibility to enable programmable networking and data storage functions in cloud infrastructure.

Keynote II

Wednesday, January 22, 08:30 – 09:30
Venue: Rooms 300 + 301 + 302 (Suntec)

"Designing Analog Functions without Analog Transistors"

Prof. Georges Gielen

Katholieke Universiteit Leuven, Belgium

Abstract: Analog functions are indispensable for most electronic applications, ranging from telecom to biomedical or automotive applications. Yet, designing the analog circuits has become a large burden, especially in advanced CMOS technologies where reduced voltage headrooms and increased variability and reliability problems challenge the design of power-efficient analog circuits. Together with the lack of adequate EDA tools this also jeopardizes efficient analog circuit design. This keynote describes a possible way forward. The industry clearly has reached a bifurcation point. Many applications will leave the scaling race, and adopt older or nonstandard (e.g. flexible organic) technologies for the analog circuits, offering the increased functionality essentially through heterogeneous integration. Many other applications will stick to advanced CMOS, but will shift the analog design paradigm from analog-heavy to digital-heavy minimalistic-analog circuits. The presentation will discuss and illustrate the challenges and solutions in such approach to design analog functions without analog transistors.

Keynote III

Thursday, January 23, 08:30 – 09:30
Venue: Rooms 300 + 301 + 302 (Suntec)

"Beyond Charge-Based Computing"

Prof. Kaushik Roy

Purdue Univ., U.S.A.

Abstract: The trend towards ultra low power logic and low leakage embedded memories for System-On-Chips, has prompted researcher to consider the possibility of replacing charge as the state variable for computation. Recent experiments on spin devices like magnetic tunnel junctions (MTJ's), domain wall magnets (DWM) and spin valves have led to the possibility of using "spin" as state variable for computation, achieving very high density on-chip memories and ultra low voltage logic. High density of memories can be exploited to develop memory-centric reconfigurable computing fabrics that provide significant improvements in energy efficiency and reliability compared to conventional FPGAs. While the possibility of having on-chip spin transfer torque memories is close to reality, several questions still exist regarding the energy benefits of spin as the state variable for logic computation. Latest experiments on lateral spin valves (LSV) have shown switching of nano-magnets using spin-polarized current injection through a metallic channel such as Cu. Such lateral spin valves having multiple input magnets connected to an output magnet using metal channels can be used to mimic "neurons". The spin-based neurons can be integrated with CMOS and other devices like Phase change memories to realize ultra low-power data processing hardware based on neural networks, and are suitable for different classes of applications like, cognitive computing,

programmable Boolean logic and analog and digital signal processing. Note, for some of these applications, CMOS technologies may not be suitable for ultra low power implementation. In this talk I will first discuss the advantages of using spin (as opposed to charge) as state variable for both memory and logic and then present how a cellular array of magneto-metallic devices, operating at terminal voltages ~20mV, can do efficient hybrid digital/analog computation for applications such as cognitive computing. Finally, I will consider recent advances in other non-charge based computing paradigm such as magnetic quantum cellular automata.

Banquet Keynote

Wednesday, January 22, 18:30 – 21:00
Venue: Flower Field Hall, Gardens by the Bay

"The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies"

Mr. Ulf Schneider

Managing Director, Lantiq Asia Pacific/President, SSIA, Singapore

Abstract: Since the mid 1960's Singapore has been an important pillar of the worldwide semiconductor industry, reinventing its portfolio, focus and strategy a few times to keep up with overall trends. Preparing for the next decade, Singapore's industry, research and academia has to put up again the right directions and strategy to keep up with the pace in a more and more competitive global environment. The talk will cover some of the really unique opportunities which Singapore has in this aspect.

Tuesday, January 21, 2014

1K Opening & Keynote I

Time: 8:30 - 10:00
Location: Room 300
Chairs: Yong Lian (National Univ. of Singapore, Singapore), Yajun Ha (National Univ. of Singapore, Singapore)

1K-1 (Time: 9:00 - 10:00)
(Keynote Address) All Programmable SOC FPGA for Networking and Computing in Big Data Infrastructure
Ivo Bolsens (Senior VP and CTO, Xilinx, U.S.A.)

1S Special Session: Normally-Off Computing: Towards Zero Stand-by Power Management

Time: 10:40 - 12:20
Location: Room 302
Organizer: Hiroshi Nakamura (Univ. of Tokyo, Japan)

1S-1 (Time: 10:40 - 11:05)
(Invited Paper) Normally-Off Computing Project : Challenges and Opportunities 1
*Hiroshi Nakamura, Takashi Nakada, Shinobu Miwa (Univ. of Tokyo, Japan)

1S-2 (Time: 11:05 - 11:30)
(Invited Paper) Novel Nonvolatile Memory Hierarchies to Realize "Normally-Off Mobile Processors" 6
*Shinobu Fujita, Kumiko Nomura, Hiroki Noguchi, Susumu Takeda, Keiko Abe (Toshiba, Japan)

1S-3 (Time: 11:30 - 11:55)
(Invited Paper) Normally-Off MCU Architecture for Low-Power Sensor Node 12
*Masanori Hayashikoshi, Yohei Sato, Hiroshi Ueki, Hiroyuki Kawai, Toru Shimizu (Renesas Electronics, Japan)

1S-4 (Time: 11:55 - 12:20)
(Invited Paper) Normally-Off Technologies for Healthcare Appliance 17
*Shintaro Izumi, Hiroshi Kawaguchi, Yoshimoto Masahiko (Kobe Univ., Japan), Yoshikazu Fujimori (Rohm, Japan)

1A University Design Contest

Time: 10:40 - 12:20
Location: Room 300
Chair: Chun Huat Heng (National Univ. of Singapore, Singapore)

1A-1 (Time: 10:40 - 10:44)
A Dual-Loop Injection-Locked PLL with All-Digital Background Calibration System for On-Chip Clock Generation . 21
*Wei Deng, Ahmed Musa, Teerachot Siriburanon, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

1A-2 (Time: 10:44 - 10:48)
A 950μW 5.5-GHz Low Voltage PLL with Digitally-Calibrated ILFD and Linearized Varactor 23
*Sho Ikeda, Tatsuya Kamimura, Sangyeop Lee, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu (Tokyo Inst. of Tech., Japan)

1A-3 (Time: 10:48 - 10:52)
A Swing-Enhanced Current-Reuse Class-C VCO with Dynamic Bias Control Circuits 25
*Teerachot Siriburanon, Wei Deng, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

1A-4 (Time: 10:52 - 10:56)
Design of A High-Performance Millimeter-Wave Amplifier Using Specific Modeling 27
*Xiaojun Bi (National Univ. of Singapore/A*STAR, Singapore), Yongxin Guo (National Univ. of Singapore, Singapore/National Univ. of Singapore (Suzhou) Research Institute, China), M. Annamalai Arasu (A*STAR, Singapore), M. S. Zhnag (National Univ. of Singapore, Singapore), Yong Zhong Xiong, Minkyu Je (A*STAR, Singapore)

1A-5 (Time: 10:56 - 11:00)
A Multi-Mode Reconfigurable Analog Baseband with I/Q Calibration for GNSS Receivers 29
*Zheng Song, Nan Qi, Baoyong Chi, Zhihua Wang (Tsinghua Univ., China)

Tuesday, January 21, 2014

1B Planning and Placement for Design Closure and Manufacturability

Time: 10:40 - 12:20
Location: Room 301
Chairs: Shigetoshi Nakatake (Univ. of Kitakyushu, Japan), Hung-Ming Chen (National Chiao Tung Univ., Taiwan)

1C Circuit, Architecture, and System for Emerging Technologies

Time: 10:40 - 12:20
Location: Room 303
Chairs: Hai (Helen) Li (Univ. of Pittsburgh, U.S.A.), Danghui Wang (Northwestern Polytechnical Univ., China)

Tuesday, January 21, 2014

2S Special Session: EDA for Energy

Time: 13:50 - 15:30
Location: Room 302
Organizer: Fadi Kurdahi (Univ. of California, Irvine, U.S.A.), Sani Nassif (IBM, U.S.A.), Mohammad Al Faruque (Univ. of California, Irvine, U.S.A.)

2A Distributed and Mixed-Criticality Real-Time Systems

Time: 13:50 - 15:30
Location: Room 300
Chair: Muhammad Shafique (Karlsruhe Inst. of Tech., Germany)

2B Advanced Patterning for Advanced Layout

Time: 13:50 - 15:30
Location: Room 301
Chairs: Martin Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.), Shigeki Nojima (Toshiba, Japan)

Tuesday, January 21, 2014

2C Timing-Driven Design, Modeling, and Optimization

Time: 13:50 - 15:30
Location: Room 303
Chairs: Mango Chia-Tso Chao (National Chiao Tung Univ., Taiwan), Tai-Chen Chen (National Central Univ., Taiwan)

3S Special Session: Neuron Inspired Computing using Nanotechnology

Time: 15:50 - 17:30
Location: Room 302
Organizer: Kevin Cao (Arizona State Univ., U.S.A.), Sarma Vrudhula (Arizona State Univ., U.S.A.)

3A Synthesis and Exploration Techniques for Computing Platforms

Time: 15:50 - 17:30
Location: Room 300
Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Kyle Rupnow (Nanyang Technological Univ., Singapore)

Tuesday, January 21, 2014

3B Advances in Microfluidic Biochips

Time: 15:50 - 17:30
Location: Room 301
Chairs: Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Juinn-Dar Huang (National Chiao Tung Univ., Taiwan)

3C Advanced Modeling and Simulation Techniques for Analog/Mixed-Signal Circuits

Time: 15:50 - 17:30
Location: Room 303
Chairs: Hao Yu (Nanyang Technological Univ., Singapore), Shi Guoyong (Shanghai Jiao Tong Univ., China)

Wednesday, January 22, 2014

2K Keynote II

Time: 8:30 - 9:30
Location: Room 300
Chair: Nagisa Ishiura (Kwansei Gakuin Univ., Japan)

2K-1 (Time: 8:30 - 9:30)
(Keynote Address) Designing Analog Functions without Analog Transistors
Georges Gielen (Katholieke Univ. Leuven, Belgium)

4S Special Session: Design Automation Methods for Highly-Complex Multimedia Systems

Time: 10:10 - 12:15
Location: Room 302
Organizer: Sri Parameswaran (Univ. of New South Wales, Australia)

4S-1 (Time: 10:10 - 10:40)
(Invited Paper) SDG2KPN: System Dependency Graph to Function-Level KPN Generation of Legacy Code for MPSoCs 267
Jude Angelo Ambrose, Jorgen Peddersen (Univ. of New South Wales, Australia), Alvin Labios, Yusuke Yachide (Canon Information Systems Research Australia (CiSRA), Australia), *Sri Parameswaran (Univ. of New South Wales, Australia)

4S-2 (Time: 10:40 - 11:10)
(Invited Paper) Low Power Design of the Next-Generation High Efficiency Video Coding 274
*Muhammad Shafique, Jörg Henkel (Karlsruhe Inst. of Tech., Germany)

4S-3 (Time: 11:10 - 11:40)
(Invited Paper) Mapping Complex Algorithm into FPGA with High Level Synthesis 282
*Kazutoshi Wakabayashi, Takashi Takenaka, Hiroaki Inoue (NEC, Japan)

4S-4 (Time: 11:40 - 12:10)
(Invited Paper) Leveraging Parallelism in the Presence of Control Flow on CGRAs 285
Jihyun Ryoo, Kyuseung Han, *Kiyoung Choi (Seoul National Univ., Republic of Korea)

4A System-Level Thermal and Power Optimization Techniques

Time: 10:10 - 12:15
Location: Room 300
Chairs: Yun (Eric) Liang (Peking Univ., China), Wengfai Wong (National Univ. of Singapore, Singapore)

4A-1 (Time: 10:10 - 10:35)
Physical-Aware Task Migration Algorithm for Dynamic Thermal Management of SMT Multi-Core Processors 292
Bagher Salami (Ferdowsi Univ. of Mashhad, Iran), Mohammadreza Baharani (Univ. of Tehran, Iran), Hamid Noori (Ferdowsi Univ. of Mashhad, Iran), *Farhad Mehdipour (Kyushu Univ., Japan)

4A-2 (Time: 10:35 - 11:00)
Agile Frequency Scaling for Adaptive Power Allocation in Many-Core Systems Powered by Renewable Energy Sources 298
*Xiaohang Wang, Zhiming Li (Guangzhou Institute of Advanced Technology, CAS, China), Mei Yang, Yingtao Jiang (Univ. of Nevada, Las Vegas, U.S.A.), Masoud Daneshtalab (Univ. of Turku, Finland), Terrence Mak (Chinese Univ. of Hong Kong, China)

4A-3 (Time: 11:00 - 11:25)
Variation Aware Voltage Island Formation for Power Efficient Near-Threshold Manycore Architectures 304
*Ioannis Stamelakos, Sotirios Xydis, Gianluca Palermo, Cristina Silvano (Politecnico di Milano, Italy)

4A-4 (Time: 11:25 - 11:50)
An Evaluation of an Energy Efficient Many-Core SoC with Parallelized Face Detection 311
*Hiroyuki Usui, Jun Tanabe, Toru Sano, Hui Xu, Takashi Miyamori (Toshiba, Japan)

4A-5 (Time: 11:50 - 12:15)
Energy Aware Real-Time Scheduling Policy with Guaranteed Security Protection 317
*Wei Jiang (Univ. of Electronic Science and Tech. of China, China), Ke Jiang (Linköping Univ., Sweden), Xia Zhang (Univ. of Electronic Science and Tech. of China, China), Yue Ma (Univ. of Notre Dame, U.S.A.)

Wednesday, January 22, 2014

4B Emerging Techniques for Future NoC

Time: 10:10 - 12:15
Location: Room 301
Chairs: Paul Bogdan (Univ. of Southern California, U.S.A.), Wei Zhang (HKUST, Hong Kong)

4C Emerging Applications

Time: 10:10 - 12:15
Location: Room 303
Chairs: Yu Wang (Tsinghua Univ., China), Dajiang Zhou (Waseda Univ., Japan)

Wednesday, January 22, 2014

5S Special Session: Billion Chips of Trillion Transistors

Time: 13:50 - 15:30
Location: Room 302
Organizer: Chen-Yong Cher (IBM, U.S.A.)

5A Simulation and Modeling

Time: 13:50 - 15:30
Location: Room 300
Chairs: Atushi Ike (Fujitsu Labs., Japan), Yuichi Nakamura (NEC, Japan)

5B Reliability Analysis and Enhencement

Time: 13:50 - 15:30
Location: Room 301
Chair: Shigeki Nojima (Toshiba, Japan)

Wednesday, January 22, 2014

5C Variational Design Techniques for Analog/Mixed-Signal Circuits

Time: 13:50 - 15:30
Location: Room 303
Chairs: C.Y. Tsui (Hong Kong Univ. of Science and Tech., Hong Kong), Hideki Asai (Shizuoka Univ., Japan)

6S Special Session: Overcoming Major Silicon Bottlenecks: Variability, Reliability, Validation and Debug

Time: 15:50 - 17:30
Location: Room 302
Organizer: Subhasish Mitra (Stanford Univ., U.S.A.)

6A Synthesis of Quantum Circuits and Adaptive Logic

Time: 15:50 - 17:30
Location: Room 300
Chairs: Yusuke Matsunaga (Kyushu Univ., Japan), Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

Wednesday, January 22, 2014

6B Contemporary Routing

Time: 15:50 - 17:30
Location: Room 301
Chairs: Mark Lin (National Chung Cheng Univ., Taiwan), Toshiyuki Shibuya (Fujitsu Labs., Japan)

6C Power Supply Noise Aware Design Optimization

Time: 15:50 - 17:30
Location: Room 303
Chairs: Wenjian Yu (Tsinghua Univ., China), Shi Guoyong (Shanghai Jiao Tong Univ., China)

Wednesday, January 22, 2014

BK Banquet & Banquet Keynote

Time: 18:30 - 21:00
Location: Flower Field Hall, Gardens by the Bay
Chair: Mashiro Fujita (Univ. of Tokyo, Japan)

BK-1 (Time: 19:30 - 20:00)
(Keynote Address) The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies
Ulf Schneider (Managing Director, Lantiq Asia Pacific/President, SSIA, Singapore)

Thursday, January 23, 2014

3K Keynote III

Time: 8:30 - 9:30
Location: Room 300
Chair: Naehyuck Chang (Seoul National Univ., Republic of Korea)

3K-1 (Time: 8:30 - 9:30)
(Keynote Address) Beyond Charge-Based Computing
Kaushik Roy (Purdue Univ., U.S.A.)

7S Special Session: Brain Like Computing: Modelling, Technology, and Architecture

Time: 10:10 - 12:15
Location: Room 302
Chair: Ahmed Hemani (KTH, Sweden)

7S-1 (Time: 10:10 - 10:40)
(Invited Paper) Spiking Brain Models: Computation, Memory and Communication Constraints for Custom Hardware Implementation 556
*Anders Lansner, Ahmed Hemani, Nasim Farahini (KTH, Sweden)

7S-2 (Time: 10:40 - 11:10)
(Invited Paper) Advanced Technologies for Brain-Inspired Computing 563
*Fabien Clermidy, Rodolphe Heliot, Alexandre Valentian (CEA-LETI, France), Christian Gamrat, Olivier Bichler, Marc Duranton (CEA-LIST, France), Bilel Blehadj, Olivier Temam (INRIA, France)

7S-3 (Time: 11:10 - 11:40)
(Invited Paper) GPGPU Accelerated Simulation and Parameter Tuning for Neuromorphic Applications 570
Kristofor D. Carlson, Michael Beyeler, *Nikil Dutt, Jeffrey L. Krichmar (UC Irvine, U.S.A.)

7S-4 (Time: 11:40 - 12:10)
(Invited Paper) A Scalable Custom Simulation Machine for the Bayesian Confidence Propagation Neural Network Model of the Brain 578
Nasim Farahini, *Ahmed Hemani, Anders Lansner (KTH, Sweden), Fabian Clermidy (CEA-LETI, France), Christer Svensson (Linköping Univ., Sweden)

7A Power and Life Time Issues of Memory Subsystem

Time: 10:10 - 12:15
Location: Room 300
Chairs: Muhammad Shafique (Karlsruhe Inst. of Tech., Germany), Wei Zhang (Hong Kong Univ. of Science and Tech., Hong Kong)

7A-1 (Time: 10:10 - 10:35)
No△:Leveraging Delta Compression for End-to-End Memory Access in NoC Based Multicores 586
*Jia Zhan, Matt Poremba (Pennsylvania State Univ., U.S.A.), Yi Xu (AMD Research, China), Yuan Xie (AMD, China/Pennsylvania State Univ., U.S.A.)

7A-2 (Time: 10:35 - 11:00)
DPA: A Data Pattern Aware Error Prevention Technique for NAND Flash Lifetime Extension 592
Jie Guo, Zhijie Chen (Univ. of Pittsburgh, U.S.A.), Danghui Wang (Northwestern Polytechnical Univ., China), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), *Yiran Chen (Univ. of Pittsburgh, U.S.A.)

7A-3 (Time: 11:00 - 11:25)
Scattered Refresh: An Alternative Refresh Mechanism to Reduce Refresh Cycle Time 598
*T. Venkata Kalyan, Ravi Kasha, Madhu Mutyam (Indian Inst. of Tech. - Madras, India)

7A-4 (Time: 11:25 - 11:50)
A Read-Write Aware DRAM Scheduling for Power Reduction in Multi-Core Systems 604
*Chih-Yen Lai, Gung-Yu Pan, Hsien-Kai Kuo (National Chiao Tung Univ., Taiwan), Jing-Yang Jou (National Central Univ./National Chiao Tung Univ., Taiwan)

7A-5 (Time: 11:50 - 12:15)
A Coherent Hybrid SRAM and STT-RAM L1 Cache Architecture for Shared Memory Multicores 610
*Jianxing Wang, Yenni Tim, Weng-Fai Wong, Zhong-Liang Ong (National Univ. of Singapore, Singapore), Zhenyu Sun, Hai (Helen) Li (Univ. of Pittsburgh, U.S.A.)

Thursday, January 23, 2014

7B Advances in High-Level and Logic Synthesis

Time: 10:10 - 12:15
Location: Room 301
Chairs: Yuko Hara-Azumi (NAIST, Japan), Robert Wille (Univ. of Bremen, Germany)

7C Advanced Test Solutions

Time: 10:10 - 12:15
Location: Room 303
Chairs: Jiun-Lang Huang (National Taiwan Univ., Taiwan), Mango Chia-Tso Chao (National Chiao Tung Univ., Taiwan)

Thursday, January 23, 2014

8S Special Session: Design Flow for Integrated Circuits using Magnetic Tunnel Junction Switched by Spin Orbit Torque

Time: 13:50 - 15:30
Location: Room 302
Organizer: Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

8S-1 (Time: 13:50 - 14:15)
(Invited Paper) An Overview of Spin-Based Integrated Circuits 676
Wang Kang (Univ. Beihang, China/Univ. Paris-Sud, France), *Weisheng Zhao, Zhaohao Wang, Jacques-Olivier Klein, Yue Zhang, Djaafar Chabi (Univ. Paris-Sud, France), Youguang Zhang (Univ. Beihang, China), Dafiné Ravelosona, Claude Chappert (Univ. Paris-Sud, France)

8S-2 (Time: 14:15 - 14:40)
(Invited Paper) Advances in Spintronics Devices for Microelectronics - from Spin-Transfer Torque to Spin-Orbit Torque 684
*Shunsuke Fukami, Hideo Sato, Michihiko Yamanouchi, Shoji Ikeda, Fumihiro Matsukura, Hideo Ohno (Tohoku Univ., Japan)

8S-3 (Time: 14:40 - 15:05)
(Invited Paper) Hybrid CMOS/Magnetic Process Design Kit and SOT-Based Non-Volatile Standard Cell Architectures 692
*Gregory Di Pendina, Kotb Jabeur, Guillaume Prenat (Spintec Laboratory, CEA-INAC/CNRS/UJF/G-INP, France)

8S-4 (Time: 15:05 - 15:30)
(Invited Paper) Architectural Aspects in Design and Analysis of SOT-Based Memories 700
Rajendra Bishnoi, Mojtaba Ebrahimi, Fabian Oboril, *Mehdi Tahoori (Karlsruhe Inst. of Tech., Germany)

8A Analysis, Optimization, and Scheduling for Multiprocessor Platforms

Time: 13:50 - 15:30
Location: Room 300
Chairs: Sebastian Steinhorst (TUM CREATE, Singapore), Akash Kumar (National Univ. of Singapore, Singapore)

8A-1 (Time: 13:50 - 14:15)
Timing Anomalies in Multi-Core Architectures due to the Interference on the Shared Resources 708
*Hardik Shah, Kai Huang, Alois Knoll (Technical Univ. Munich, Germany)

8A-2 (Time: 14:15 - 14:40)
A Unified Online Directed Acyclic Graph Flow Manager for Multicore Schedulers 714
*Karim Kanoun, David Atienza (École Polytechnique Fédérale de Lausanne, Switzerland), Nicholas Mastronarde (State Univ. of New York at Buffalo, U.S.A.), Mihaela van der Schaar (Univ. of California, Los Angeles, U.S.A.)

8A-3 (Time: 14:40 - 15:05)
Variation-Aware Statistical Energy Optimization on Voltage-Frequency Island Based MPSoCs under Performance Yield Constraints 720
*Song Jin (North China Electric Power Univ., China), Yinhe Han (Chinese Academy of Sciences, China), Songwei Pei (Beijing Univ. of Chemical Tech., China)

8A-4 (Time: 15:05 - 15:30)
QoS-Aware Dynamic Resource Allocation for Spatial-Multitasking GPUs 726
*Paula Aguilera, Katherine Morrow, Nam Sung Kim (Univ. of Wisconsin - Madison, U.S.A.)

8B Advances in Formal Verification and Debugging

Time: 13:50 - 15:30
Location: Room 301
Chairs: Charles H.-P. Wen (National Chiao Tung Univ., Taiwan), Vishvender Singh (Infineon Technologies Asia-Pacific, Singapore)

8B-1 (Time: 13:50 - 14:15)
Automated Debugging of Missing Assumptions 732
Brian Keng (Univ. of Toronto, Canada), Evean Qin (Vennsa Technologies, Canada), *Andreas Veneris, Bao Le (Univ. of Toronto, Canada)

Thursday, January 23, 2014

8C Advances in CAD Techniques for Signal Integrity

Time: 13:50 - 15:30
Location: Room 303
Chairs: Rung-Bin Lin (Yuan Ze Univ., Taiwan), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

9S Special Session: The Role of Photons in Harming or Increasing Security

Time: 15:50 - 17:30
Location: Room 302
Organizer: Francesco Regazzoni (Univ. of Lugano, Switzerland), Edoardo Charbon (Delft Univ. of Tech., Netherlands)

Thursday, January 23, 2014

9A System-Level Verification

Time: 15:50 - 17:30
Location: Room 300
Chairs: Yinhe Han (Chinese Academy of Sciences, China), Akash Kumar (National Univ. of Singapore, Singapore)

9B Modeling and Evaluator for Emerging Technologies

Time: 15:50 - 17:30
Location: Room 301
Chairs: Guangyu Sun (Peking Univ., China), Wei Zhang (Hong Kong Univ. of Science and Tech., Hong Kong)

9C Design and Simulation Toward Power and Temperature Awareness

Time: 15:50 - 17:30
Location: Room 303
Chairs: Yasuhiro Takashima (Univ. of Kitakyushu, Japan), Yukihide Kohira (Univ. of Aizu, Japan)

Thursday, January 23, 2014

Tutorials

ASP-DAC has changed the format for the tutorials. Instead of full-day, in-depth tutorials, participants can choose two 3-hour tutorials – one in the morning session and one in the afternoon. For each session, four options are available – two in the physical-design (PD) domain and two in the system-design (SD) domain.

TUTORIAL-PD1: Energy-efficient Datacenters

Lead Organizer: Massoud Pedram (Univ. of Southern California, U.S.A.)
Speakers: (1) Massoud Pedram (Univ. of Southern California, U.S.A.)
Time: 20 January 2014, 09:00 - 12.00 Location: Room 303

Tutorial Outline:

Pervasive use of cloud computing and the resulting rise in the number of datacenters and hosting centers (which provide platform or software services to clients who do not have the means to set up and operate their own compute facilities) have brought forth many concerns including the electrical energy cost, peak power dissipation, cooling, carbon emission, etc. With power consumption becoming an increasingly important issue for the operation and maintenance of the hosting centers, corporate and business owners are becoming increasingly concerned. Furthermore, provisioning resources in a cost-optimal manner so as to meet different performance criteria such as throughput or response time has become a critical challenge. The goal of this talk is to provide an introduction to resource provisioning and power/thermal management problems in datacenters and to review strategies that maximize the datacenter energy efficiency subject to peak/total power consumption and thermal constraints while at the same time meeting stipulated service level agreements in terms of task throughput and/or response time.

TUTORIAL-PD2: Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyber-physical System Integration

Lead Organizer: Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)
Speakers: (1) Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)
(2) Krishnendu Chakrabarty (Duke Univ., U.S.A.)
Time: 20 January 2014, 14:00 – 17:00 Location: Room 303

Tutorial Outline:

This tutorial will first provide an overview of typical bio-molecular applications (market drivers) such as immunoassays, DNA sequencing, clinical chemistry, etc. Next, microarrays and various microfluidic platforms will be discussed. The next part of the tutorial will focus on electro-wetting-based digital microfluidic biochips. The key idea here is to manipulate liquids as discrete droplets. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial. Attendees will learn about CAD, design-for-testability, and reconfiguration aspects of digital microfluidic biochips. Synthesis tools will be described to map assay protocols from the lab bench to a droplet-based microfluidic platform and generate an optimized schedule of bioassay operations, the binding of assay operations to functional units, and the layout and droplet-flow paths for the biochip. The role of the digital microfluidic platform as a "programmable and reconfigurable processor" for biochemical applications will be highlighted. Cyber-physical integration using low-cost sensors and adaptive control, software will be highlighted. Cost-effective testing techniques will be described to detect faults after manufacture and during field operation. On-line and off-line reconfiguration techniques will be presented to easily bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. With the availability of these tools, chip

users and chip designers will be able to concentrate on the development and chip-level adaptation of nano-scale bioassays (higher productivity), leaving implementation details to CAD tools.

TUTORIAL-PD3: On Variability and Reliability; Dynamic Margining and Low Power

Lead Organizer: Fadi Kurdahi (Univ. of California - Irvine, U.S.A.)
Speakers: (1) Fadi Kurdahi (University of California - Irvine, USA)
(2) Greg Taylor (Intel Research Lab, U.S.A.)
(3) Ahmed Eltawil (Univ. of California - Irvine, U.S.A.)
(4) Amin Khajeh (Intel Research Lab, U.S.A.)
Time: 20 January 2014, 09:00 – 12:00 Location: Room 304

Tutorial Outline

The design for manufacturing and yield (DFM&Y) is fast becoming an indispensable consideration in today's SoCs. Most current flows only consider manufacturability and yield at the lowest levels: process, layout and circuit. As such, these metrics are treated as an afterthought. With advanced process nodes, it has become increasingly expensive --and soon prohibitive-- to guarantee bit level error free chips. The challenge now is to design reliable systems using chips that may have some faults, and hence leads to approaches that consider DFM&Y at the system level where more benefit can be reaped, and to consider the problem across the design layers. This tutorial covers cross layer approach to design for DFM&Y spanning from the application all the way to manufacturing, overviews various techniques being explored today, and demonstrates its effectiveness on key applications including wireless communication systems (using 3G and 4G as the transmission physical layer), and multimedia applications (H.264 and H.265). The results confirm that there is a significant opportunity for cross-layer error exploitation, resulting in an expanded design space with interesting design points that would otherwise have not been discovered by SoC designers.

We then proceed to describe a scalable, unified statistical model that accurately reflects the impact of random hardware failures (embedded memory as an example) due to power management policies on the overall performance of a communication system. This enables system designers to efficiently and accurately determine the effectiveness of novel power management techniques and algorithms that are designed to manage both hardware failure and communication channel noise. We will also present early work on extending the modeling strategy to logic blocks. To illustrate those concepts, the tutorial will explore application-aware power management technique based on autonomous learning for power management. The tutorial will discuss using techniques such as Q learning to learn the dynamics of the system over time and apply the optimal parameters to save power. This will be presented in the context of a wireless DVB and WiMax system.

TUTORIAL-PD4: Architecture Level Thermal Modeling, Prediction and Management for Multi-core and 3D Microprocessors

Lead Organizer: Sheldon Tan (Univ. of California - Riverside, U.S.A.)
Speakers: (1) Sheldon Tan (Univ. of California - Riverside, U.S.A.)
(2) Hai Wang (Univ. of Electronic Science and Technology, China)
Time: 20 January 2014, 14:00 – 17:00 Location: Room 304

Tutorial Outline:

Temperature has become a major concern for high performance microprocessor and package design as more devices are integrated on a chip. This problem becomes more severe as the VLSI technology scales to the nanometer ranges. Excessively high on-chip temperature can cause many severe problems such as reduced reliability of chips and elevated cooling cost of the packaging. As a result, temperature estimation, prediction and runtime thermal management are critical to reduce hot spots, improve reliability for today's high performance multi-core micro-processors.

In the first part of the tutorial, we will describe several new architecture level thermal modeling and analysis techniques. We will first present moment matching based fast thermal analysis algorithm, called TMM and compare it with HotSpot-based thermal analysis method. We then present a new compact behavioral thermal modeling technique for multi-core microprocessor designs. In the second part of this tutorial, we will present a new method to accurately estimate and predict the full-chip temperature at runtime under more practical conditions where we have inaccurate thermal model, less accurate power estimations and limited number of on-chip physical thermal sensors. The new approach employs a number of new techniques to address this problem by error compensation method, correlation-modeling scheme and time-series power prediction techniques. A number of examples based on Intel quad-core microprocessors will be presented. In the third part of this tutorial, we will present is a new distributed dynamic thermal management scheme for reducing the temperature variations across the chip. Instead of intuitively assigning the heavy tasks to the low temperature cores to balance the thermal profile based on steady state thermal analysis, the new method applies moment matching based frequency-domain thermal analysis techniques for fast thermal estimation and prediction to guide task assignment process. The resulting algorithm can lead to significant reduction of hot spots without full transient thermal simulation, which will benefit the system reliability.

TUTORIAL-SD1: High-Level Specifications to Cope With Design Complexity

Lead Organizer: Gunar Schirner (Northeastern Univ., U.S.A.)

Speakers: (1) Gunar Schirner (Northeastern Univ., U.S.A.)
(2) Wolfgang Müller (Univ. of Paderborn, Germany)
(3) Eugenio Villar (Univ. of Cantabria, Spain)
(4) Rainer Dömer (Univ. of California at Irvine, U.S.A.)

Time: 20 January 2014, 14:00 – 17:00 Location: Room 306

Tutorial Outline:

Design abstractions are key to deal with design complexity of high-performance computer system, mobile embedded system, and real-time automobile system. In Electronic System Level (ESL) design we have enjoyed abstractions above the Register Transfer Level (RTL) up to Transaction Level Modeling (TLM). Much research work starts with a behavioral specification of the system functionality captured in a System-Level Description Language (SLDL) and then focuses on identifying heterogeneous allocation, mapping and scheduling. However, less attention has been given on how to obtain such a behavioral specification, which already determines the quality and performance of the final system to a large degree. Crucial aspects already locked down include algorithm quality, parallelization potential (task-, data-, and instruction-level parallelism), demands on local data storage, and amount of traffic. Therefore a sufficiently flexible, parallelism exposing specification is paramount to enable meaningful design space evaluation.

This tutorial discusses the topics of creating and validating a "good" system specification from complementary perspectives. The first talk titled "*From Requirements Specification to Executable Testbenches - Methodologies and Standards*" deals with how high-level system requirements, captured in a natural language, can be translated into a testbench for validating the specifications correctness. The second presentation "*Conceptual Abstraction Levels (CALs): From Concept to Executable Functional Specification*" looks into higher abstraction levels that aid the designer in defining a behavioral specification traversing tradeoffs of quality, performance and traffic with a focus on embedded vision systems. The third talk "*Modeling and SW synthesis for heterogeneous embedded systems in UML/MARTE*" highlights opportunities and methods to describe, simulate and automatically generate the SW stacks on heterogeneous platforms using UML/MARTE. The fourth presentation "*Designer-in-the-Loop Recoding to Create Safe Parallel ESL Models*" introduces a

modeling environment and methodology that aids the system designer in obtaining a model specification with safe parallelism when starting from abundantly available flat C-code.

TUTORIAL-SD2: Many-core and Heterogeneous System-Level Verification Methodology

Lead Organizer: Alex Goryachev (IBM Research - Haifa, Israel)
Speakers: (1) Alex Goryachev (IBM Research - Haifa, Israel)
(2) Ronny Morad (IBM Research - Haifa, Israel)
Time: 20 January 2014, 09:00 – 12:00 Location: Room 306

Tutorial Outline:
Many companies today employ many-core and heterogeneous architectures for their systems to meet the growing needs of high performance products with low power consumption. These architectures significantly increase the complexity of SoCs, especially at the system-level. Being on the critical path of the product development, system-level verification is the bottleneck for such projects. Traditional verification approaches do not provide an adequate solution to this challenge since they view a system as a combination of individual components, and they concentrate on SW-HW co-verification at the system-level. In this tutorial, we present a proven methodology to deal with such systems. The key points of our methodology are:

– Treat the system as a whole rather than merely a combination of diverse individual components. By doing so, our method is able to verify complex interdependencies between various system components.

– Focus on HW-only integration level as opposed to SW and HW. This does not mean SW-HW co-verification is not a required step in system verification: one must verify how the real HW works with the real SW. However, our method does not require the real SW, thus allowing early verification. This also makes our approach more suitable for verifying general-purpose aspects of system architecture that are present in most of the SoCs today.

– Include technologies and toolset that support the methodology for system- level verification, including test plan definition, intelligent test-case generation, checking, and coverage.

Our methodology has been widely used within IBM across several product lines: Power Systems, System z, as well as gaming consoles and other SoCs. In addition to presenting our methodology, we also address the role of system- level verification in the overall verification cycle, its goals and challenges.

TUTORIAL-SD3: The Formal Specification Level: Bridging the Gap between the Spec and its Implementation

Lead Organizer: Robert Wille (Univ. of Bremen, Germany)
Speakers: Prof. (1) Robert Wille (Univ. of Bremen, Germany)
(2) Rainer Findenig (Intel Mobile Communication, Austria)
(3) Rolf Drechsler (DFKI GmbH, Germany)
Time: 20 January 2014, 14.00 pm – 17.00 pm Location: Room 307

Tutorial Outline:
For the design of modern cyber-physical embedded and automobile system, the starting point of each design process usually is given by means of a textual specification provided in a natural language. But in order to perform even the simplest automatic synthesis techniques, an initial implementation is generated -- usually at the Electronic System Level (ESL) by means of high-level

programming languages such as SystemC. This process is expensive, time-consuming, and requires a large number of well-trained design engineers. In fact, this process builds the major bottleneck in today's design flows. Consequently, designers are constantly striving for higher levels of abstraction to bridge the gap between the initial spec and the resulting implementation. After the gate level, the Register Transfer Level (RTL), and the Electronic System Level (ESL), researchers are increasingly considering the Formal Specification Level (FSL). Here, modeling languages such as the Unified Modeling Language (UML) or the System Modeling Language (SysML) are applied. They allow for a formal specification of the structure and the behavior of a system while, at the same time, abstracting from precise implementation details.

In fact, the FSL is particularly suited to address the bottleneck mentioned above since: 1) initial solutions exist to automatically derive a respective FSL description from a given informal specification using techniques of Natural Language Processing (NLP); 2) crucial design flaws can already be detected at the specification level and, thus, before any line of code is written; and 3) the description means of the FSL provide a proper input for automatic code generation techniques. The tutorial addresses hardware- and software engineers from industry and academia, as well as students of computer science, electrical engineering, or similar areas. The focus is on early phases within the design flow, i.e. the transformation of an initial specification into a first implementation.

TUTORIAL-SD4: High-Level Synthesis for Low-Power Design

Lead Organizer: Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)
Speakers: (1) Zhiru Zhang (Cornell Univ., U.S.A.)
(2) Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)
Time: 20 January 2014, 09:00 – 12.00 Location: Room 307

Tutorial Outline:

The IC industry has undergone a significant transition from performance-constrained design to power-constrained design. In order to meet stringent power requirement, designers often have to optimize the initial RTL in an ad hoc manner, with consideration of functional, structural, temporal, and spatial information needed for applying various low-power optimization techniques, such as clock and/or power gating, multi- Vdd and multi-clock designs, etc. In this light, high-level synthesis (HLS), which enables automatic generation of optimized hardware from high-level programming languages and facilitates effective exploration of software and hardware architectures, is a promising direction to improve design productivity and at the same time address the increasing difficulty to meet power budgets. In spite of multiple technical challenges of accurately estimating power above the RT level, we believe that promoting power as a first-order design objective is crucial for HLS to attain wider adoption in the design community. Advances in this area have the potential to significantly reduce the turnaround time in achieving the power closure.

In this tutorial, we will first provide an overview of the state-of-the-art HLS technologies, including the general design methodologies, major synthesis steps, and key optimization techniques. In particular, we will dis- cuss the common practices of using commercial/academic HLS tool flows to explore the design space and derive low-power implementations. We will then provide an in-depth coverage of various low-power optimization techniques and synthesis algorithms in HLS, including high-level power estimation techniques, scheduling and binding algorithms for static and dynamic power reductions and behavior-level observability analysis for clock and/or power gating. Tutorial presentations will encompass two segments, with the first segment focusing on the general HLS methodologies and various specific low-power optimization and synthesis techniques, and the second segment on the FCUDA compilation and synthesis flow for energy-efficient computing.

Tutorials at a Glance

	Monday, 20 January 2014			
	Room: 303	Room: 304	Room: 306	Room: 307
09:00	**Tutorial-PD1:** Energy-Efficient Datacenters	**Tutorial-PD3:** On Variability and Reliability; Dynamic Margining and Low Power	**Tutorial-SD2:** Many-core and Heterogeneous System-Level Verification Methodology	**Tutorial-SD4:** High-Level Synthesis for Low-Power Design
12:00				
	Lunch Break (12:00 – 14:00)			
14:00	**Tutorial-PD2:** Digital Microfluidic Biochips: Towards Hardware/Software Co-Design and Cyber-Physical System Integration	**Tutorial-PD4:** Architecture Level Thermal Modeling, Prediction and Management for Multi-Core and 3D Microprocessors	**Tutorial-SD1:** High-Level Specifications to Cope with Design Complexity	**Tutorial-SD3:** The Formal Specification Level: Bridging the Gap between the Spec and its Implementation
17:00				

- Tea refreshments will be provided @ 10:20 – 1040 and @ 15:20 – 15:40

At a Glance

	Tuesday, 21 January 2014			
	Room: 302	Room: 300	Room: 301	Room: 303
08:30 10:00	**Opening & Keynote I** (Room 300 + Room 301 + Room 302)			
	Break			
10:40 12:20	**1S (Special Session):** Normally-Off Computing: Towards Zero Stand-by Power Management	**1A (UDC):** University Design Contest	**1B:** Planning and Placement for Design Closure and Manufacturability	**1C:** Circuit, Architecture, and System for Emerging Technologies
	Lunch Break/**University Design Contest Discussion** (Room 304)			
13:50 15:30	**2S (Special Session):** EDA for Energy	**2A:** Distributed and Mixed-Criticality Real-Time Systems	**2B:** Advanced Patterning for Advanced Layout	**2C:** Timing-Driven Design, Modeling, and Optimization
	Coffee Break			
15:50 17:30	**3S (Special Session):** Neuron Inspired Computing using Nanotechnology	**3A:** Synthesis and Exploration Techniques for Computing Platforms	**3B:** Advances in Microfluidic Biochips	**3C:** Advanced Modeling and Simulation Techniques for Analog/Mixed-Signal Circuits

	Wednesday, 22 January 2014			
	Room: 302	Room: 300	Room: 301	Room: 303
08:30 09:30	**Keynote II** (Room 300 + Room 301 + Room 302)			
	Break			
10:10 12:15	**4S (Special Session):** Design Automation Methods for Highly-Complex Multimedia Systems	**4A:** System-Level Thermal and Power Optimization Techniques	**4B:** Emerging Techniques for Future NoC	**4C:** Emerging Applications
	Lunch Break			
13:50 15:30	**5S (Special Session):** Billion Chips of Trillion Transistors	**5A:** Simulation and Modeling	**5B:** Reliability Analysis and Enhancement	**5C:** Variational Design Techniques for Analog/Mixed-Signal Circuits
	Coffee Break			
15:50 17:30	**6S (Special Session):** Overcoming Major Silicon Bottlenecks: Variability, Reliability, Validation, and Debug	**6A:** Synthesis of Quantum Circuits and Adaptive Logic	**6B:** Contemporary Routing	**6C:** Power Supply Noise Aware Design Optimization
	Break			
18:30 21:00	**Banquet & Banquet Keynote (**Flower Field Hall, Gardens by the Bay*)			

* Transportation will be provided; please refer to page 51 for more details

	Thursday, 23 January 2014			
	Room: 302	Room: 300	Room: 301	Room: 303
08:30 09:30	**Keynote III** (Room 300 + Room 301 + Room 302)			
	Break			
10:10 12:15	**7S (Special Session):** Brain Like Computing: Modelling, Technology, and Architecture	**7A:** Power and Life Time Issues of Memory Subsystem	**7B:** Advances in High-Level and Logic Synthesis	**7C:** Advanced Test Solutions
	Lunch Break			
13:50 15:30	**8S (Special Session):** Design Flow for Integrated Circuits using Magnetic Tunnel Junction Switched by Spin Orbit Torque	**8A:** Analysis, Optimization, and Scheduling for Multiprocessor Platforms	**8B:** Advances in Formal Verification and Debugging	**8C:** Advances in CAD Techniques for Signal Integrity
	Coffee Break			
15:50 17:30	**9S (Special Session):** The Role of Photons in Harming or Increasing Security	**9A:** System-Level Verification	**9B:** Modeling and Evaluator for Emerging Technologies	**9C:** Design and Simulation Toward Power and Temperature Awareness

Supporter's Exhibition

Supporter's exhibition is held in ASP-DAC 2014. 2 companies support ASP-DAC 2014 and have exhibition booths. The supporter's exhibition is presented at Room 304 from January 21 through January 23.

Exhibit Hours*: **10:00 – 17:30, January 21**
09:00 – 17:30, January 22
09:00 – 17:30, January 23

* Time may change

Location: **Room 304**

TOSHIBA Leading Innovation Toshiba Email: mari.takada@toshiba.co.jp http://www.toshiba.com	"FlashAir" is an SD memory card with embedded wireless LAN functionality. It has a built-in web server function and a wireless LAN access point. If power is supplied to the card, FlashAir can work as a server. Files stored in FlashAir are accessible from smartphones, tablets or PCs through Wi-Fi. Ad-hoc local networks between FlashAir and mobile devices are established, so that Internet access or Wi-Fi access points are not needed. We provide an on-site download service, accessible only at ASP-DAC 2014 venues with FlashAir. The API of FlashAir is disclosed on the developer site. https://www.flashair-developers.com
SILICON CLOUD INTERNATIONAL Silicon Cloud International Pte Ltd. Email: tony.ng @siliconcloudinternational.com http://www.siliconcloudinterntional.com	Incorporated in Singapore, Silicon Cloud International (SCI) establishes secure and multi-tenant cloud computing centers for universities and research institutions. As an initial application, SCI's cloud is providing a turn-key Integrated Circuits (IC) design infrastructure. The design infrastructure is all encompassing and includes PDK (Process Design Kit), EDA software tools, design IP, integrated design flows, virtualized and scalable computing resources, and IC design training packages. SCI's private cloud and thin client architecture establishes a novel security model through which university academics and researchers can safely and confidently collaborate with each other and their industry partners on leading edge semiconductor design. SCI will participate in this year's 2014 Asia South Pacific Design Automation Conference in Singapore as an exhibitor and presenter to showcase the next wave in cloud-based inter-organizational IC design and university-industry collaboration.

Social Events

[1] Welcome Reception /Welcome Cocktail

Date: Monday, 20 January 2014
Time: 18:00 – 20:00
Venue: Room 309 + Room 310 (Suntec)

Food and drinks will welcome ASP-DAC 2014 attendees.

[2] Conference Banquet

Date: Wednesday, 22 January 2014
Time: 18:30 – 21:00
Venue: Flower Field Hall, Gardens by the Bay

Conference banquet will offer you a good opportunity to promote friendship with all ASP-DAC 2014 attendees. Highlights include

- Delicious food;
- A Banquet Keynote entitled "The Art of Innovation - How Singapore Will Continue to Drive the Progress in Semiconductor Technologies" by Ulf Schneider (Managing Director, Lantiq Asia Pacific/President, SSIA, Singapore);
- A sensory experience of beautiful scenes within the Flower Dome, Gardens by the Bay;
- Performance.

Remarks:

- Transportation will be provided between the conference venue and banquet venue. All guests **MUST** gather at the **Main Driveway** (see the location map at page 55) by **17:35**.
- An additional ticket costs S$150. Please find more information on the registration site.

Information

Proceedings:

ASP-DAC 2014 will be producing a USB of the ASP-DAC 2014 Proceedings. Conference registration in any of the categories will include it. Additional Proceedings will be available for purchase at the Conference. Price is as follows:

Additional ASP-DAC 2014 Proceedings: S$30

Climate:

Singapore has a tropical climate. Temperature ranges from a low of 24ºC to a high of around 31ºC every day, and relative humidity is high.

Currency Exchange:

Singapore dollar (S$) is accepted at stores and restaurants. You can exchange your currency for S$ at foreign exchange banks and authorized money exchange offices.

Electricity:

The electrical power supply is 230V at 50Hz. Three pin-sockets are the norm.

Shopping:

The business hours of most department stores are from 10:00 to 22:00. Department stores and most tourist attraction places are open 7 days a week.

Sightseeing:

You may browse the following website:
http://www.yoursingapore.com/content/traveller/en/experience.html

SENTOSA

Sentosa is a popular island resort in Singapore. Attractions include a 3.2km stretch of sandy white shores for different watersports, Imbiah Lookout – a cluster of attractions for adventure-seekers & nature lovers, Siloso Point – a home to many edutainment attractions, and the Resorts World Sentosa, featuring the theme park Universal Studios Singapore. For more information about Sentosa, please visit http://www.sentosa.com.sg/en/.

MARINA BAY

Marina Bay is a place for people for all walks of life to explore, exchange and entertain. Attractions nearby include an integrated resort – Marina Bay Sands, ArtScience Museum, Esplanade, Singapore Flyers, Gardens by the Bay, Merlion Park, etc. For more information about Marina Bay, please visit http://www.marina-bay.sg/attractions.html.

CHINA TOWN

China Town is an ethnic neighborhood featuring distinctly Chinese cultural elements. China Town is now an extremely vibrant place for shopping, walking around, sightseeing and eating. Be enjoyed in the China Town, with its stunning lights-up, night markets, decorations and various celebrations (especially before and after Chinese New Year). For visitors' information, the Chinese New Year 2014 will be on January 31, 2014.

ORCHARD ROAD

As a shopper's haven, Orchard Road is a swanky one-way boulevard flanked by distinctive and iconic shopping malls, restaurants and hotels. The shopping belt offers retail, dining and entertainment options to please any taste or budget - from opulent brands to high street fashion, and exclusive restaurants to fast food joints.

SINGAPAORE ZOO, NIGHT SAFARI, RIVER SAFARI, JURONG BIRD PARK

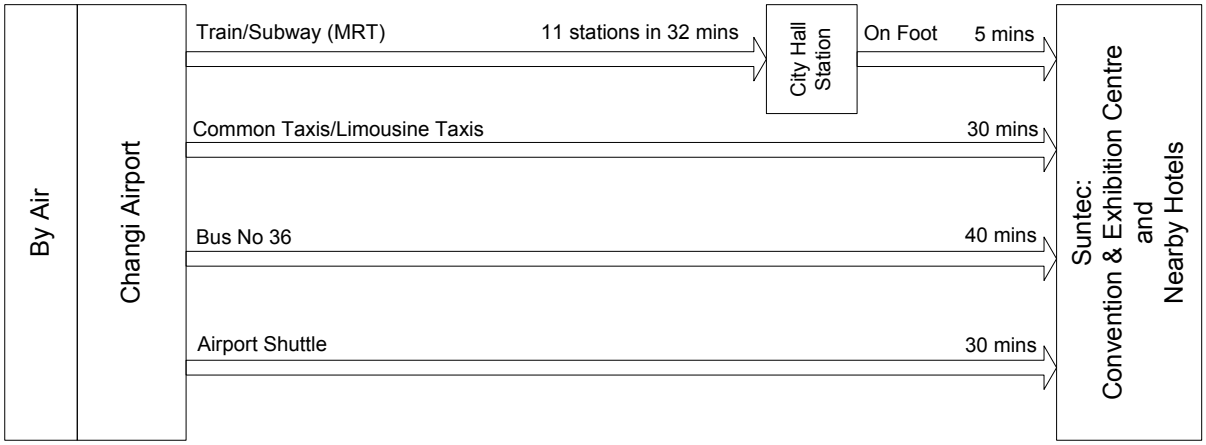
Singapore has several wildlife reserve attractions. These attractions are evolving from being "viewing" parks to "learning" parks, providing an experiential learning experience for visitors who will learn more about animals, birds, plants and the environment through sight/sounds, and to gain awareness on the need for conservation of wildlife. For more information, please visit http://www.wrs.com.sg/.

Other Information:

SINGAPORE CHANGI AIRPORT
http://www.changiairport.com/
SUNTEC INTERNATIONAL CONVENTION & EXHIBITION CENTRE
http://www.suntecsingapore.com
SINGAPORE TRANSPORTATION INFORMATION
http://www.smrt.com.sg/Home.aspx

Access to Suntec, Singapore

❖ Traffic information:



❖ Estimated cost (from Changi Airport to Suntec):
- By Train/Subway (MRT): ~S$2
- By Common Taxis: ~S$18 to ~S$38 depending on the sub-charges
- By Limousine Taxis: ~S$55 to ~S$60
- By Bus (no. 36): ~S$2
- By Airport Shuttle: ~S$9

More transportation information at Singapore Changi Airport, please visit http://www.changiairport.com/getting-around/to-and-from-the-airport.

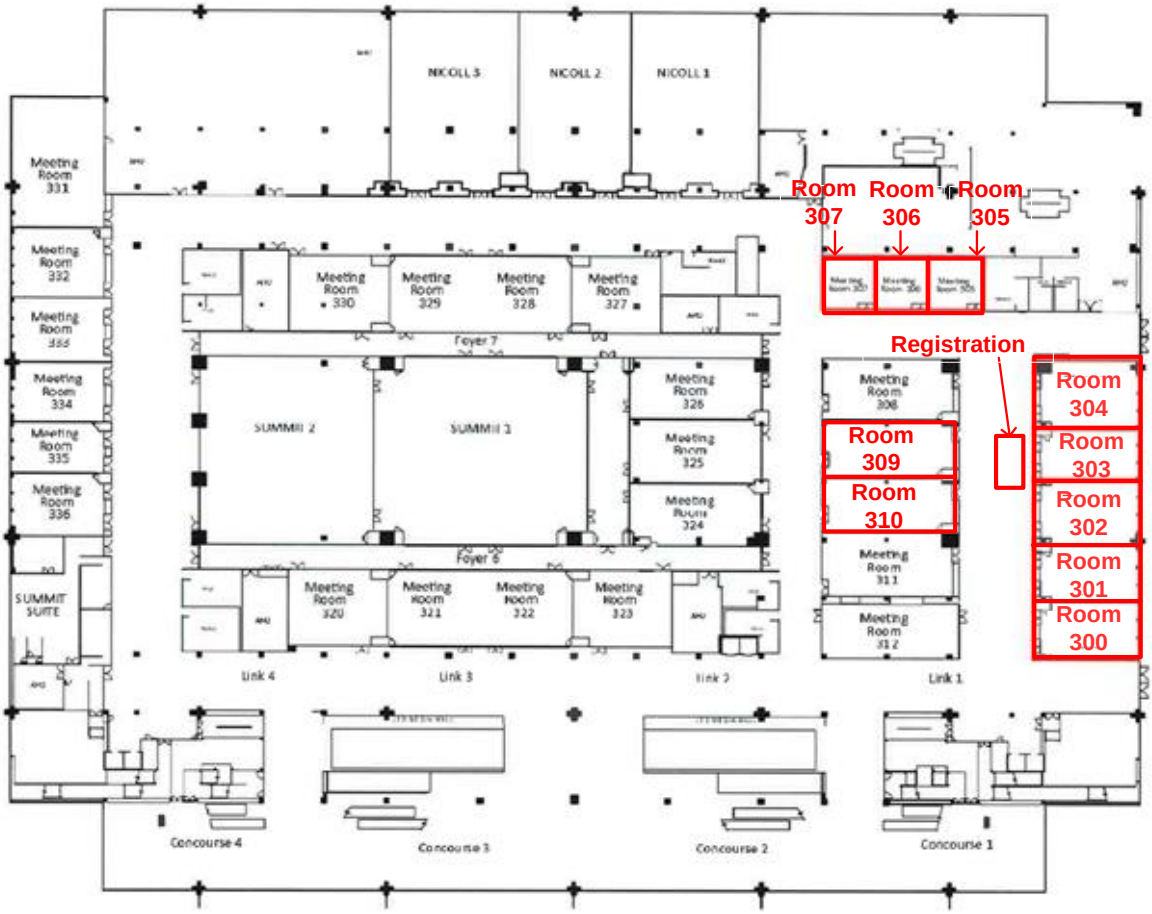
❖ 2014 ASP-DAC Conference is held at Suntec Convention and Exhibition Center:

Room Assignment/Venue Map

- ASP-DAC 2014 is held at Suntec, 3rd level floor.
- The registration/information desk will be at the foyer of Room 303 (see the location map at page 55).
- Speakers' Breakfast will be from 07:00 – 08:00 @ Room 310 from 21 – 23 Jan 2014.
- The Rehearsal Room (Room 304 or Room 305) will be open from 08:00 to 18:00.

Room Assignment

Date / Room	20 Jan 2014	21 Jan 2014	22 Jan 2014	23 Jan 2014
Room 300		Opening, Keynote I / Session A	Keynote II / Session A	Keynote III / Session A
Room 301		Opening, Keynote I / Session B	Keynote II / Session B	Keynote III / Session B
Room 302		Opening, Keynote I / Session S	Keynote II / Session S	Keynote III / Session S
Room 303	Tutorial-PD1 / Tutorial-PD2	Session C	Session C	Session C
Room 304	Tutorial-PD3 / Tutorial-PD4	Poster / Exhibition / Rehearsal Room / Slide Check	Poster / Exhibition / Rehearsal Room / Slide Check	Poster / Exhibition / Rehearsal Room / Slide Check
Room 305	Secretariat / Rehearsal Room	Secretariat	Secretariat	Secretariat
Room 306	Tutorial-SD1 / Tutorial-SD2	Meeting / Working Room	Meeting / Working Room	Meeting / Working Room
Room 307	Tutorial-SD3 / Tutorial-SD4			
Room 309	Welcome Reception			
Room 310	Welcome Reception	Speakers' Breakfast	Speakers' Breakfast	Speakers' Breakfast



Location Map for Rooms (3rd floor, Suntec)

Pickup Location for Conference Banquet (1st floor, Suntec)

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Visit our website
http://www.aspdac.com/

ASP-DAC 2014 SECRETARIAT

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