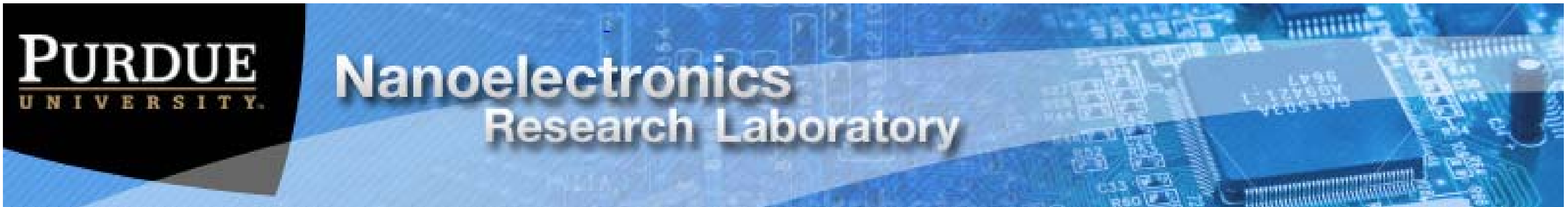


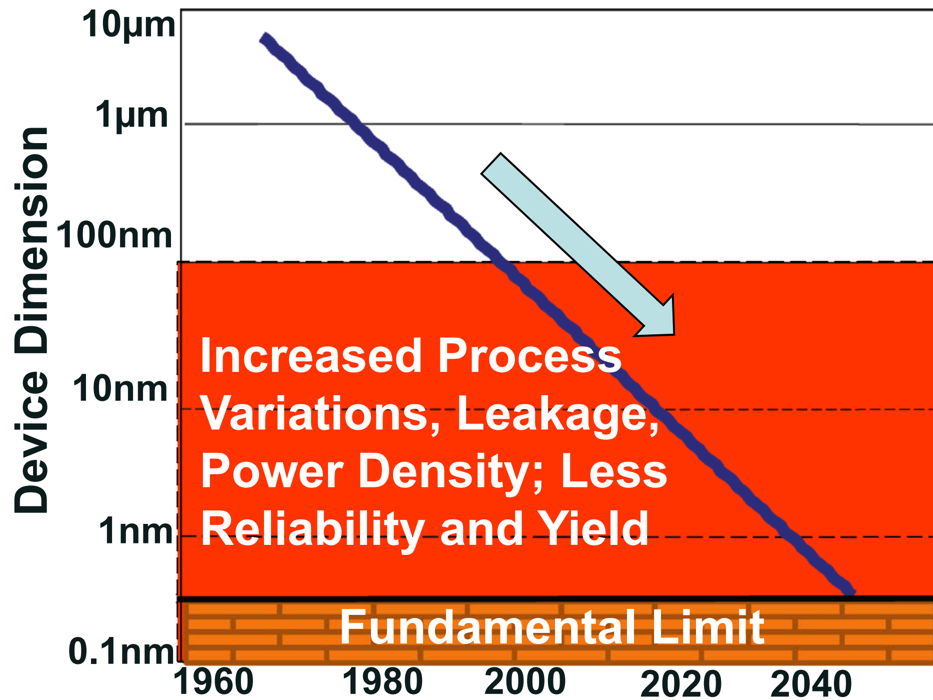
BEYOND CHARGE-BASED COMPUTING

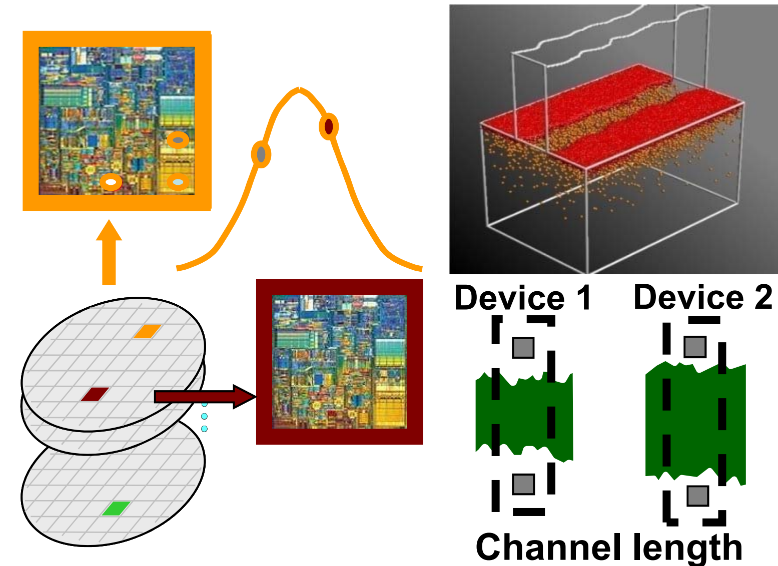
KAUSHIK ROY

MRIGANK SHARAD, DELIANG FAN, KARTHIK YOGENDRA, CHARLES AUGUSTINE, GEORGE PANAGOPOULOS, XUANYAO FONG

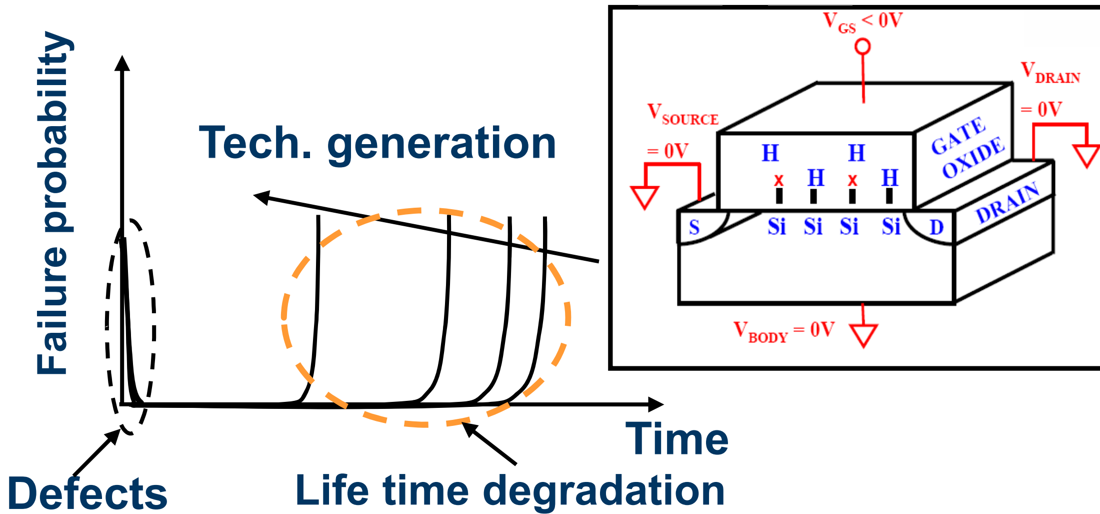
ELECTRICAL & COMPUTER ENGINEERING
PURDUE UNIVERSITY
WEST LAFAYETTE, IN 47906, USA

Why "Beyond Charge based Computing"?

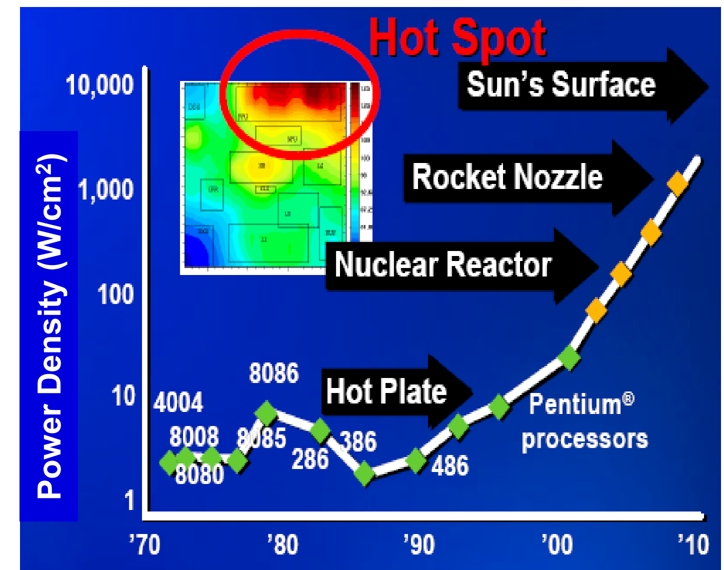




Process Variations



Reliability



Power Density

Why Beyond Charge Based Computing?

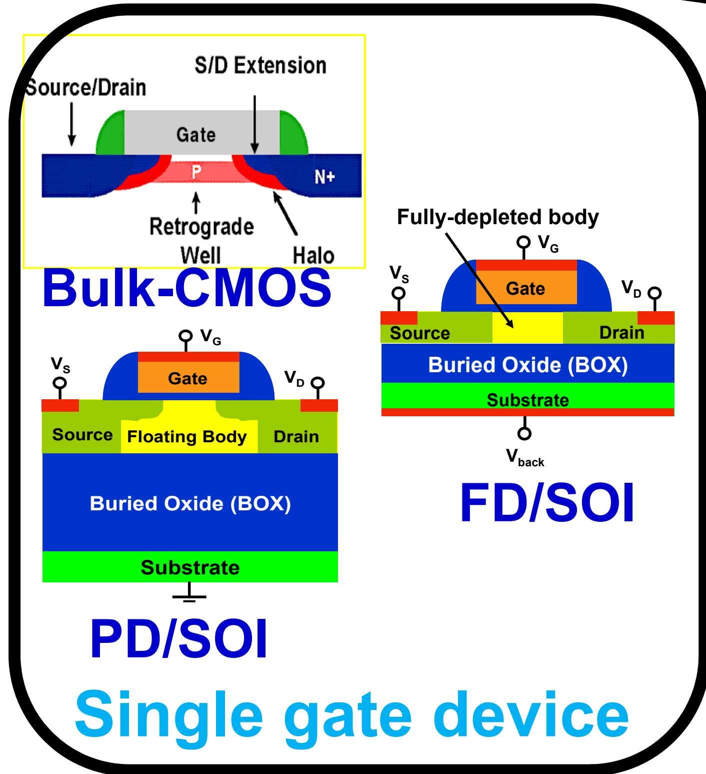
- Traditional computing models (Boolean logic, von Neumann architectures) are highly inefficient at performing tasks that humans routinely perform, such as visual recognition, semantic analysis, and reasoning.

- Bio-inspired computation can outperform Von-Neumann designs in many such data processing applications if the computing model matches device architecture and the devices operated at very low voltage

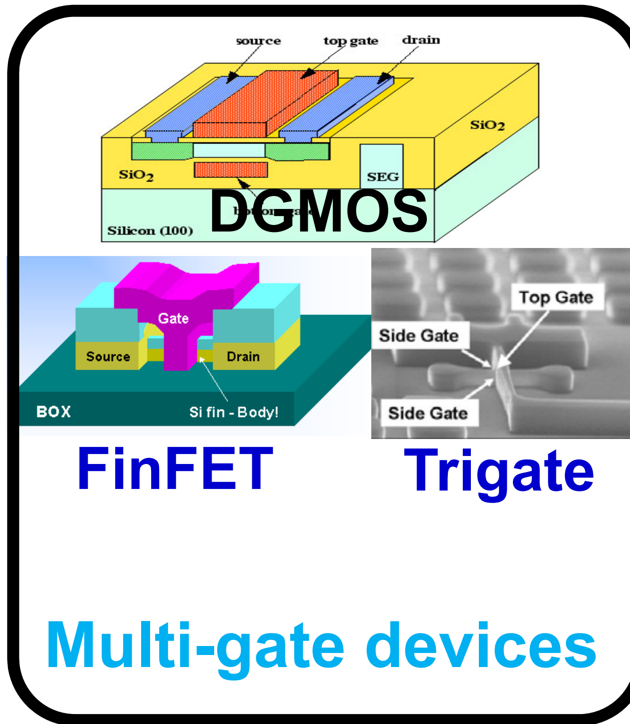
Technology Trend

More Moore

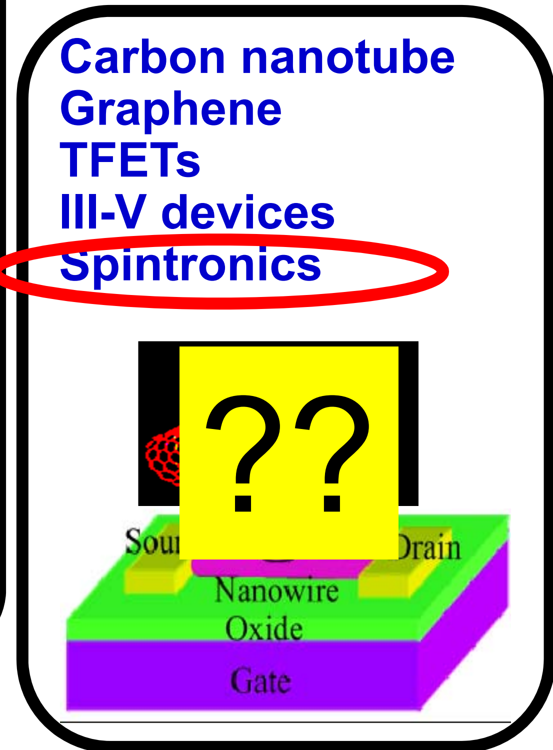
Beyond CMOS



Single gate device

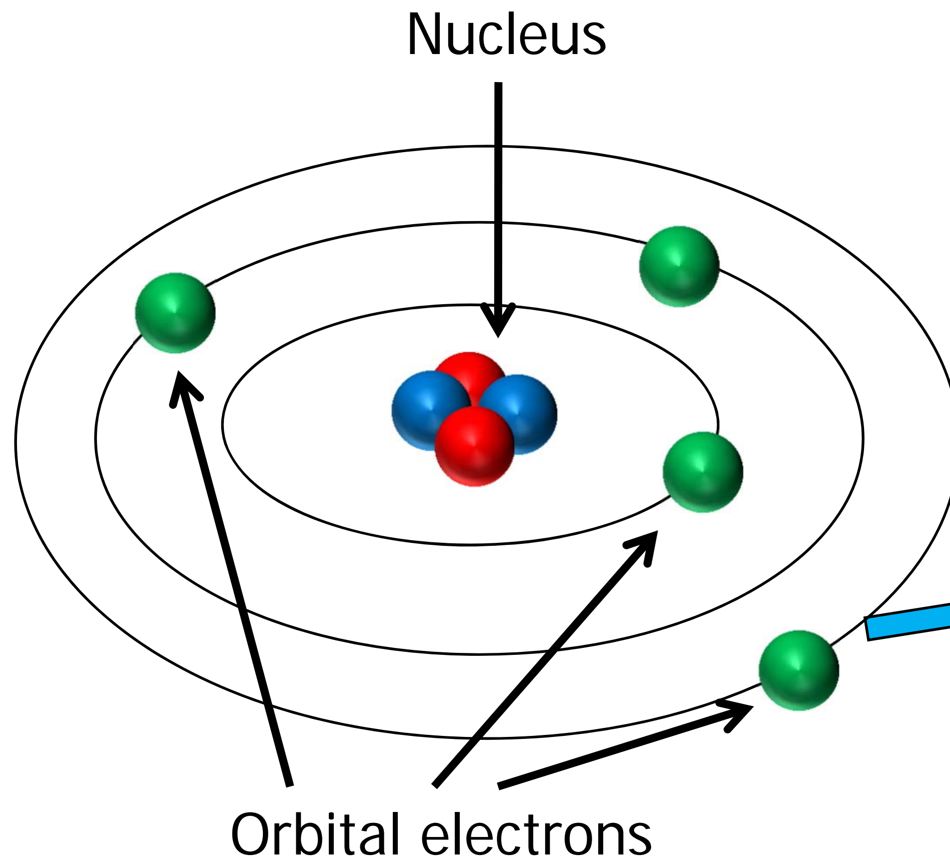


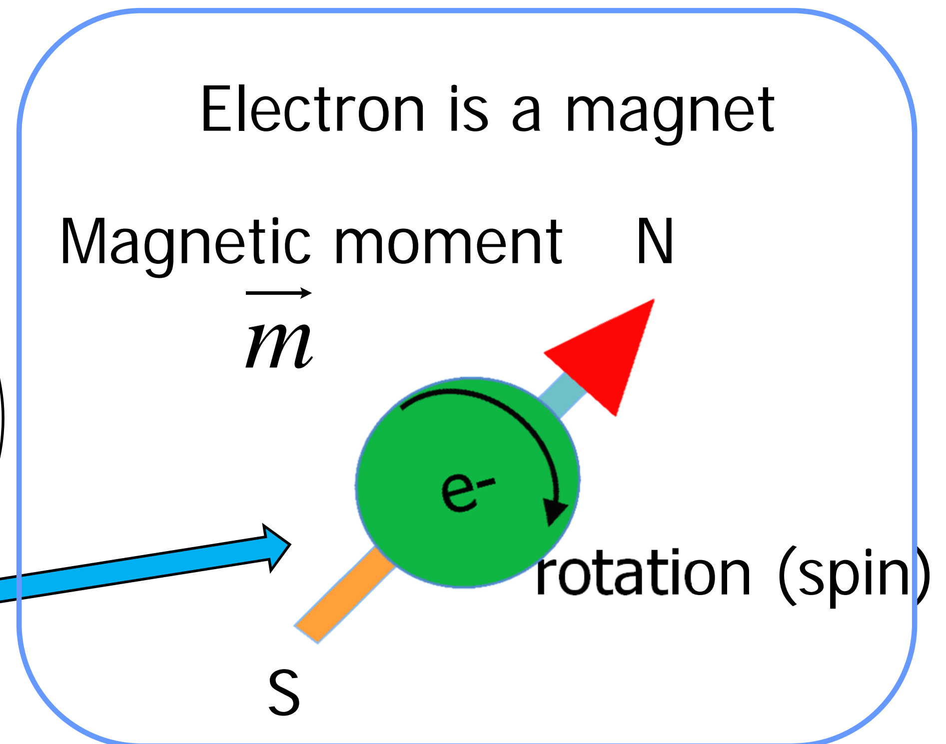
Multi-gate devices



Design methods to exploit the advantages of technology innovations

Electron SPIN



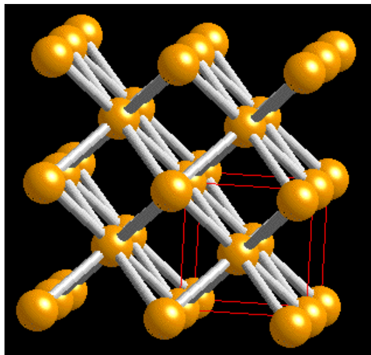


Classical representation of atom

Electrons with uni-directional electron spin moments results in magnet with non-zero moment (ferro-magnets)

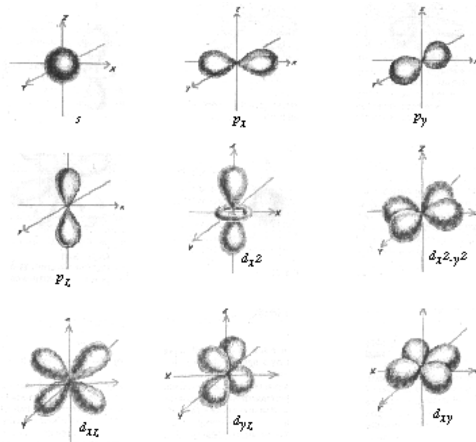
Fe (4), Co (3) and Ni (2) : unpaired electrons per atom

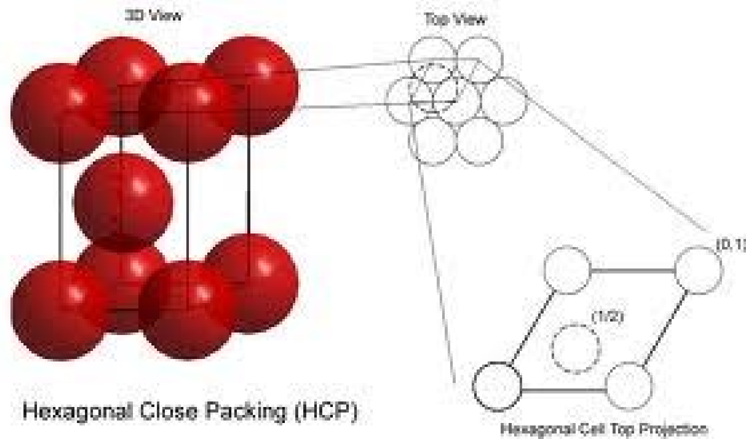
Sources of Magnetic Moments in Ferromagnetic Materials



Iron Lattice Structure (body central cubic)

Direction Characteristics in s-, p- and d- orbital's



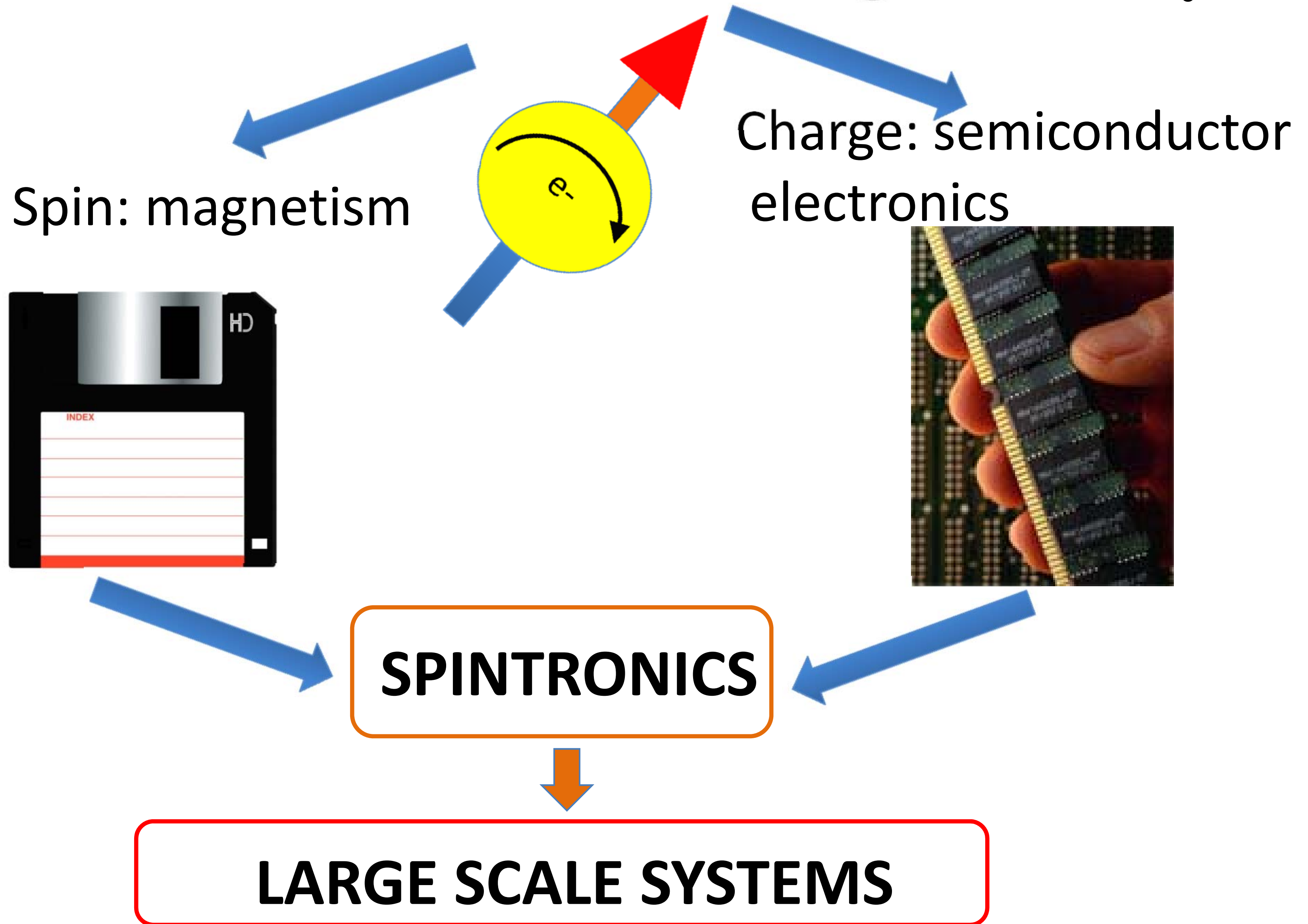


Cobalt Lattice Structure (Hexagonal Close Pack)

Ions	Spin direction of 3*d* orbitals					# electrons	Mag. Moment
Ti3+ , V4+	↑					1	1 mB
Ti2+ , V3+	↑	↑				2	2 mB
V2+, Cr3+, Mn4+	↑	↑	↑			3	3 mB
Cr2+ , Mn3+	↑	↑	↑	↑		4	4 mB
Mn2+, Fe3+	↑	↑	↑	↑	↑	5	5 mB
Fe2+, Co3+	↑↓	↑	↑	↑	↑	6	4 mB
Co2+	↑↓	↑↓	↑	↑	↑	7	3 mB
Ni2+	↑↓	↑↓	↑↓	↑	↑	8	2 mB
Cu2+	↑↓	↑↓	↑↓	↑↓	↑	9	1 mB
Zn2+, Cu+	↑↓	↑↓	↑↓	↑↓	↑↓	10	0 mB

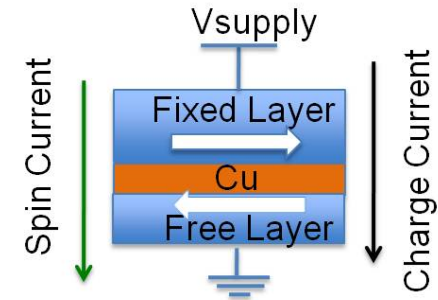
Incomplete 3d orbitals is the principle source of magnetic moments in transition metals

State Variable: Charge & Spin

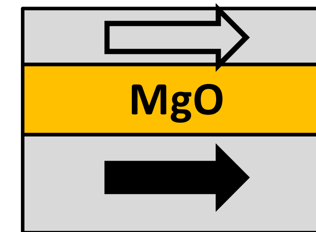


Recent Inventions

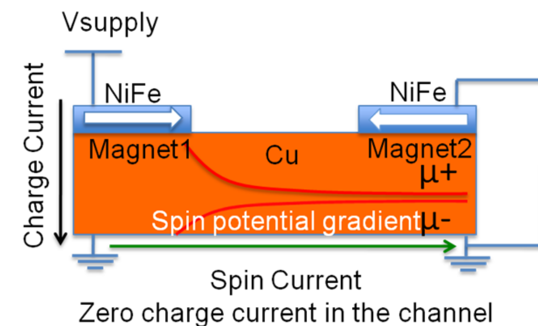
Giant Magneto Resistance (GMR)
1988: Peter Grunberg, Germany
Albert Fert, France
2007: Nobel Prize



Spin Transfer Switching (STS)
1996: Slonczewski, US



Lateral Spin Valves
(Local & Non-Local)
2008: Yang, Kimura, Otani
2009: Sun

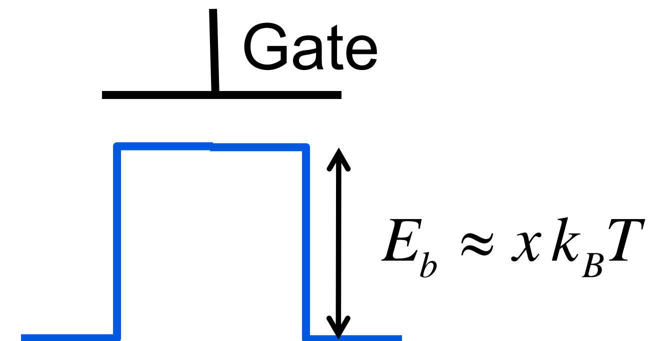


Memories: high density, stability, low read/write current, access time, zero leakage..
Logic (Boolean & Non-Boolean): Ultra low voltage switch, Neuromorphic computing, (all-spin logic – no spin-charge conversion), i/p o/p isolation, zero leakage,
Interconnects: Spin channel (short), Ultra low voltage swing for charge based int.

MOS vs. Magnets Switching Energy

MOS

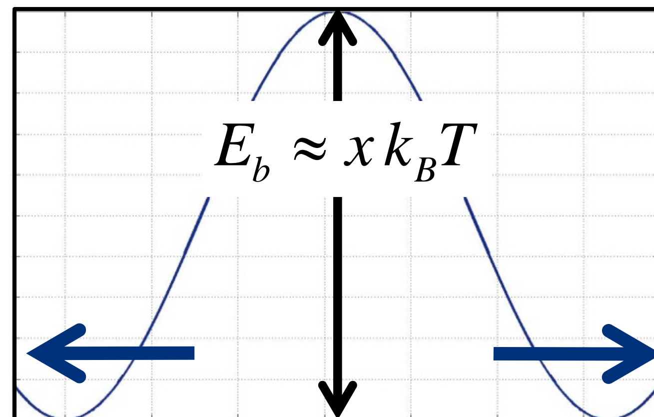
- Dissipated Energy= $0.5CV^2$ ≈ N*Eb
- N ≈10,000 , x=40   1e-15 J / switch



Magnet ("Collective Entity")

- Dissipated Energy ≈ Eb
- equivalent N =1

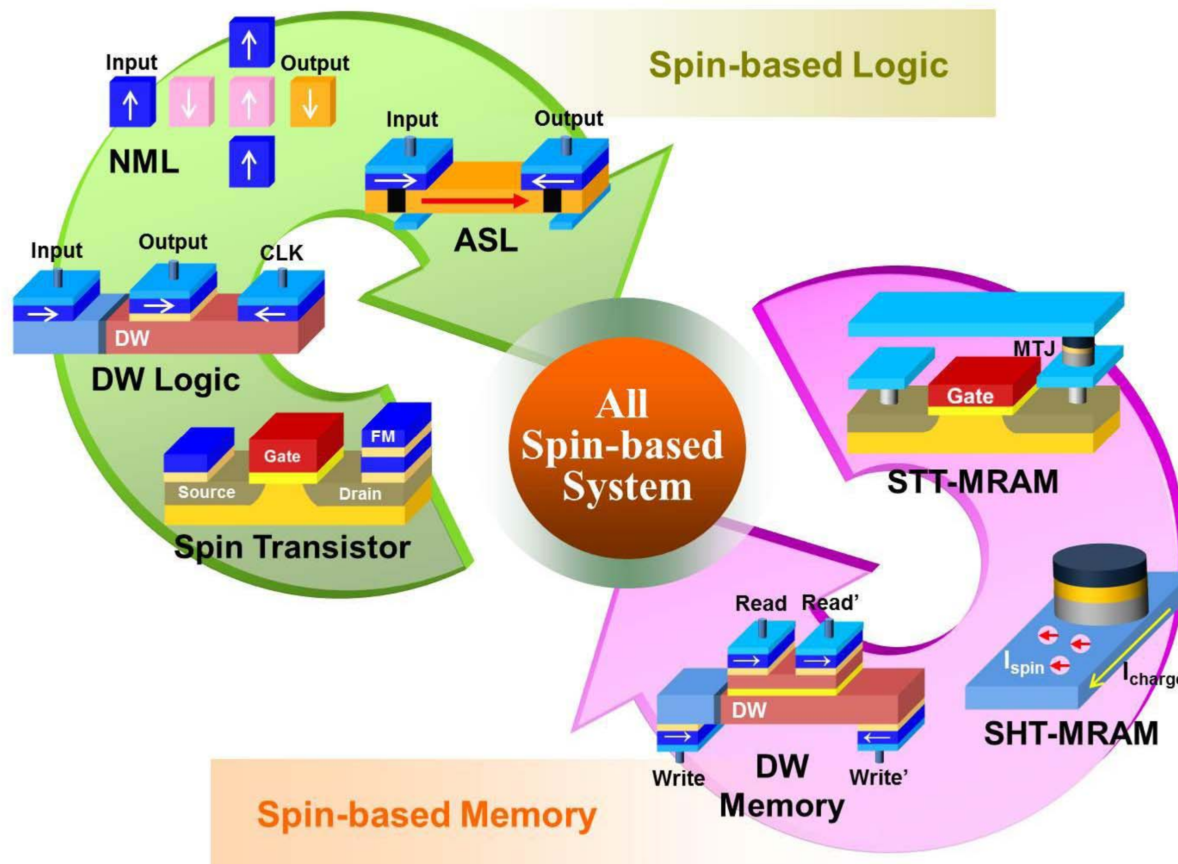
x=40 → 1e-19 J / switch
Life-time = 7 years



Non-volatile

Theoretical switching energy of magnet is 0.1aJ << 1fJ (MOSFET)

All-Spin Based Systems



Energy Barrier Modulation: MOSFETs vs. Magnets

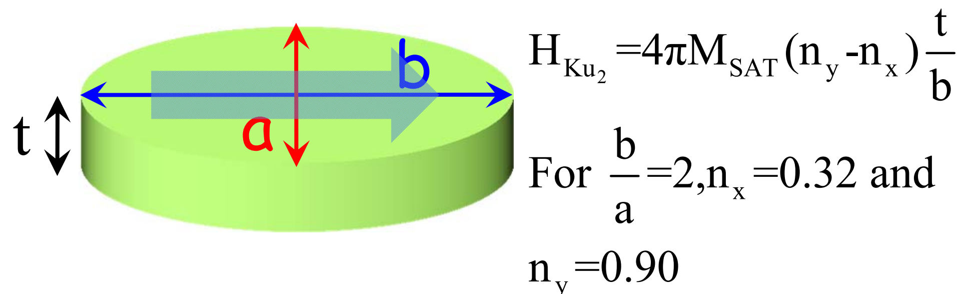
Conventional Charge-based MOSFET (Bulk/SOI/FinFETS)

- The energy barrier in the active channel region can be modulated using:
  - **Doping**
    - Uniform Channel Doping
    - Symmetric/Asymmetric Halo Doping
    - Source Drain Doping
  - **Work Function and Material Engineering**
  - **Gate Dielectric and Thickness (T_{OX}) Modulation**

Nano-Magnets with Electron Spin as State Variable

- The energy barrier in magnets is defined as the product of anisotropy and volume ($E_B = K_{u2}.V$)

- The energy barrier in magnets can be modulated using:
  - Shape and Interfacial magnetic Anisotropy (K_{u2})
  - Volume of the nano-magnet (thickness (t) and cross-sectional area (A))
  - Saturation Magnetization (M_{SAT})

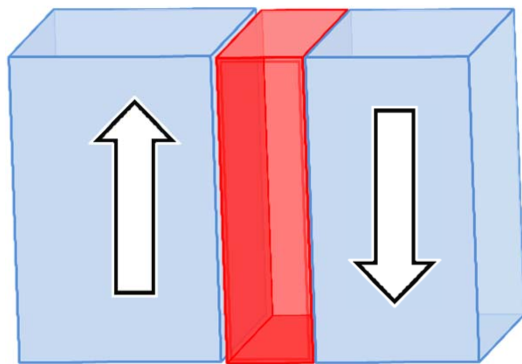


Changing the State of a Magnet

- External Magnetic Field
  - » Current carrying wires, coils, etc.
  - » Dipolar coupling
  - » ..
- Current Induced Spin-Transfer Torque (1996)

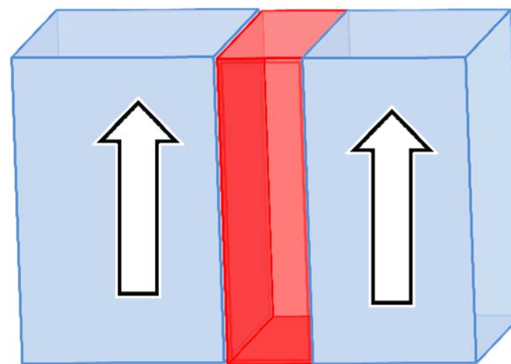
Magnetic Tunneling Junctions (MTJ) Basics: Read Operation

Anti-parallel orientation of magnets (AP)



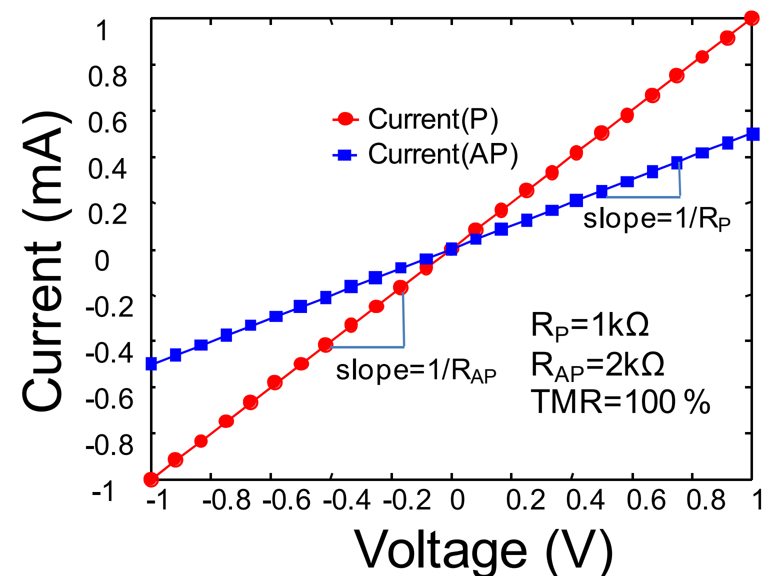
High resistance state (R_{AP})

Parallel orientation of magnets (P)



Low resistance state (R_P)

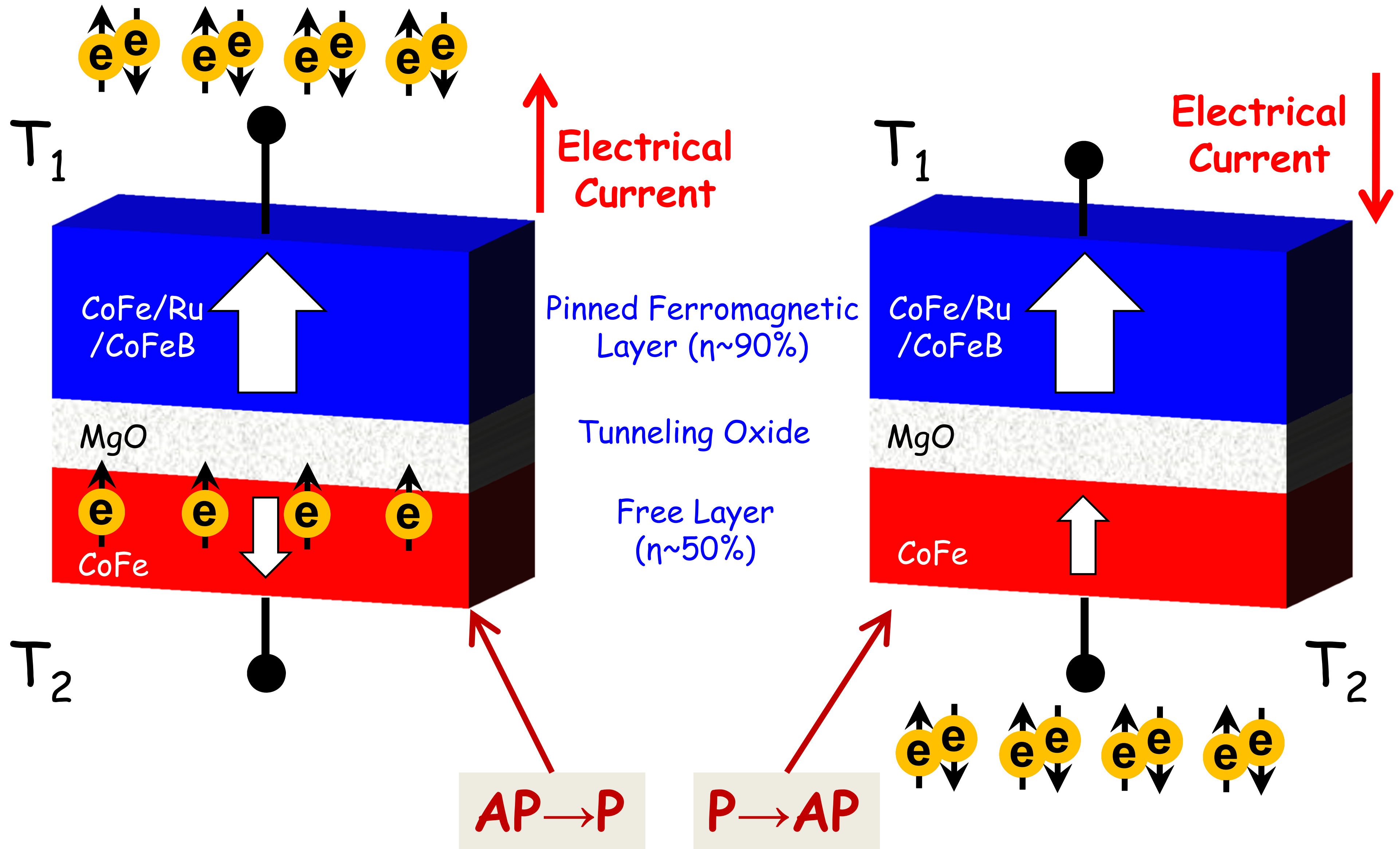
Electrical Characteristics of MTJ



$$\text{TMR}=\left(\frac{R_{AP}-R_P}{R_P}\right)100\ \%$$

Memory state is detected through difference in resistance using Sense Amplifier

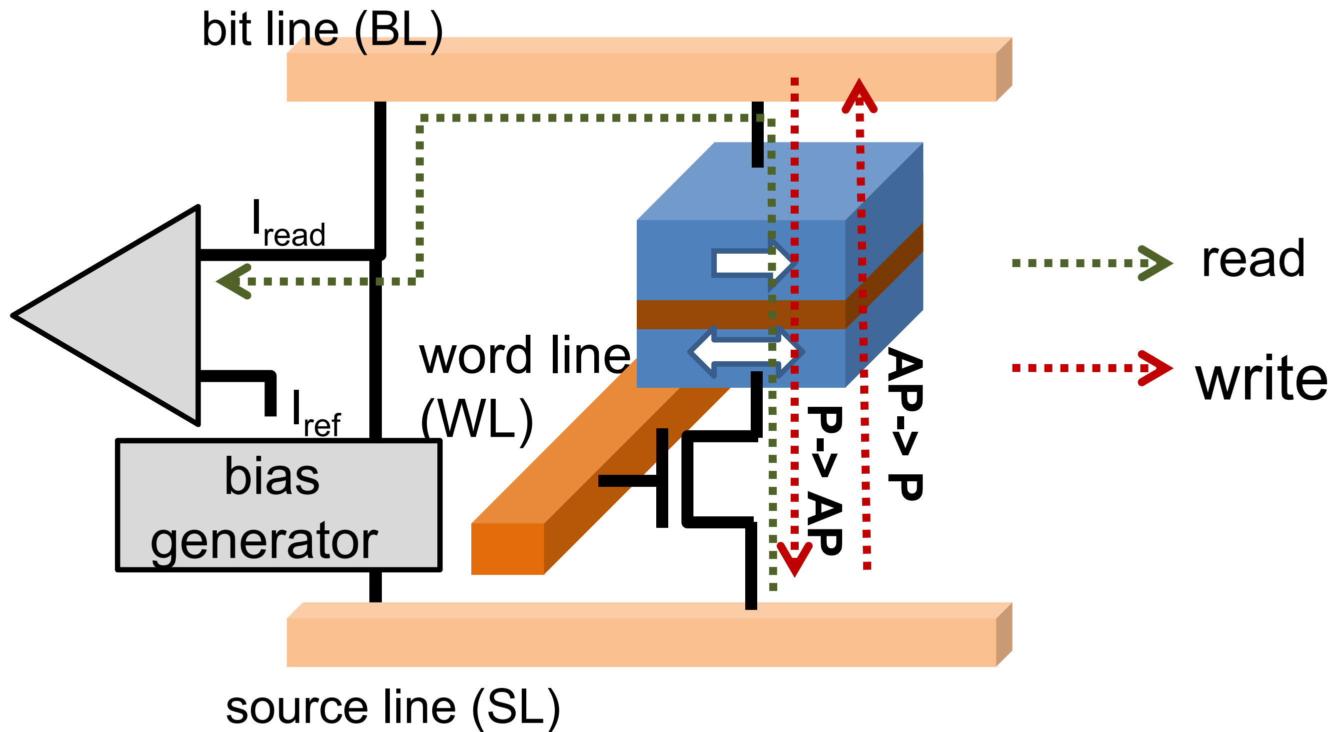
MTJ Basics: Spin-transfer torque induced write operation



P→AP magnetization switching is relatively difficult than AP→P due to lower spin injection efficiency of the free layer

Bit-Cell Design using STT-MTJ

1-T, 1 R STT-MRAM



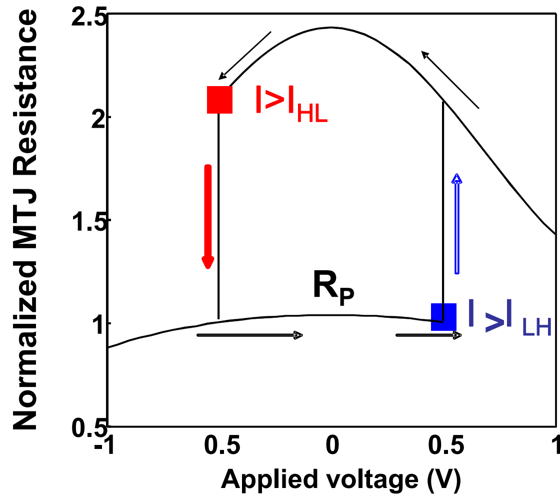
Key Advantages:

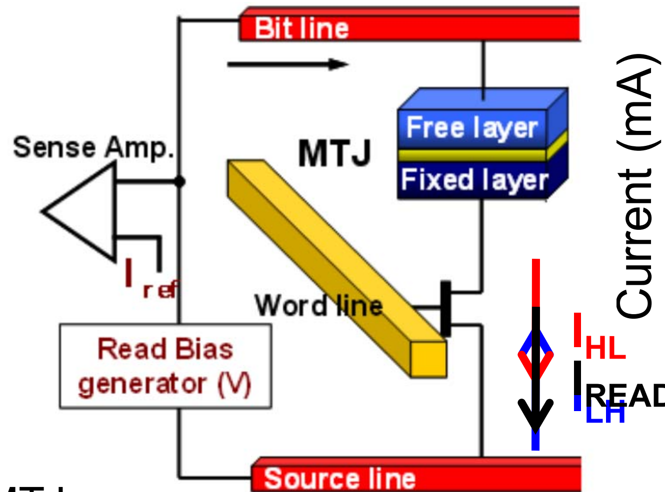
- **High Density (just 1 transistor per bit cell)**
- **Non-Volatility**
- **No leakage power in un-accessed cells**

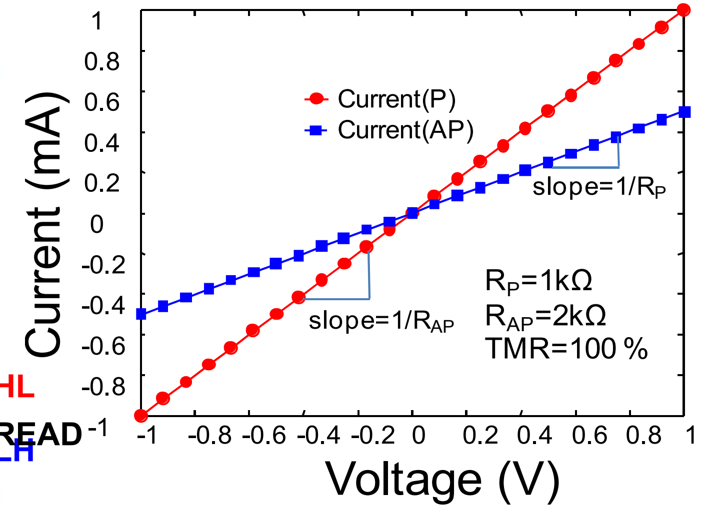
Limitations

- Write asymmetry
- Reliability-limited write speed
- Read-Write optimization conflict

Design Challenge 1: Read and Write Failures in 1T-1R Bit-cell Structures





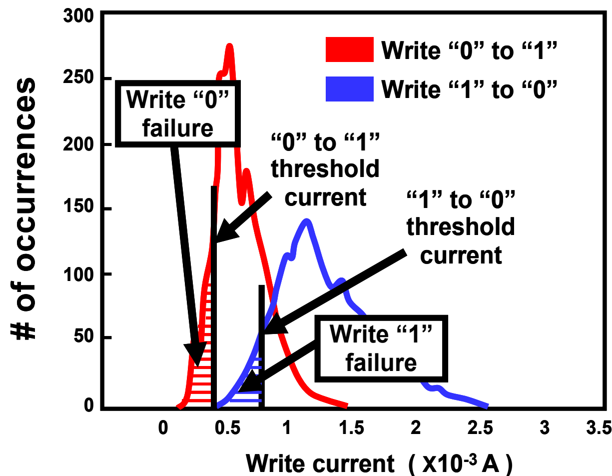


Write Failure

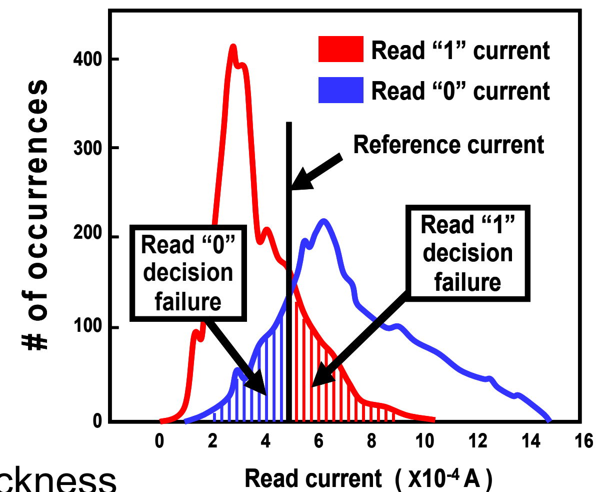
Insufficient current to switch MTJ

$I_{WRITE} < \min(I_{LH}, I_{HL})$

Insufficient TMR to distinguish between R_{AP} and R_P

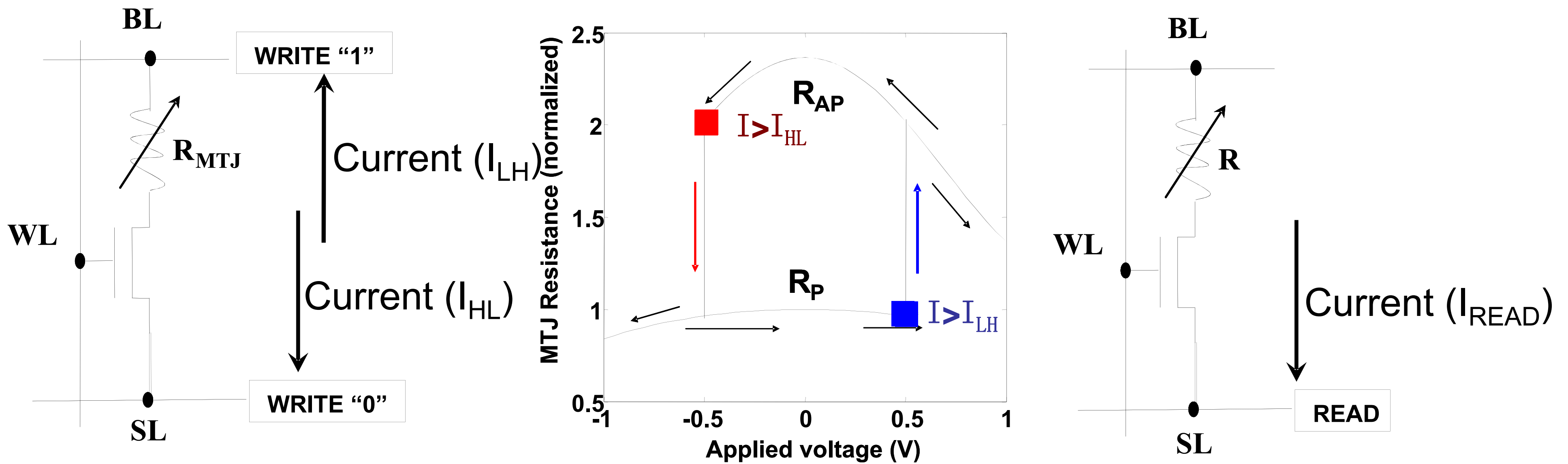


Process variations reduce memory yield

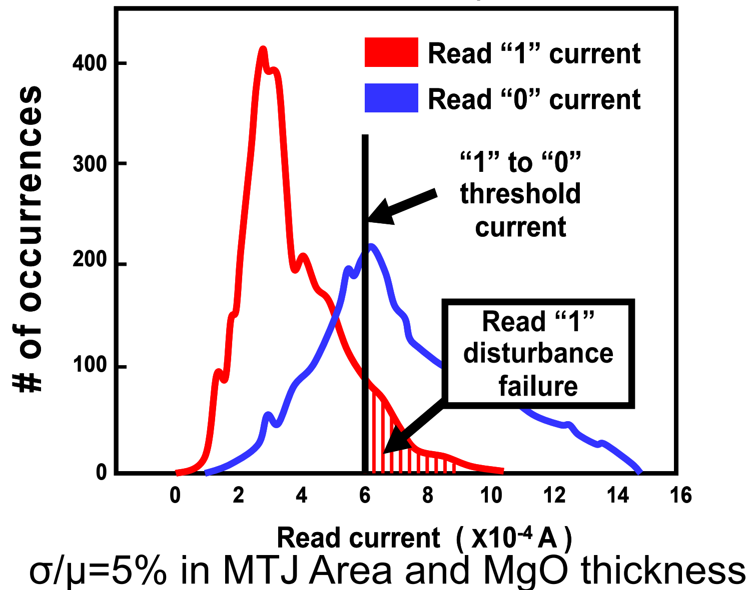


σ/μ=5% in MTJ Area and MgO thickness

Design Challenge 2: Read-Write Conflict



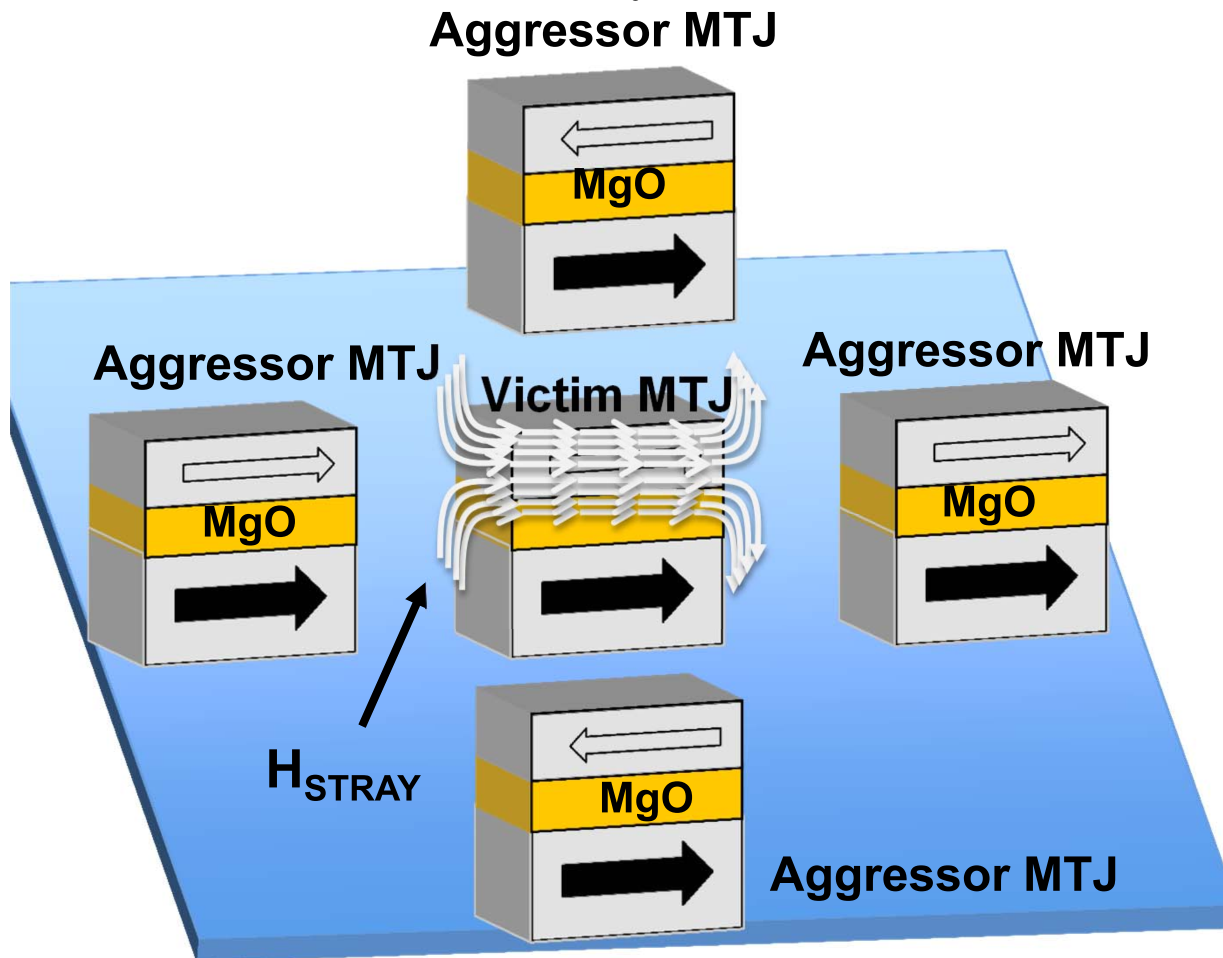
Read Disturb Failure (under process variations)



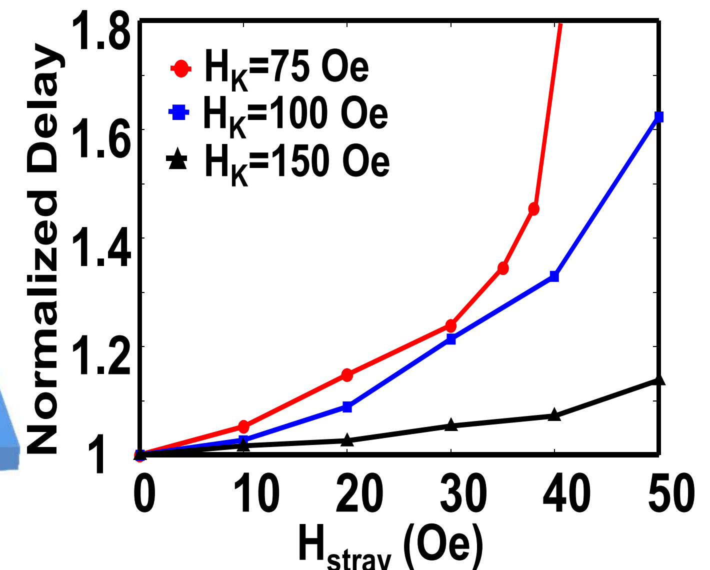
σ/μ=5% in MTJ Area and MgO thickness

- I_{READ} and I_{HL} have same polarity
- Read operation can cause unintended write (**Read Disturb**)

Design Challenge3: Stray Fields and its Impacts on MTJ Stack



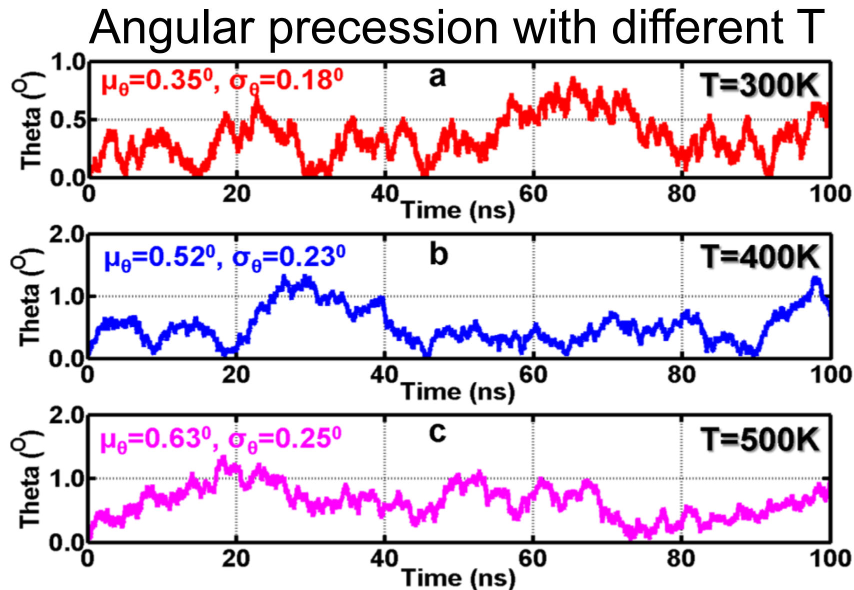
Free Layer
MgO
Fixed Layer

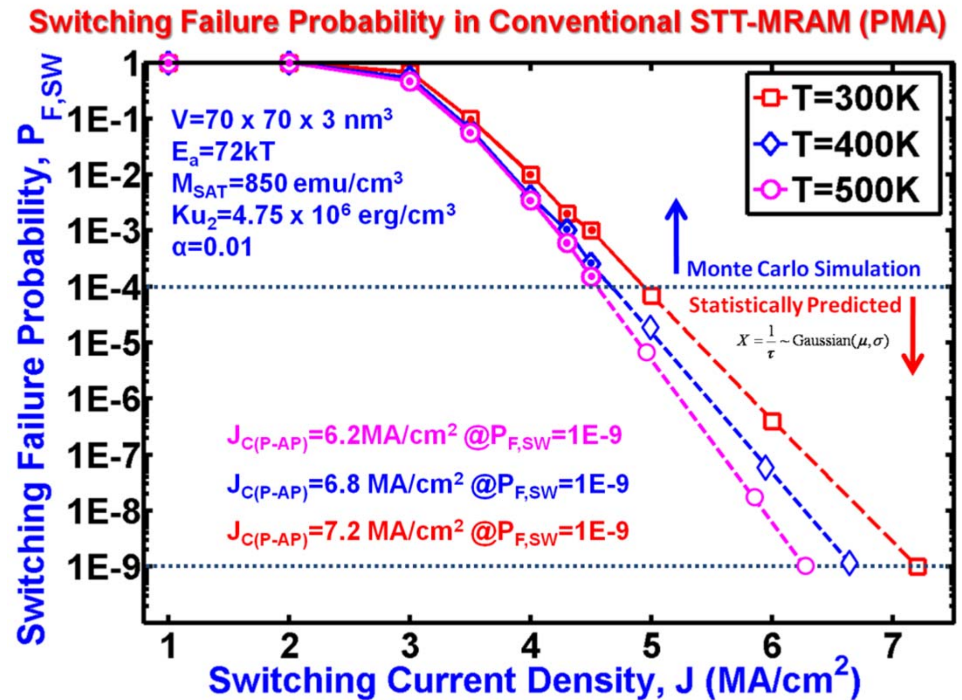


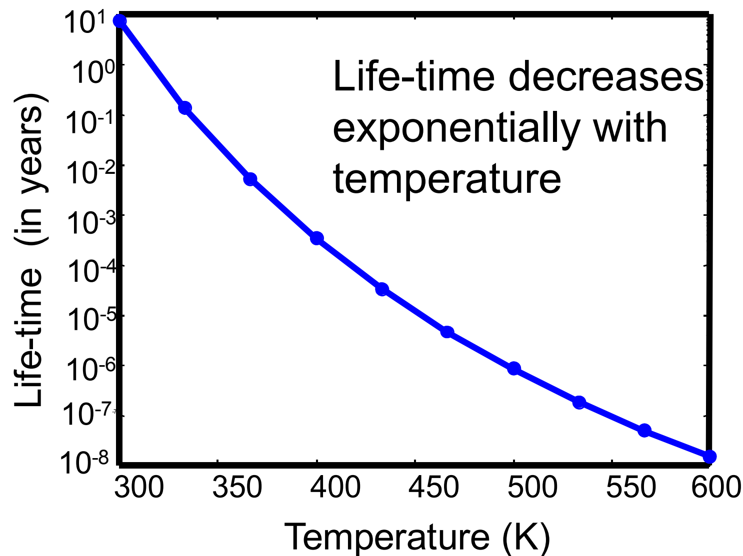
P to AP switching is opposed by stray magnetic field (H_{STRAY})

WRITE time increases for higher stray fields → write failures

Design Challenge 4: Stochastic Switching Behavior due to Thermal Fluctuations



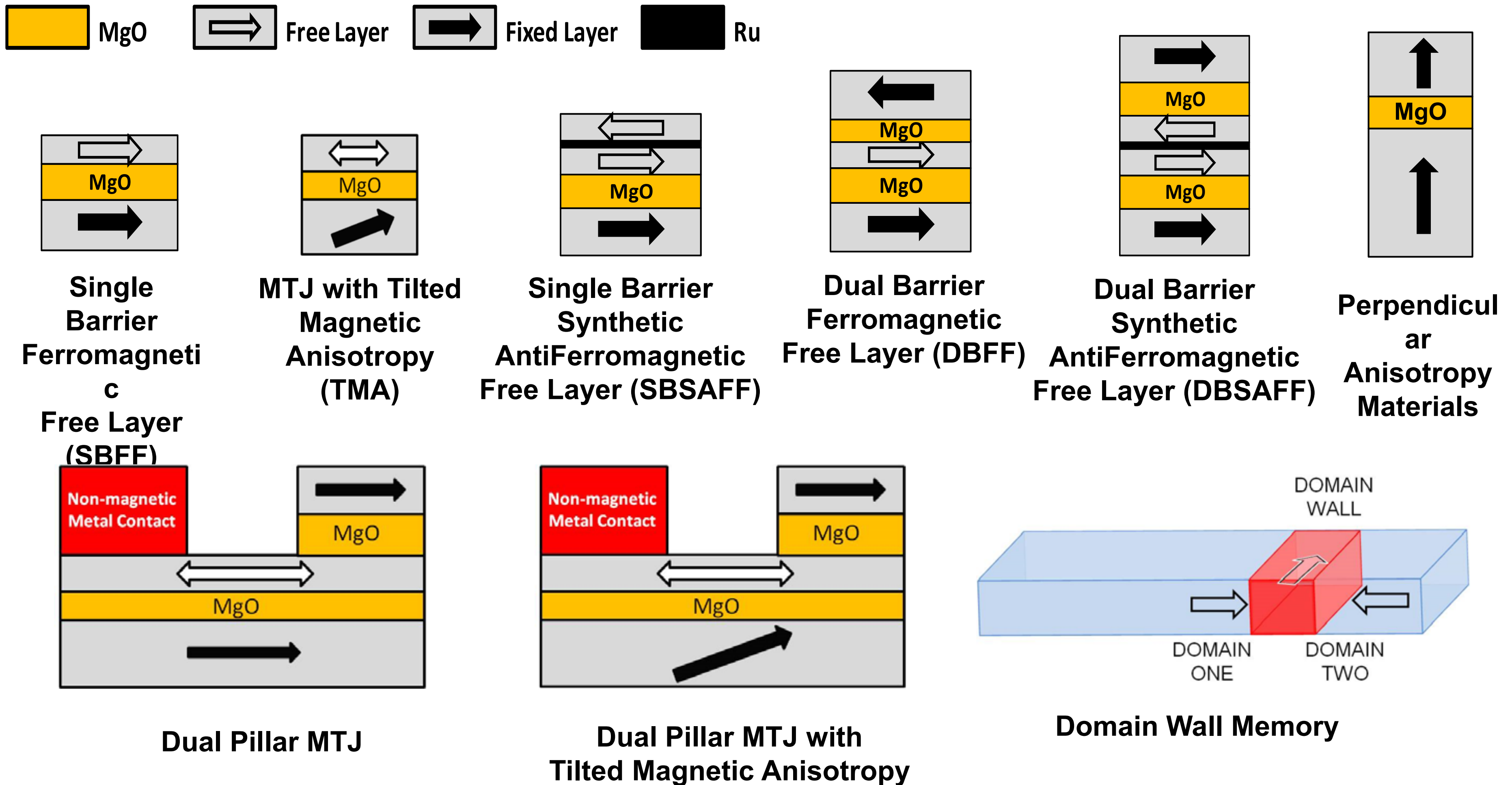




- Thermally induced initial magnetic oscillations are stochastic in nature (white noise)
- STT switching delay distribution has a longer tail, degrading memory yield
- Higher temperature helps in squeezing the switching delay distribution but degrades thermal stability

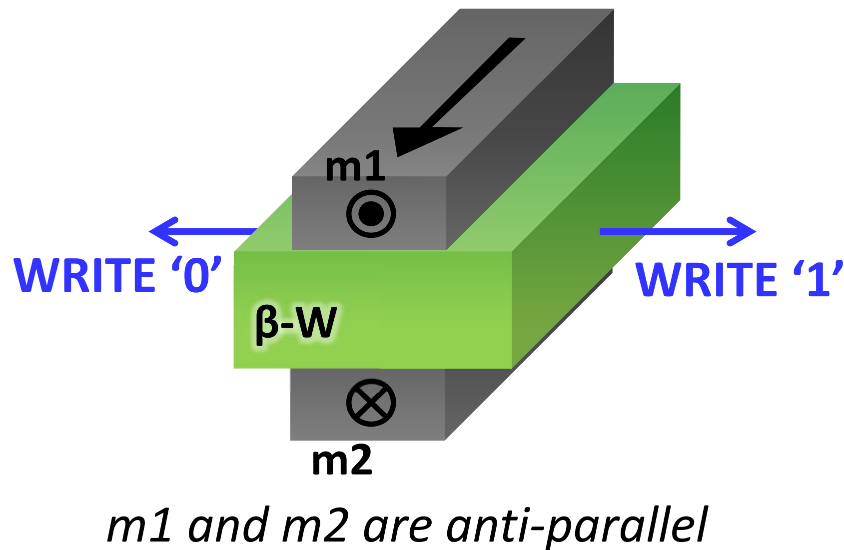
STT-MTJ Stacks: Stability, Read/Write Conflicts, Write power, ..

Alternative Device Structures

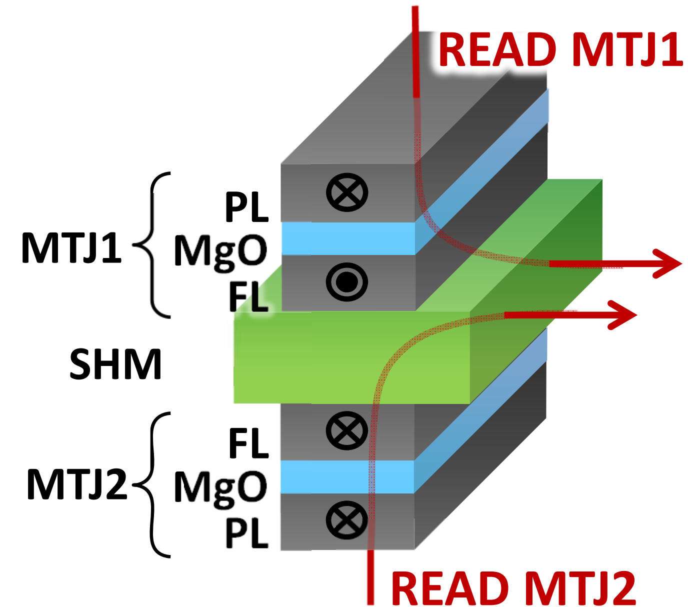


Alternative Device designs may alleviate some of the problems related to scaling

Differential Spin Hall MRAM



m1 and m2 are anti-parallel



Energy-efficient write

- Spin injection efficiency > 100 %
- Low resistance in write current path
- No tunneling barrier reliability

10X lower write energy compared to 1T1R STT-MRAM

High speed differential read

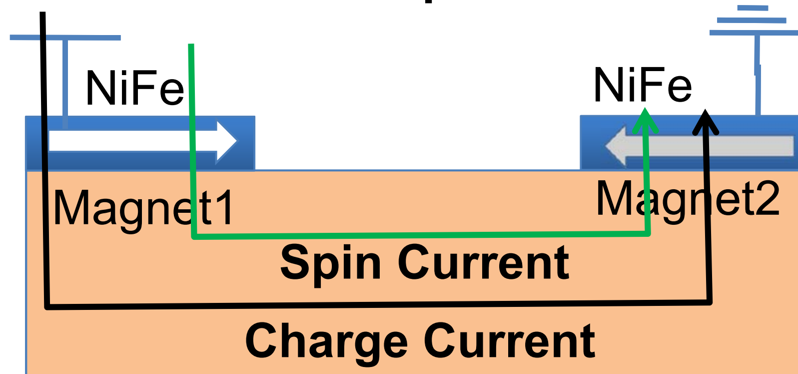
- No need for a reference cell
- 2X signal margin

1.6X faster read speed compared to single-ended reading

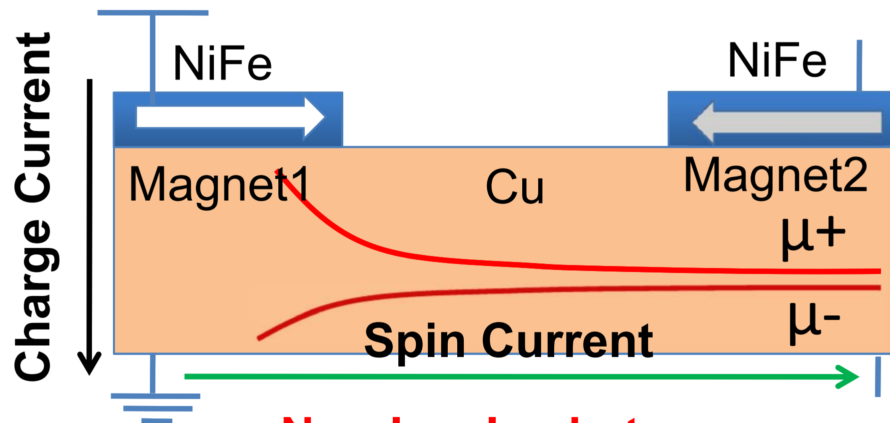
Y Kim, SH Choday, K Roy, EDL 2013

Spin Valves

Lateral Spin Valve

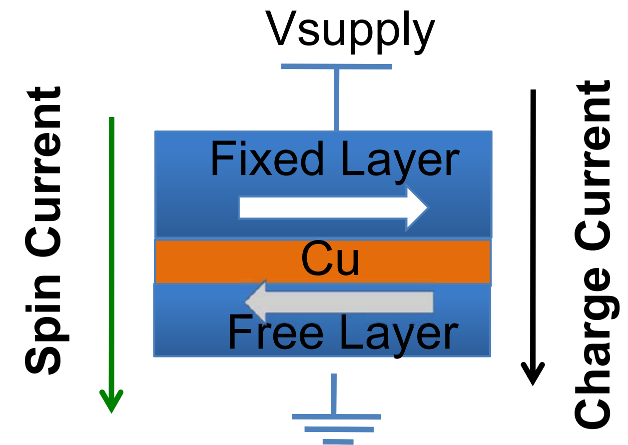


local spin torque



Non-local spin torque

Vertical spin valve structure
Local Spin torque



Free Layer switches under the influence of local spin torque

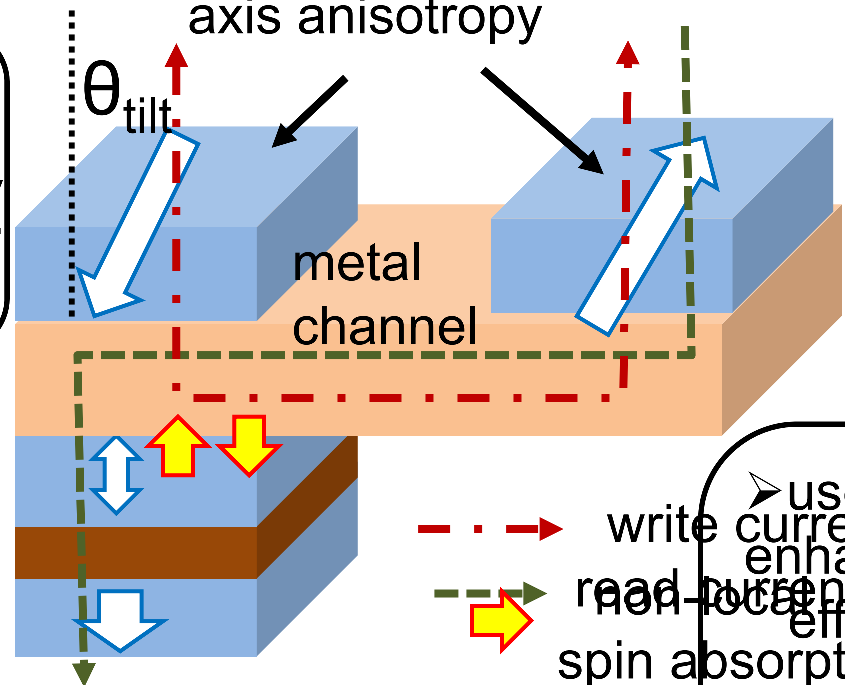
injection-efficiency is determined by interface polarization, can be ~90% for injector polarity ~ 0.9

Non-Local STT-MRAM (Separate R/W Paths)

device structure:

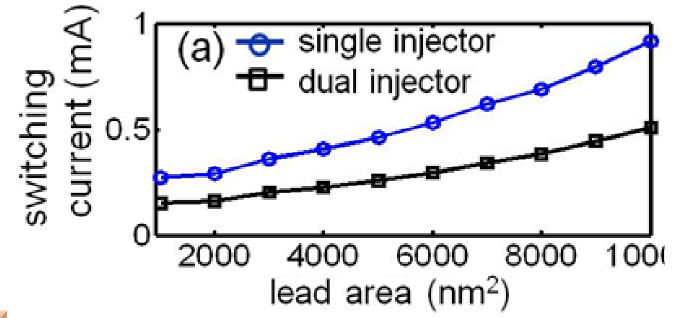
dual injectors with tilted axis anisotropy

compensate for low spin-injection efficiency for **non-local STT write ??**

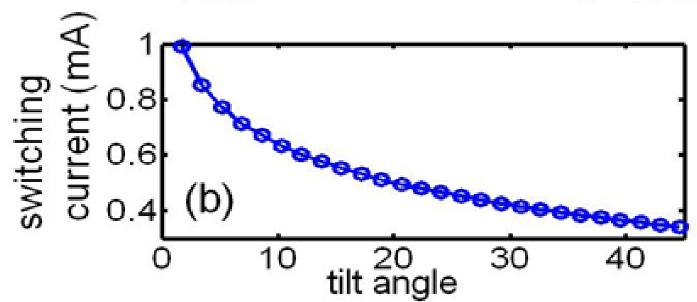


free layer →
MgO →
fixed layer →

write current
read current
non-local spin absorption

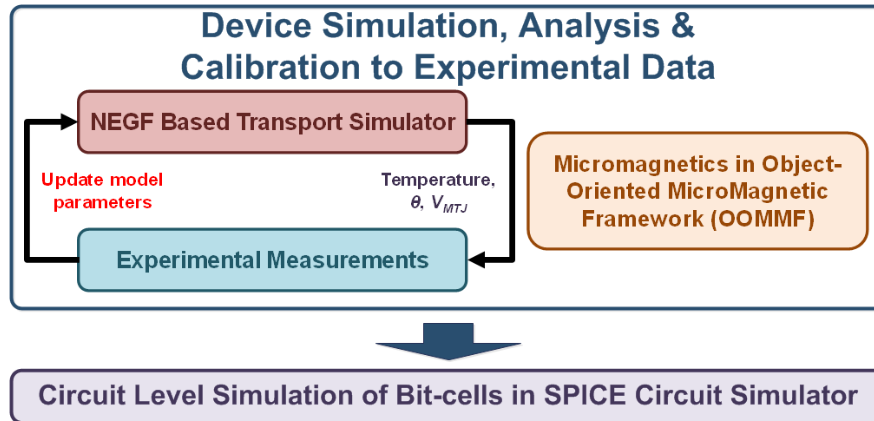


- use of **dual injector** enhances spin injection efficiency by ~2X
- tilted anisotropy for injectors further reduces the switching current by ~3X

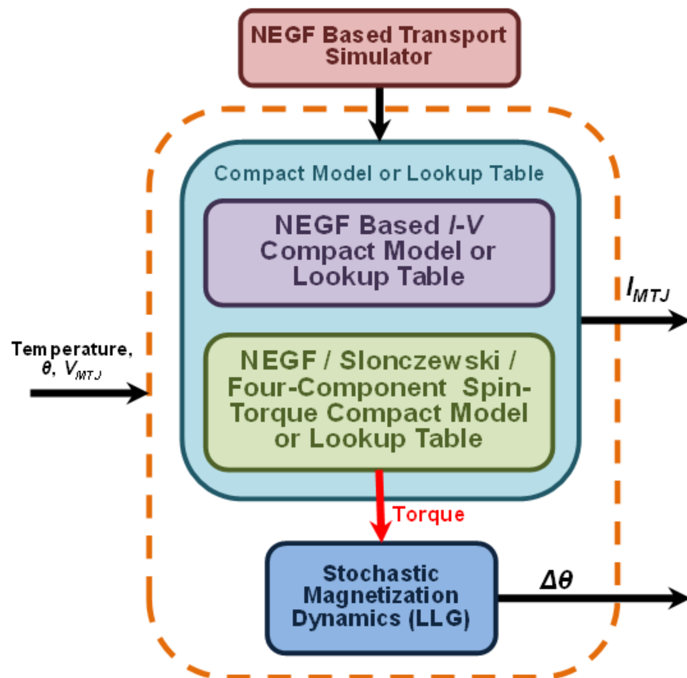


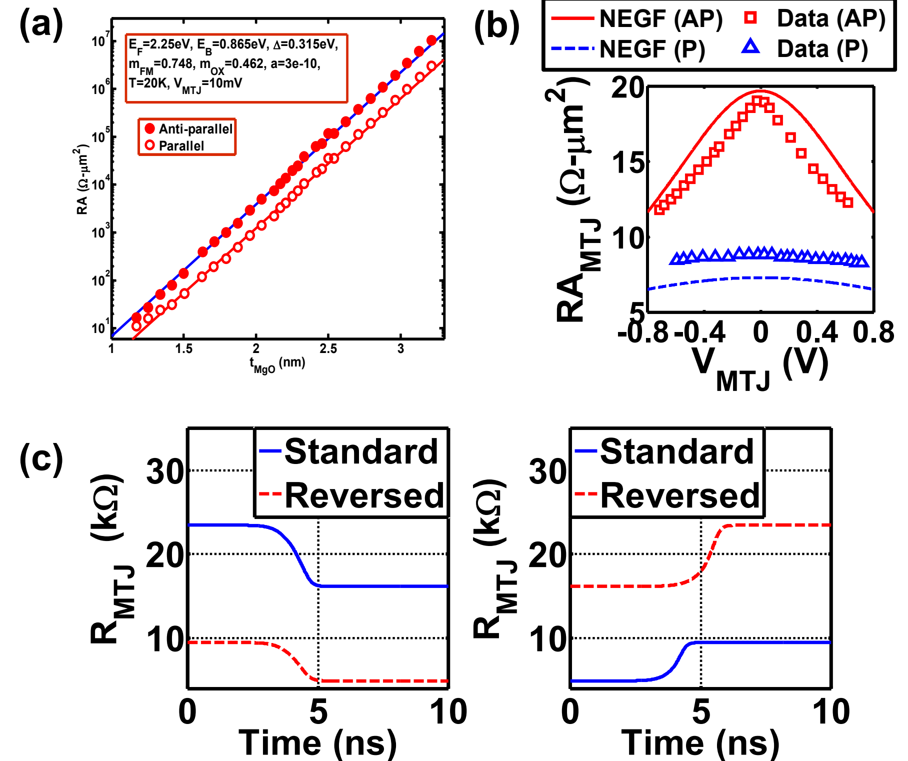
M. Sharad et al., DRC, 2012

Simulation Framework



SPICE MTJ Model





a) S. Yuasa *et al.*, *Nature Materials* vol. 3, no. 12, pp. 868-871, Dec. 2004.

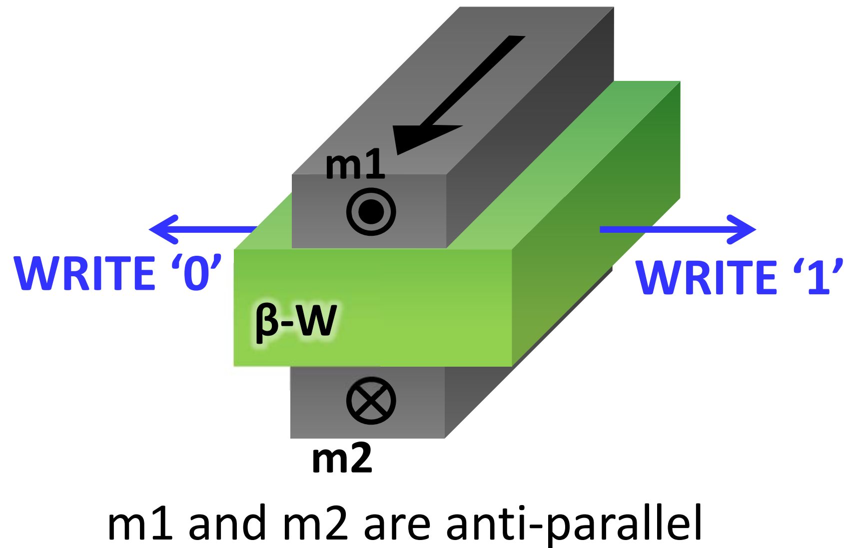
b) C. J. Lin *et al.*, *IEDM*, Dec. 2009, pp. 11.6.1-11.6.4.

c) T. Kishi *et al.*, *IEDM*, Dec. 2008, pp. 12.6.1-12.6.4.

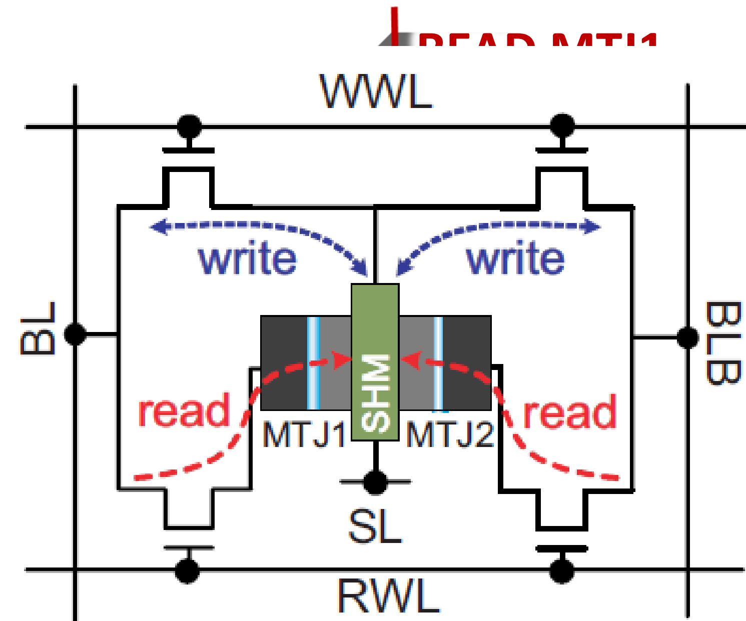
- **Device level simulation results may be calibrated to experimental data**
- **Device parameters are imported into SPICE model for circuit level simulations**

Differential Spin Hall MRAM
(Roy)

Y Kim, SH Choday, K Roy, EDL 2013



m1 and m2 are anti-parallel



Energy-efficient write:

- Spin injection efficiency > 100%.
- Low-resistance in write current path.
- No tunneling barrier reliability issue.

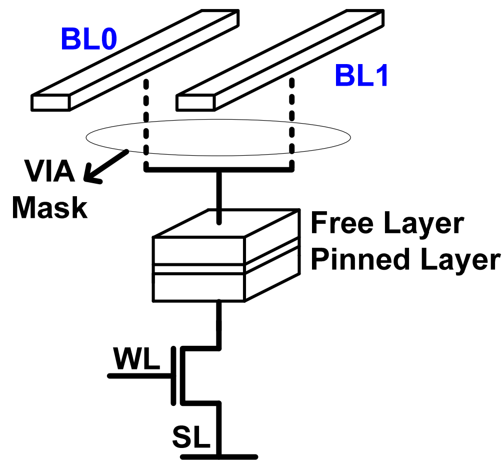
- **10X lower write energy compared to 1T1R STT-MRAM**

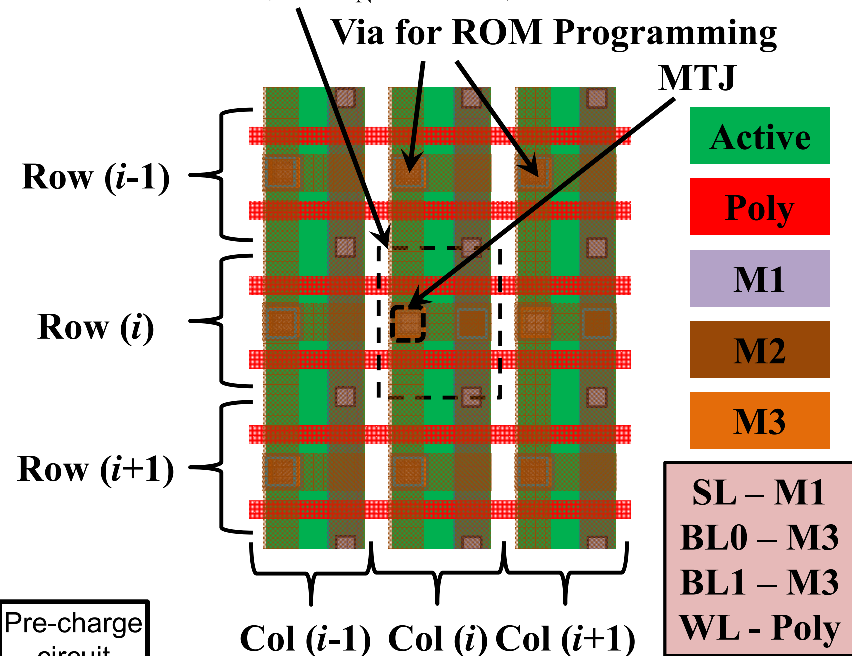
High-speed differential read:

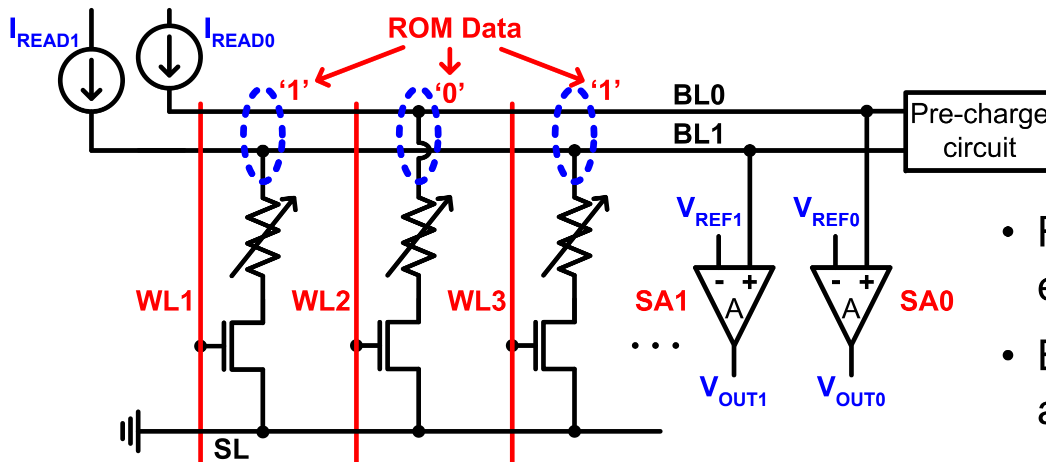
- No need for a reference cell.
- 2X signal margin.

- **1.6X faster read speed compared to single-ended reading**

Read-Only Memory-Embedded MRAM (Roy)





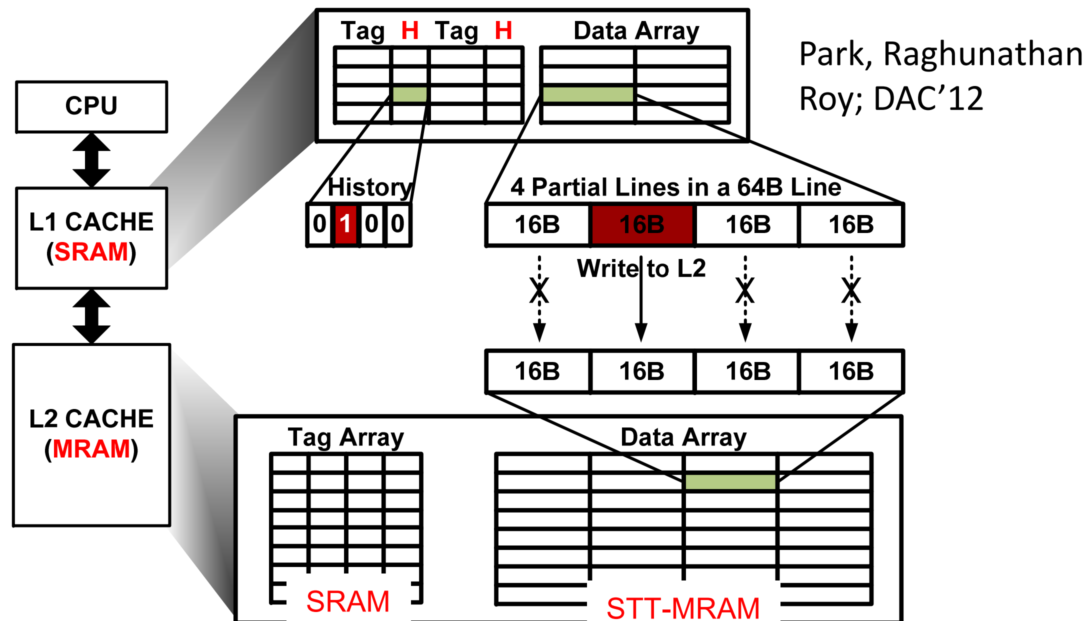


Lee, Fong, Roy, "Rom-Embedded MRAM", EDL 2013

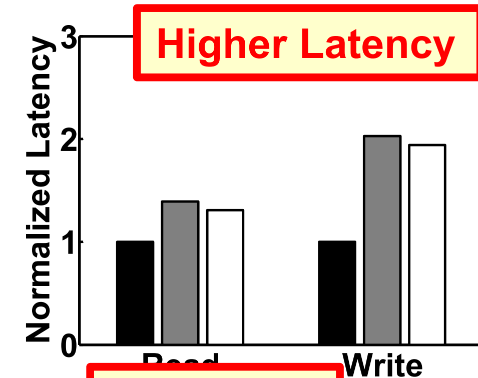
- Read-Only Memory (ROM) may be embedded with little area overhead.
- Embedded ROM can be used to accelerate function evaluations (e.g.math.)
- No performance penalty to Random Access Memory (RAM) mode.

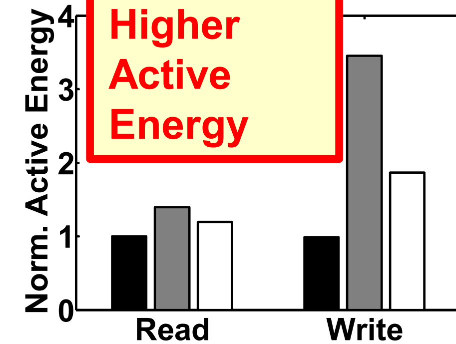
STT-MRAM: Last Level Cache (Roy)

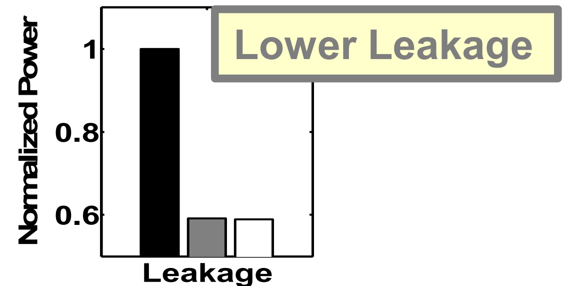
- Drop-in replacement of SRAM with STT-MRAM for LLC leads to improvement in capacity and leakage, but higher latency and active energy.



Park, Raghunathan Roy; DAC'12





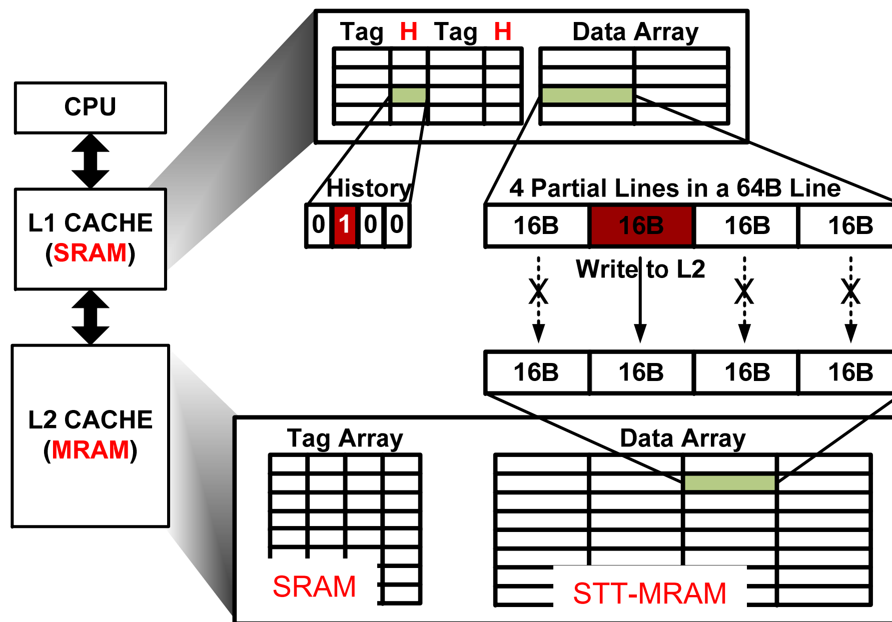


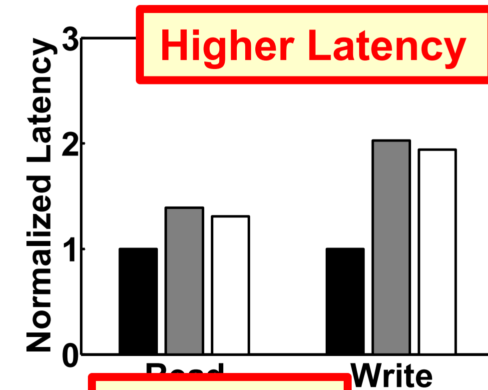
2MB 6T SRAM
8MB STT MRAM
8MB STT MRAM (Tilted Magnetic Anisotropy)

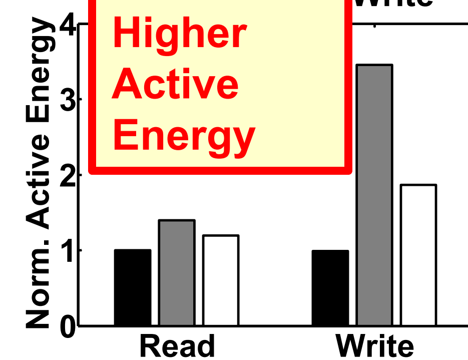
- **Circuit and architectural techniques can greatly improve the efficiency of spin-based caches.**

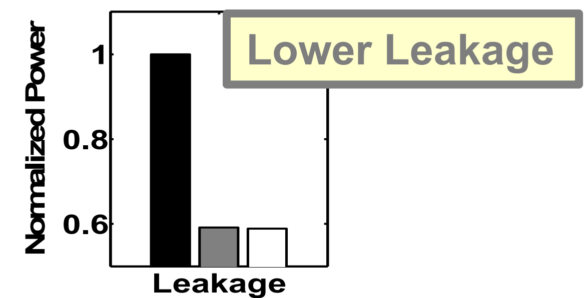
STT-MRAM: Last Level Cache

- Drop-in replacement of SRAM with STT-MRAM for LLC leads to improvement in capacity and leakage, but higher latency and active energy
- Circuit and architectural techniques can greatly improve the efficiency of spin-based caches









2MB 6T SRAM

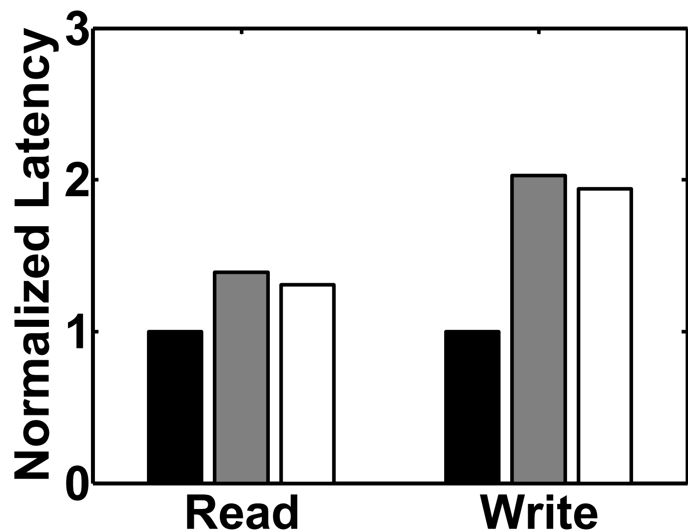
8MB STT MRAM

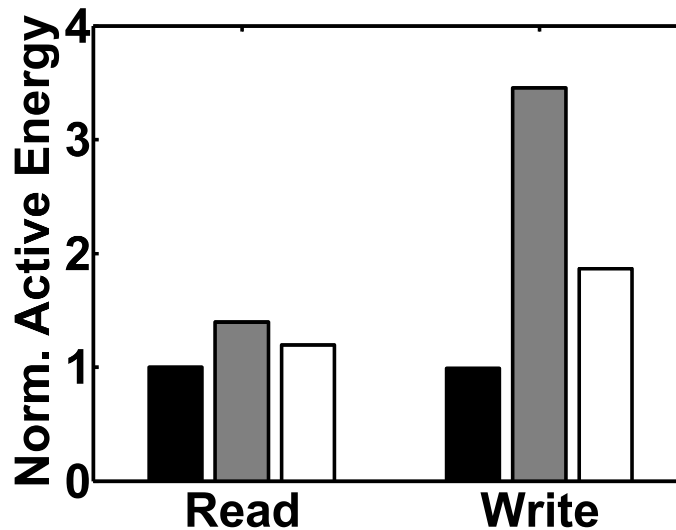
8MB STT MRAM (Tilted Magnetic Anisotropy)

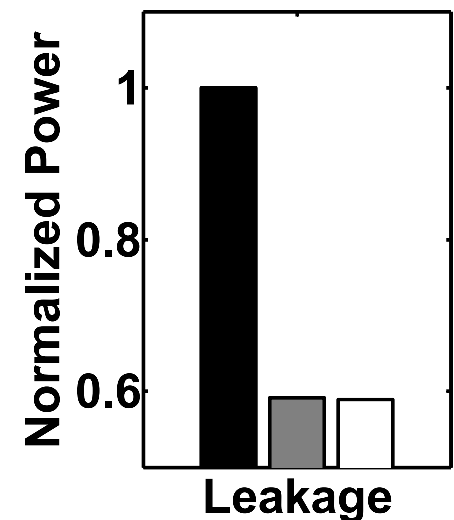
Park, Raghunathan, Roy; DAC'12

Comparison of 1T-1R with SRAM Last Level Caches with Similar Cache Area (2MB SRAM, 8MB STT MRAM)

2MB 6T SRAM | 8MB STT MRAM (Standard) | 8MB STT MRAM (Tilted Magnetic Anisotropy)







Higher Latency

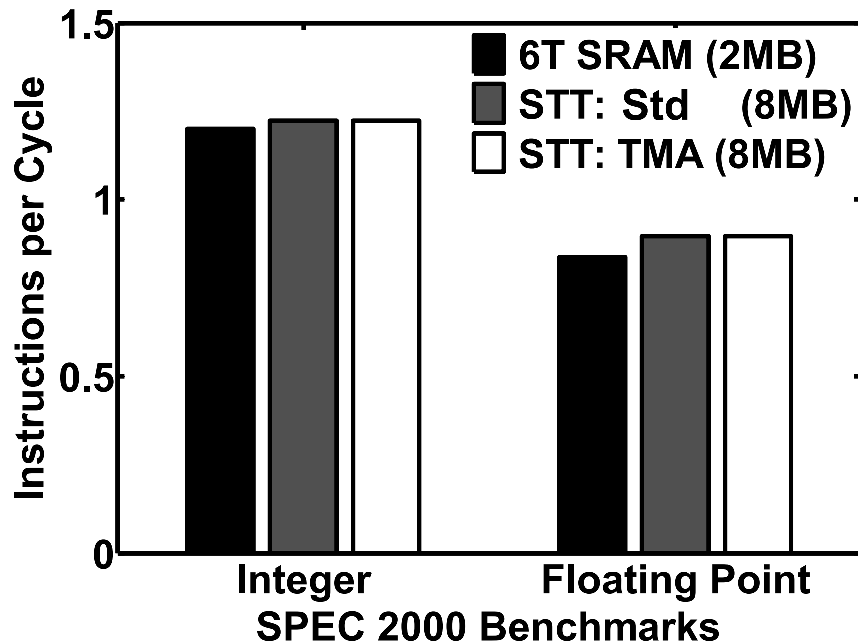
Higher Active Energy

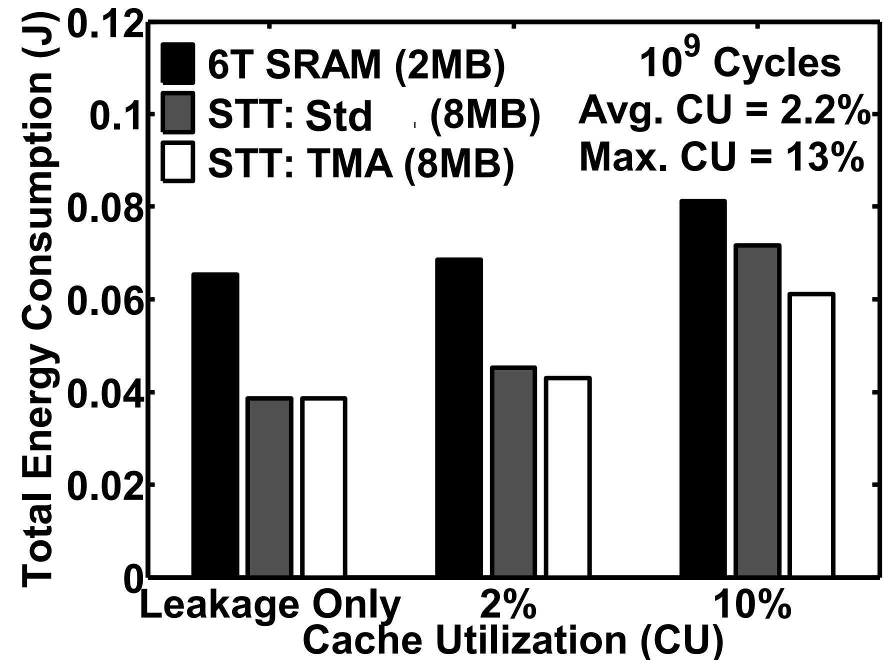
Lower Leakage

4X higher capacity

[1] S. P. Park *et al*, DAC 2012

System Level Implication of STT MRAM Last Level Caches





Compared to SRAM cache STT MRAM caches offer
- **Higher throughput due to larger integration density and lower cache miss rate**
- **Lower Energy due to low leakage and low utilization**

[1] S. P. Park *et al*, DAC 2012

Boolean/Non-Boolean Computing with Spin Torque Transfer Devices

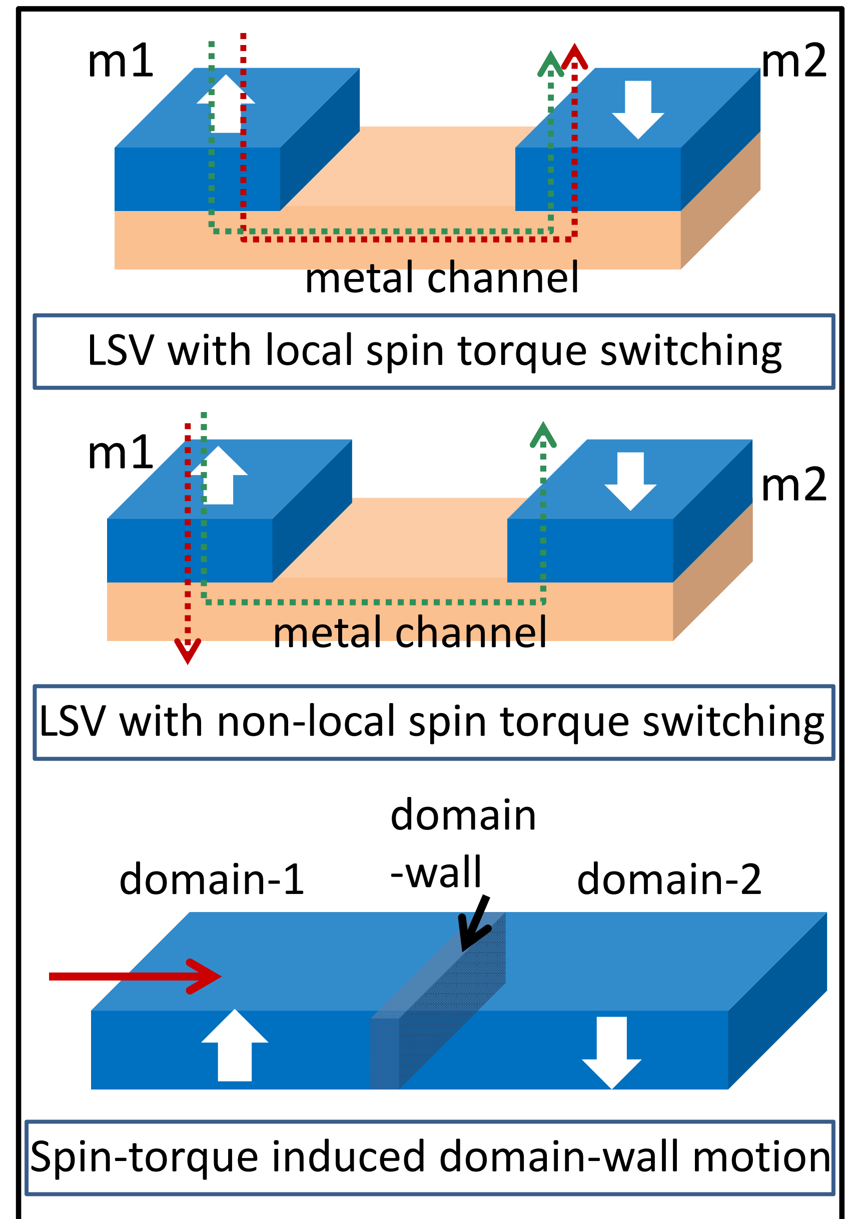
Spin-Torque Experiments

➢Nano-magnets in a Lateral Spin Valves (LSV) can interact and switch through spin-torque

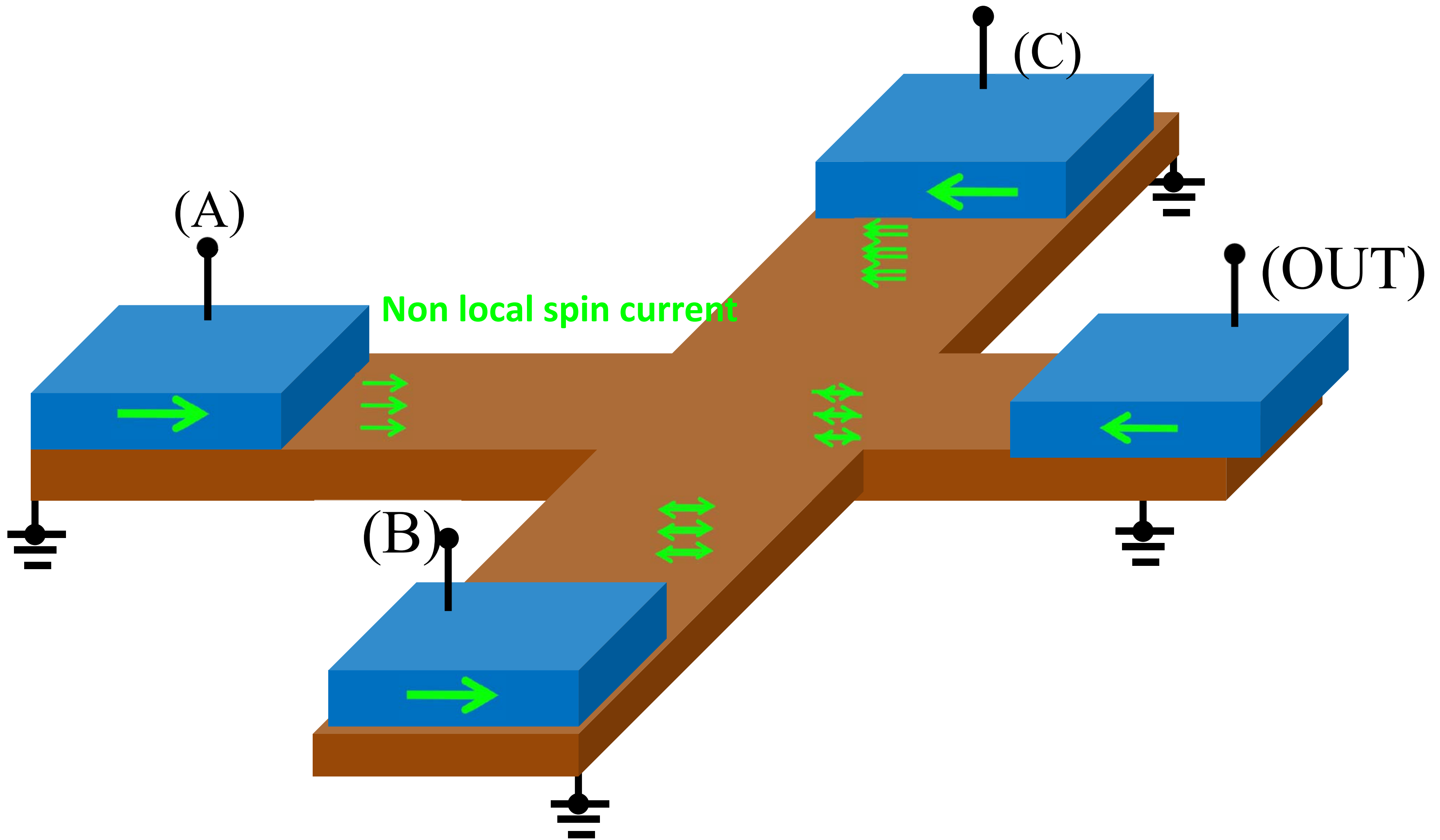
➢Non-local STT switching in LSV can be employed to realize All Spin Logic Device (ASLD)

➢ Low-current, high-speed domain-wall motion can be achieved in scaled ferromagnetic nano-strips with perpendicular magnetic anisotropy (PMA)

➢ Such low energy DW motion can be employed in logic computation



Spin Majority Gates using ASL



Spin majority gate with odd number of inputs can be realized using ASL

Compact Full Adder: Non-Boolean Logic

- **Option1:** with standard NAND logic (44 magnets)
- **Option2:** functionality enhanced NB logic (5 magnets)

Inputs: A, B and C

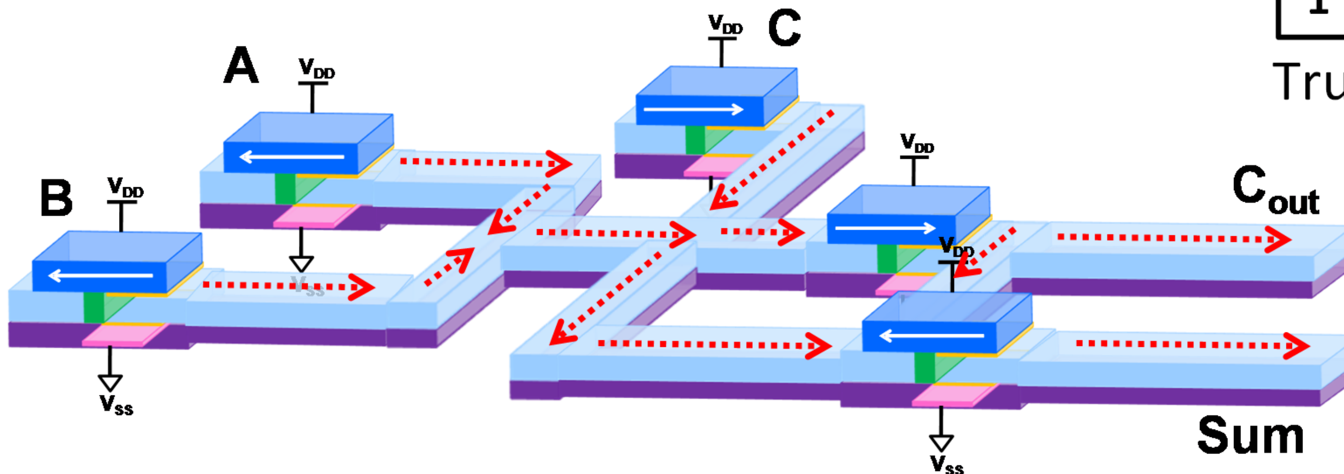
Outputs: Sum and Cout

$$Sum = A \oplus B \oplus C$$

C_{out}=AB+AC+BC=M (A,B,C)

A	B	C	C'_{out}		Sum
0	0	0	1	1	0
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	1

Truth Table for SUM

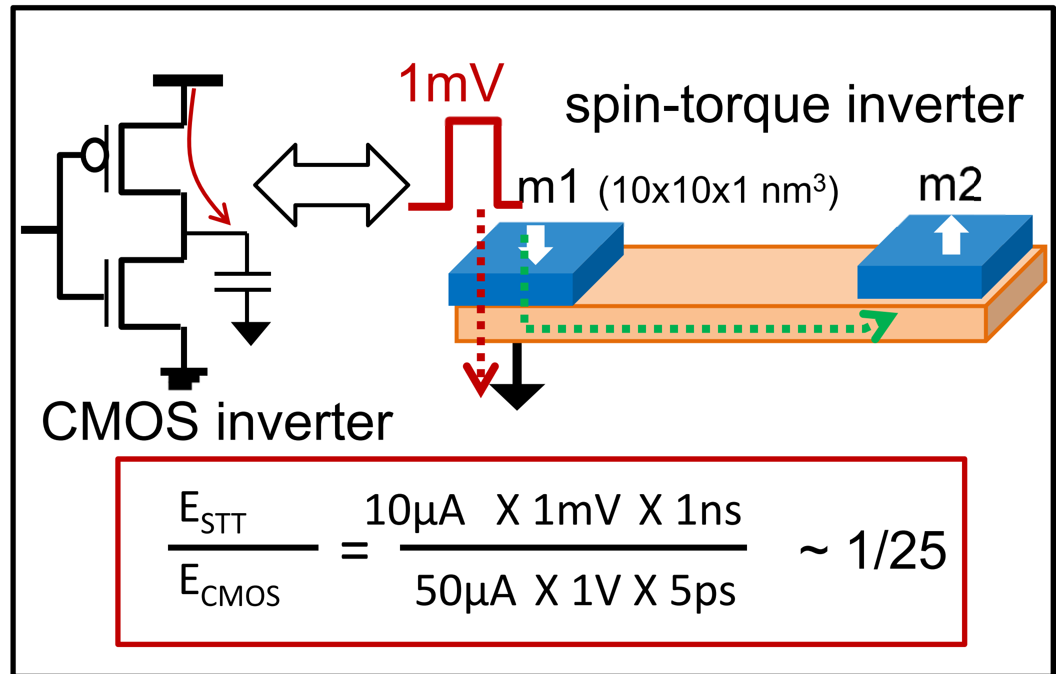


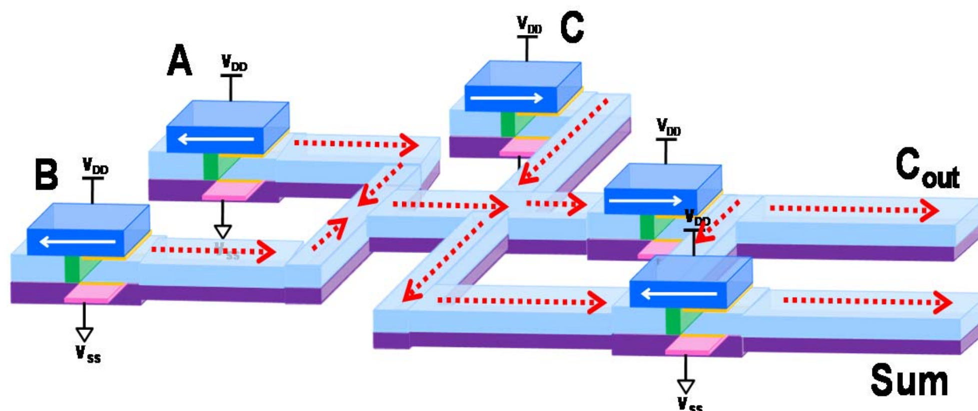
C. Augustine et al., NanoArch, 2011

Boolean Logic Using Spin Torque Devices

- low voltage, spin-torque switching in spin valves can possibly achieve lower switching energy than CMOS

- Compact All Spin Logic gates can achieve higher area density





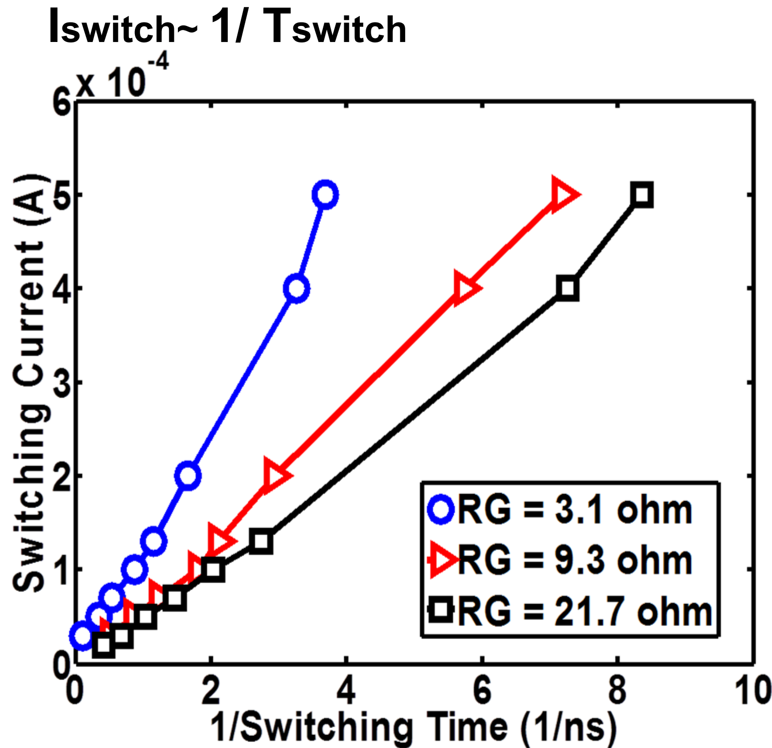
Full-Adder based on All Spin Logic

Majority Gate

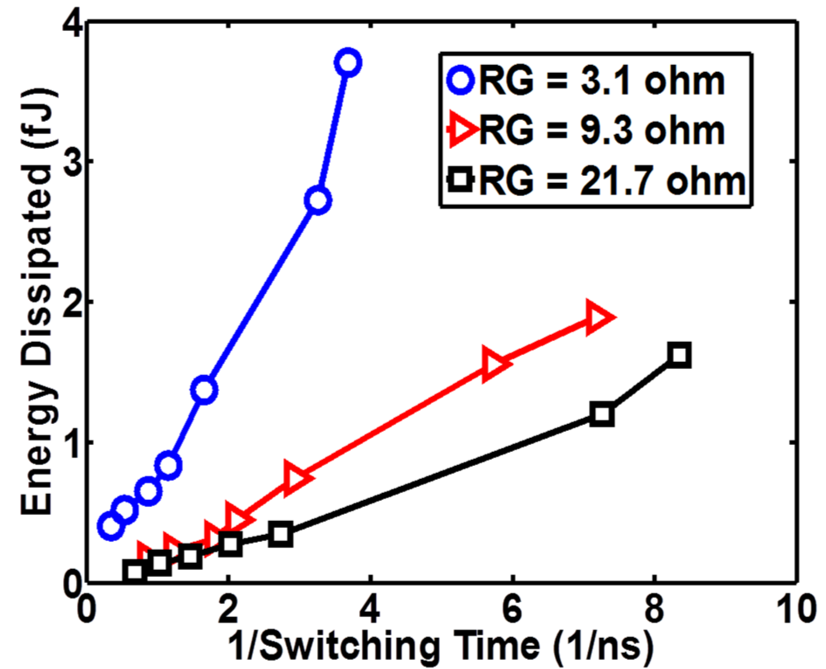
A	B	C	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Switching Energy vs. Speed

$I_{switch} \sim 1/T_{switch}$



$E_{switch} = T_{switch} \times I_{switch} \times V_{switch}$



$$\frac{E_{STT}}{E_{CMOS}} = \frac{30\mu A \times 1mV \times 0.5ns}{50\mu A \times 1V \times 5p} = 1/25$$

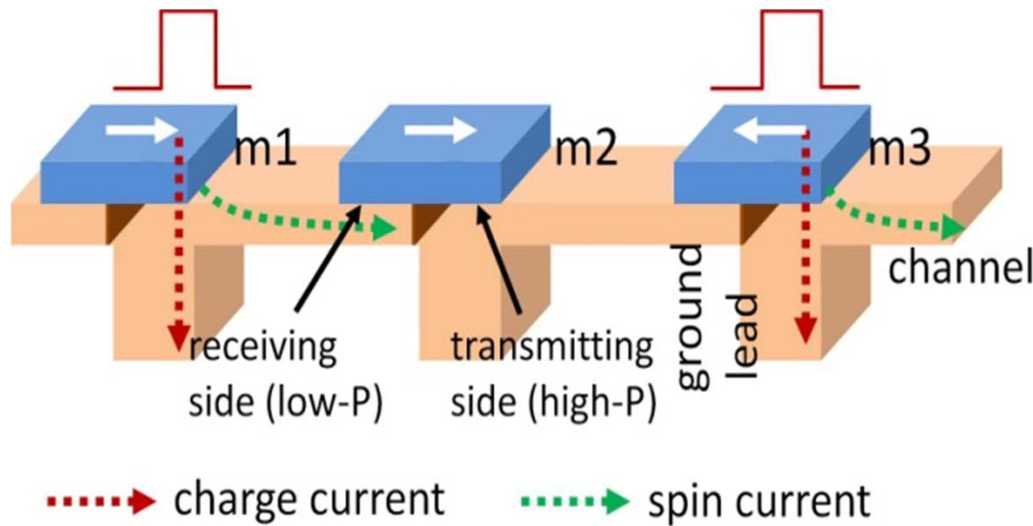
low speed STT switching

$$\frac{E_{STT}}{E_{CMOS}} = \frac{300\mu A \times 10mV \times 50ps}{50\mu A \times 1V \times 5p} = 4$$

high-speed STT switching

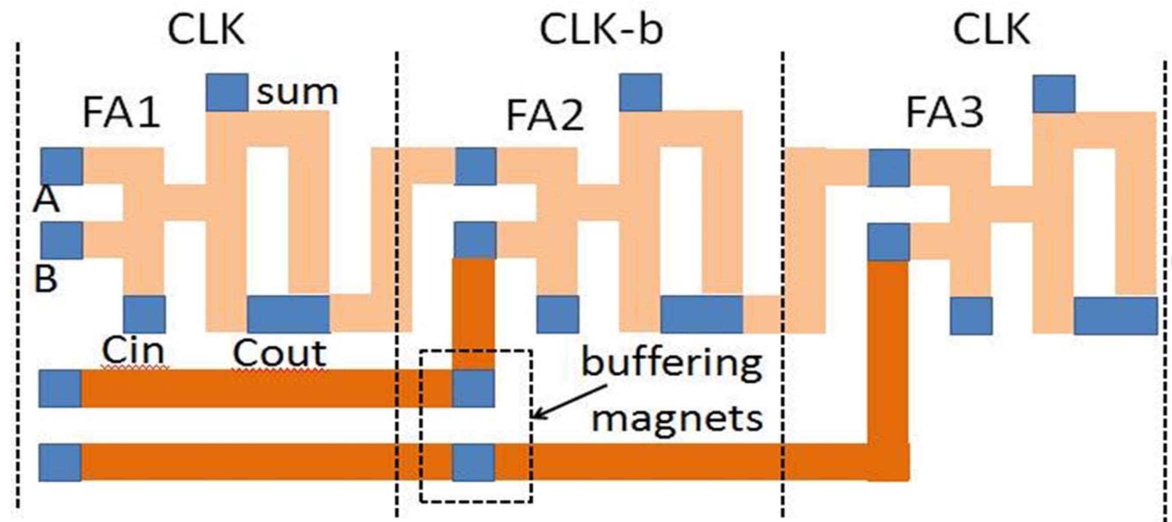
For an isolated logic gate switching energy increases linearly with switching speed

2-Phase Pipelining for Enhanced Performance



Non-volatile nano-magnets facilitate pipelining simply by the use of clocked power supply

No extra latches needed!



M. Sharad, K. Roy, ISQED, 2013

2-Phase Pipelining for Enhanced Performance

For a logic block with N-magnets in series :

$E_{switch} = \mathbf{N}(T_{switch} \times I_{switch} \times V_{switch})$

Where $T_{logic} = N\ T_{switch}$

For fine-grained pipelining:

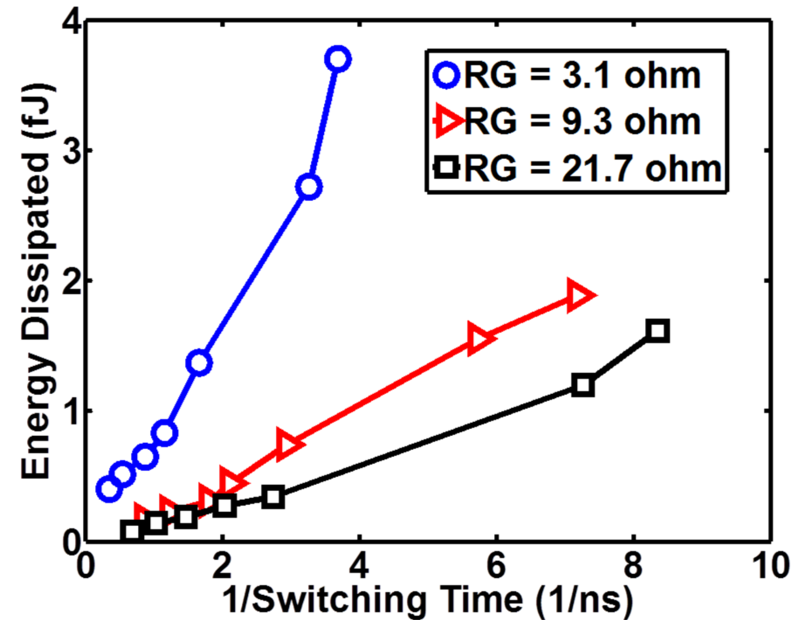
$$T_{logic_pl} = T_{switch_pl}$$

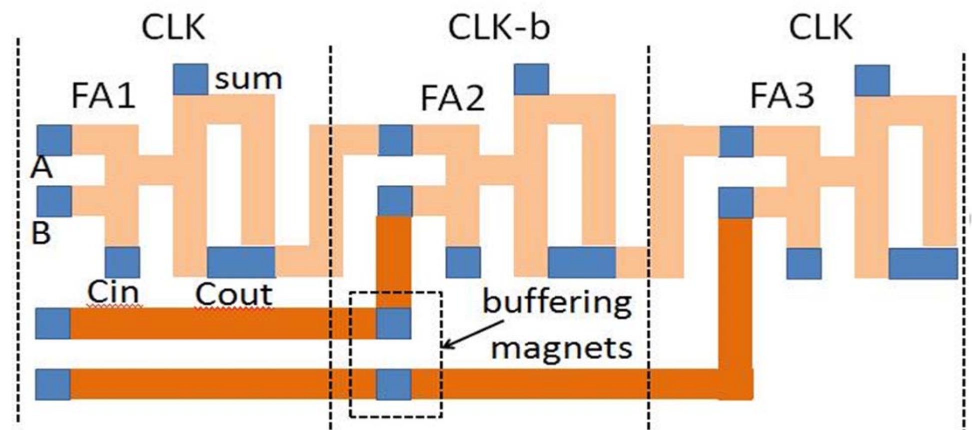
Hence , $T_{switch_pl} = T_{switch} / N$

$$E_{switch_pl} = E_{switch}/N$$

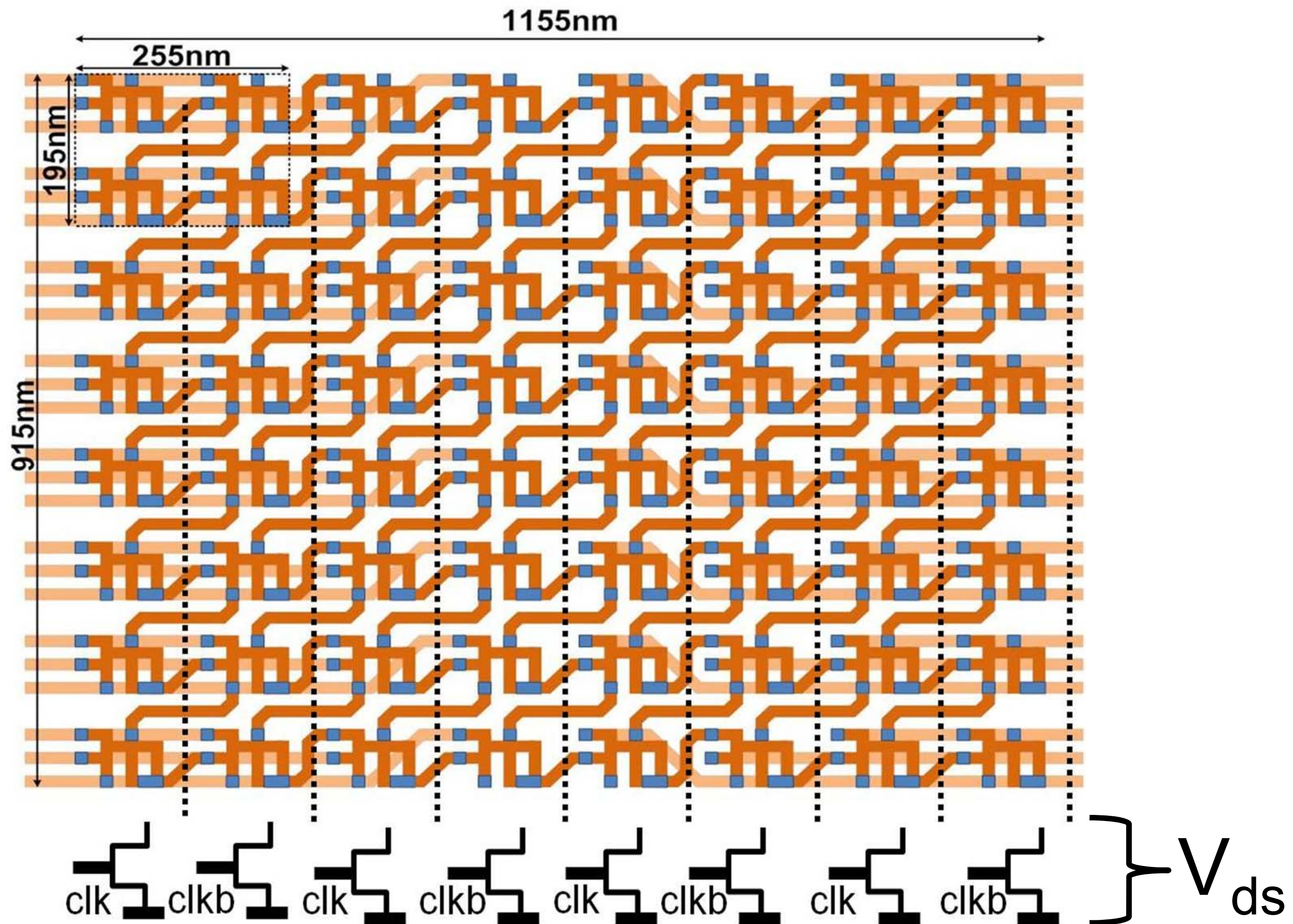
Reduction in switching energy proportional to the number of logic stages in a pipeline can be achieved

$E_{switch} = T_{switch} \times I_{switch} \times V_{switch}$





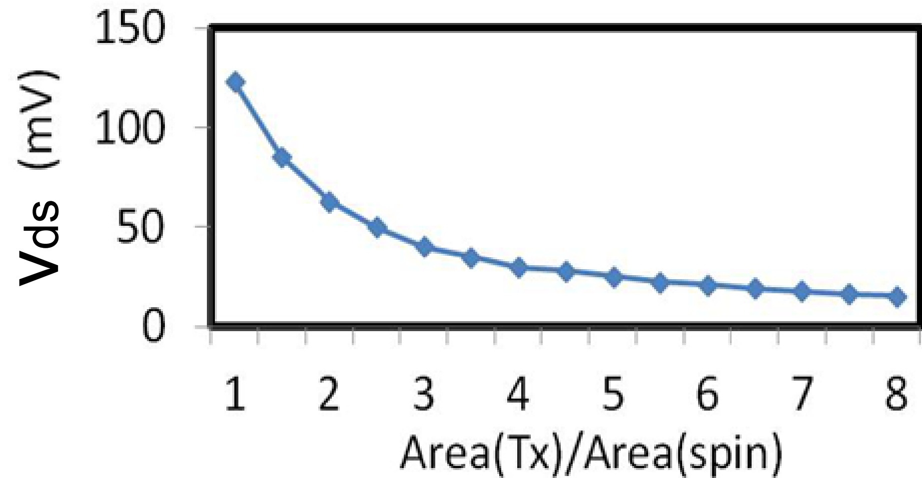
2-Phase Pipe-lined 8-bit Multiplier (Carry-save)



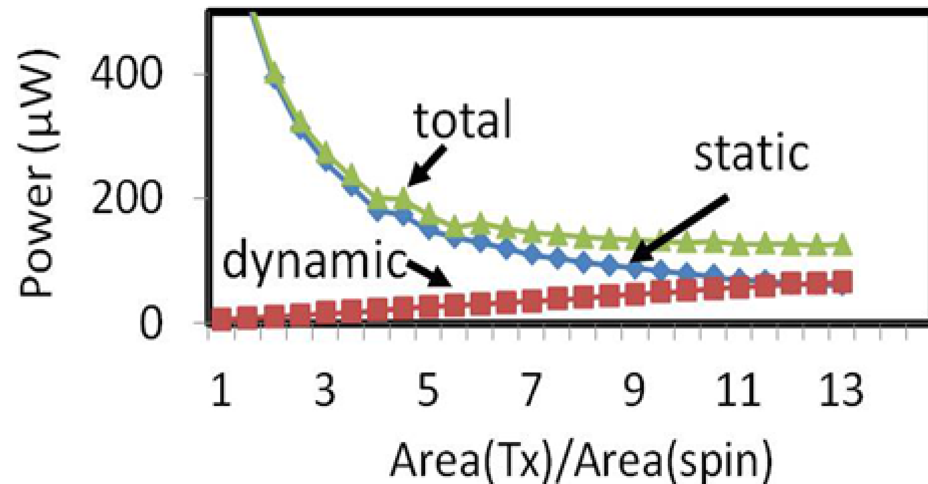
Clocked power supply requires transistors which increase the required voltage supply

2-Phase Pipelining: Design Optimization

Supply voltage needed for pipelined spin-logic reduces with Area_Tx,



Higher transistor width and lower supply voltage leads to reduction in static power but the dynamic clocking power increases.

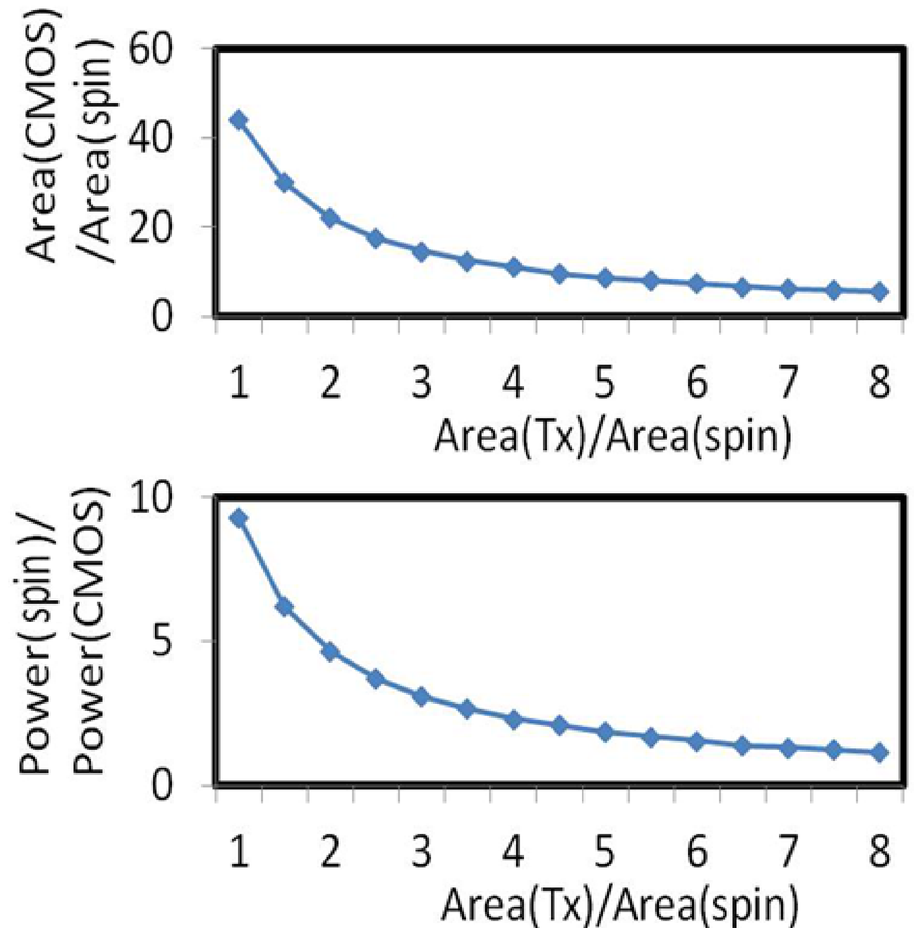


2-Phase Pipe-lining: Design Optimization

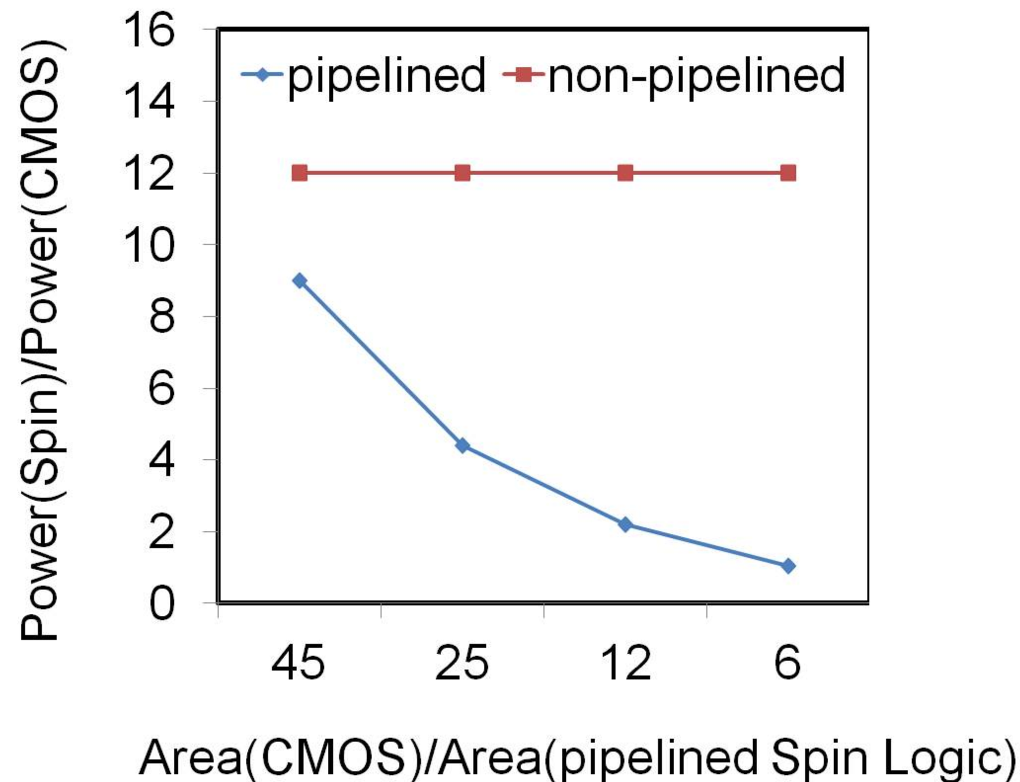
Area benefit of pipelining over 15nm CMOS design reduces with increasing Tx area for spin logic.

Power consumption of pipelined design reduces with increasing Tx area

It reaches a saturation point due to increase in dynamic power



2-Phase Pipelining: Design Trade-off



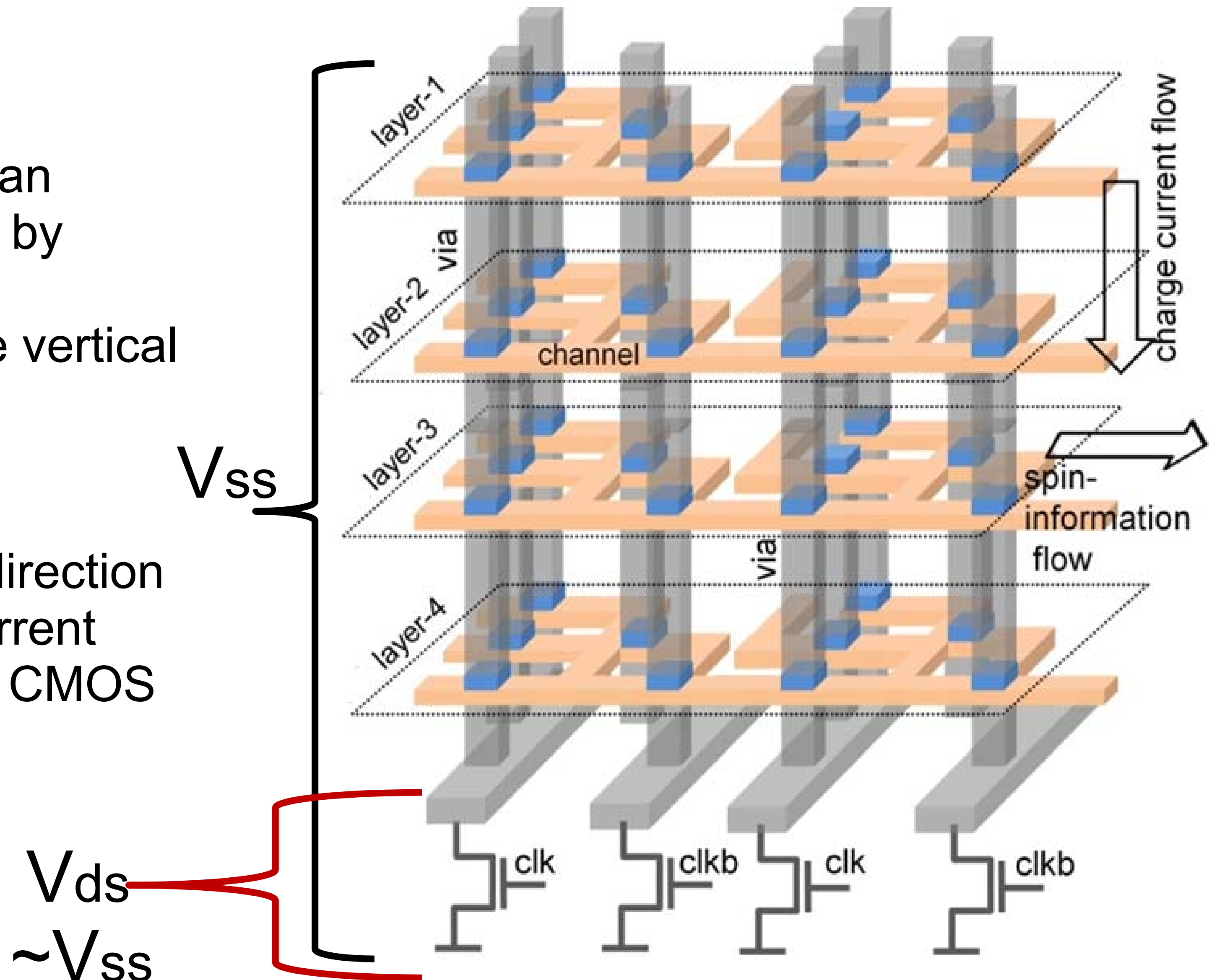
Minimum size clocking transistors require large V_{ds} and hence overall power consumption can be high

Area of spin logic block can be traded off (by using larger clocking transistors) to achieve larger power saving.

3-D FOR HIGH DENSITY AND LOW POWER COMPUTATION BLOCKS

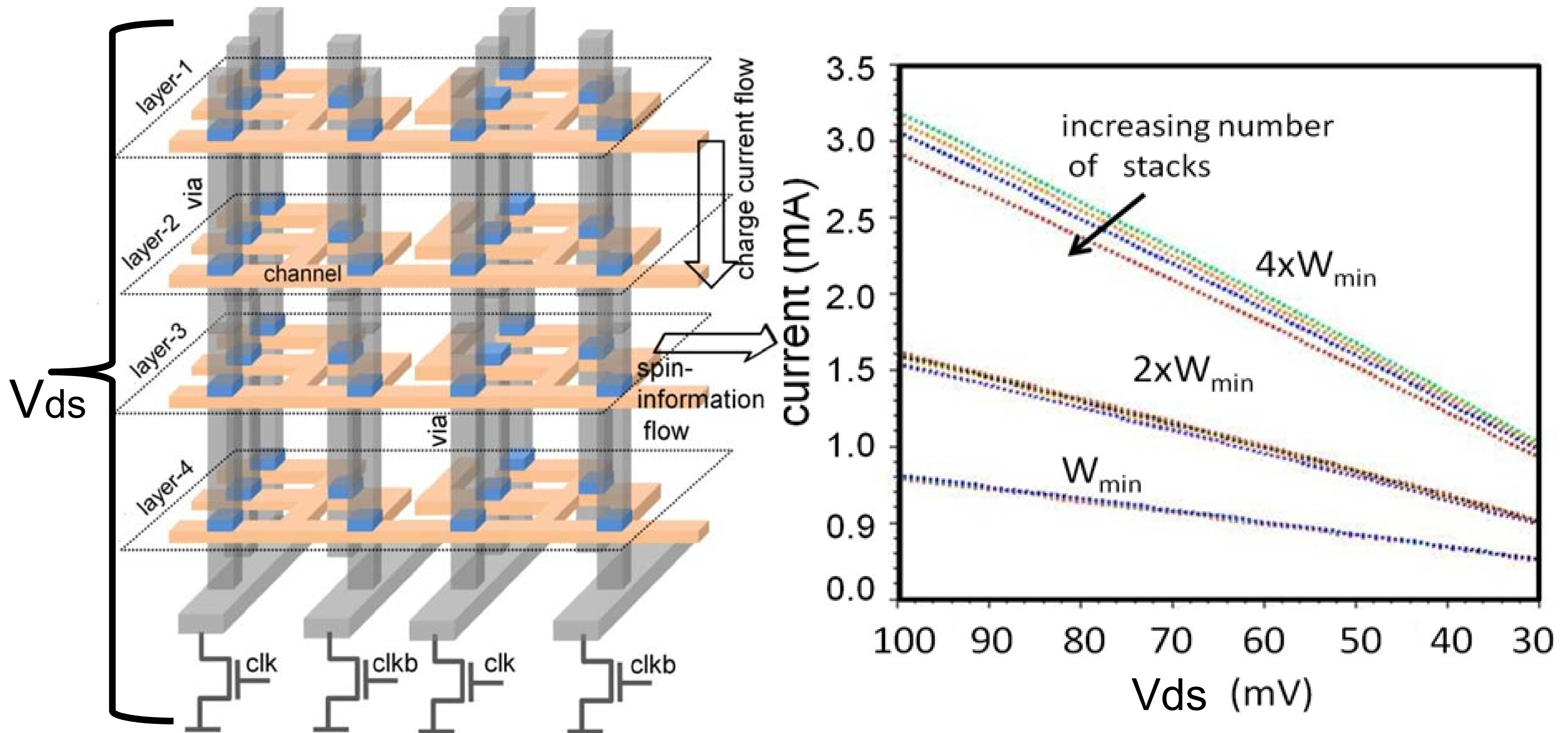
3-D spin logic can be constructed by stacking 2-D layers along the vertical direction.

All the layers in the vertical direction are supplied current using the same CMOS transistors.



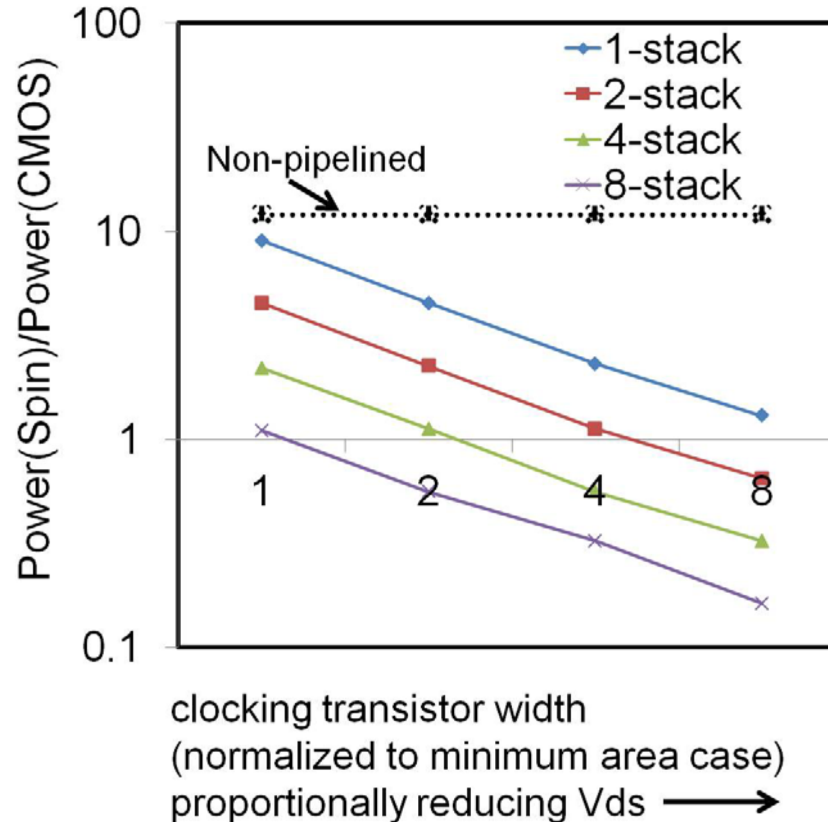
M. Sharad, K. Roy, ISQED, 2013

3-D FOR HIGH DENSITY AND LOW POWER COMPUTATION BLOCKS



Due to low resistance of the metallic vias, the current injection per magnet remains almost the same for a given transistor width and supply voltage, even when multiple layers are stacked.

3-D FOR HIGH DENSITY AND LOW POWER COMPUTATION BLOCKS



Staking N layers reduces the effective power consumption by a factor of N

For a given number of stacks, larger size of clocking transistors can be used to lower the supply voltage and hence the static power

Purdue University Nanoelectronics Research Laboratory

Non-Boolean/Neuromorphic Computing with Spin Devices

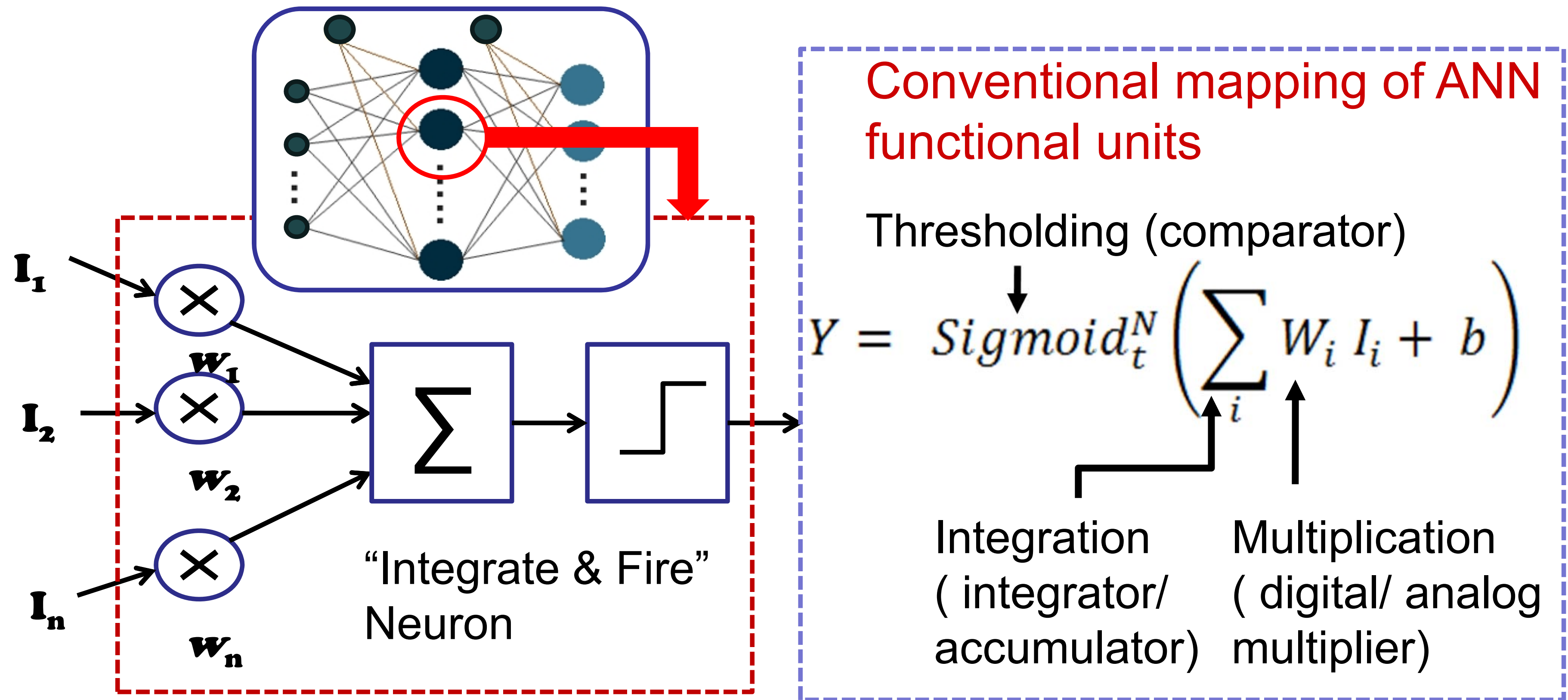
M. Sharad, K. Roy; TNANO 2011, DAC 2012, DRC 2012, IEDM 2012

Non-Boolean & Neuromorphic Computing

- Traditional computing models (Boolean logic, von Neumann architectures) are highly inefficient at performing tasks that humans routinely perform, such as visual recognition, semantic analysis, and reasoning.

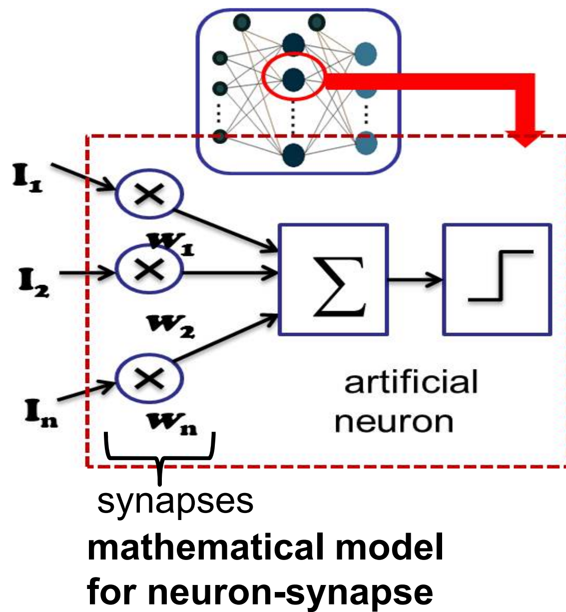
- Bio-inspired computation can outperform Von-Neumann designs in many such data processing applications

Hardware Implementation of Neural Networks

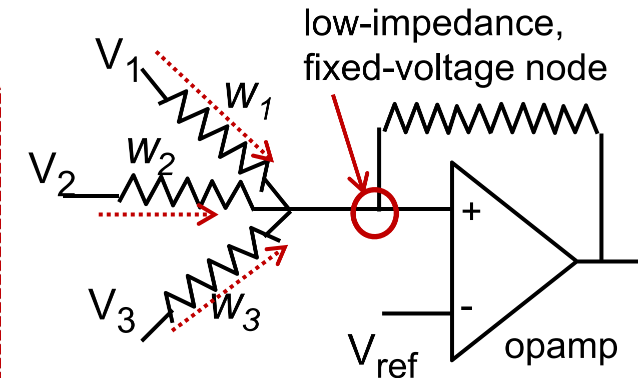


Digital designs consume large area whereas analog designs provide power hungry solutions. Hence, there is need to match the characteristics of the devices to the computing models to provide drastic improvements in efficiency.

Artificial Neural Networks



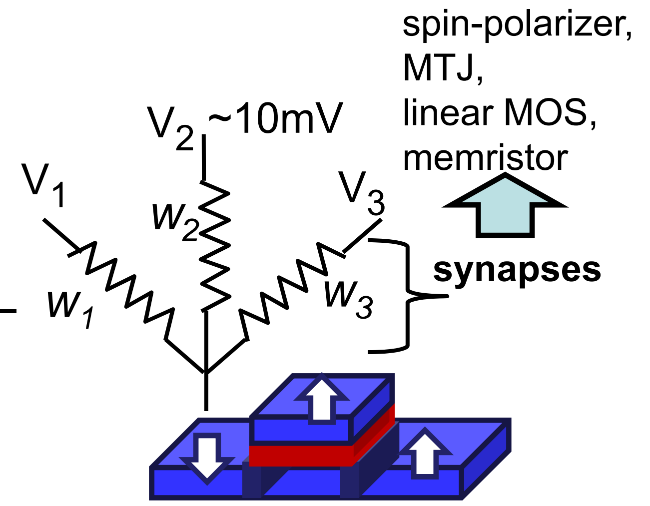
mathematical model for neuron-synapse



Analog-CMOS implementation of Neuron

V_{supply} ~ 1V, bias current ~10-100μA

switching-speed > 10-100ns



Spin Neuron

V_{supply} ~ 10mV

switching-speed ~ 1ns

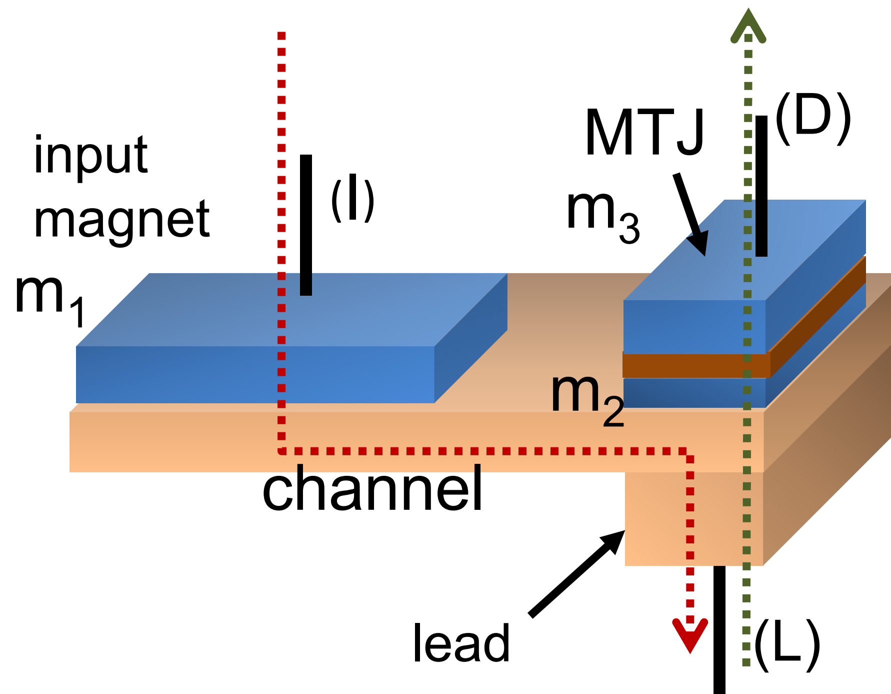
free-layer: 20x20x2

critical current : few μA

Sharad, Roy; TNANO'12; Sharad, Roy, DAC, 2012 Sharad, Roy, IEDM, 2012 Sharad, Roy, IJCNN, 2012

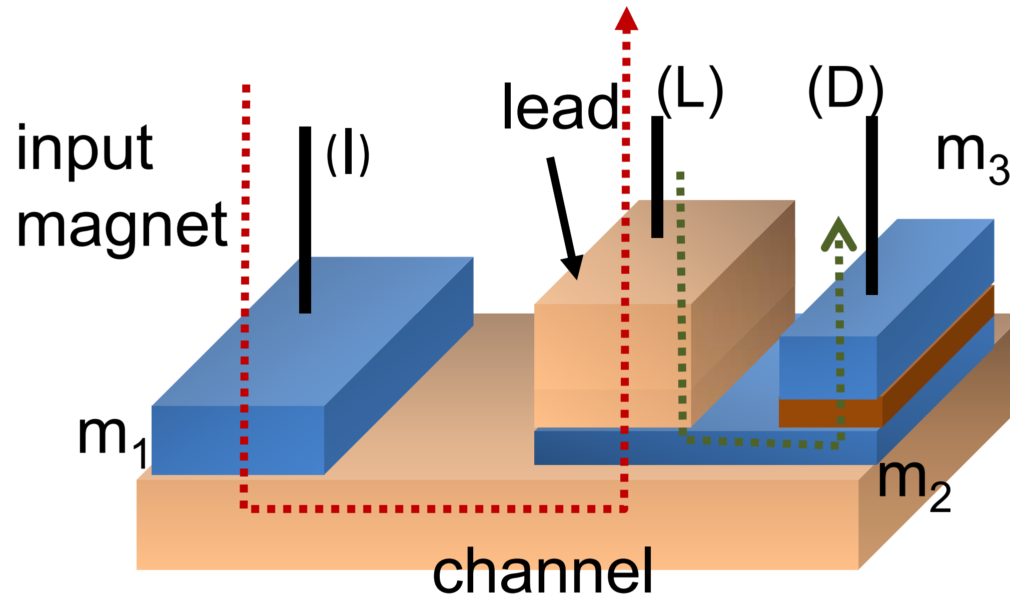
- **Low-impedance, current-mode STT-switches can provide compact and energy-efficient mapping for analog thresholding operation of a 'neuron'.**
- **Spin neurons with spin/charge based synapses can facilitate the design of ultra low power neuromorphic hardware for non-Boolean data processing.**

Lateral Spin Valve with Decoupled Read-Write Path : Non-local Spin Injection



- ❑Read-write decoupling in LSV's facilitates ultra low voltage switching
- ❑MTJ interface allows dynamic read operation with ~zero static power dissipation

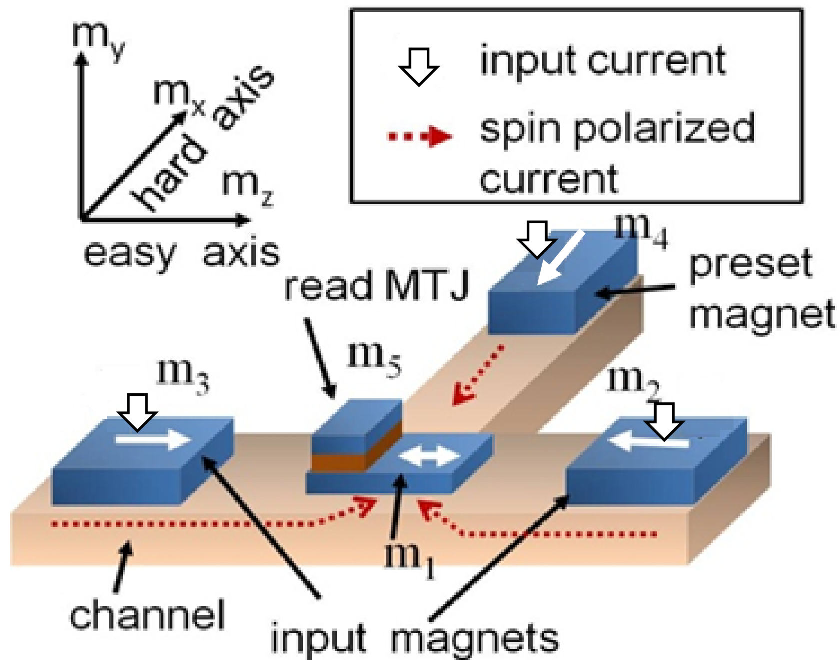
Lateral Spin Valve with Decoupled Read-Write Path: Local Spin Injection



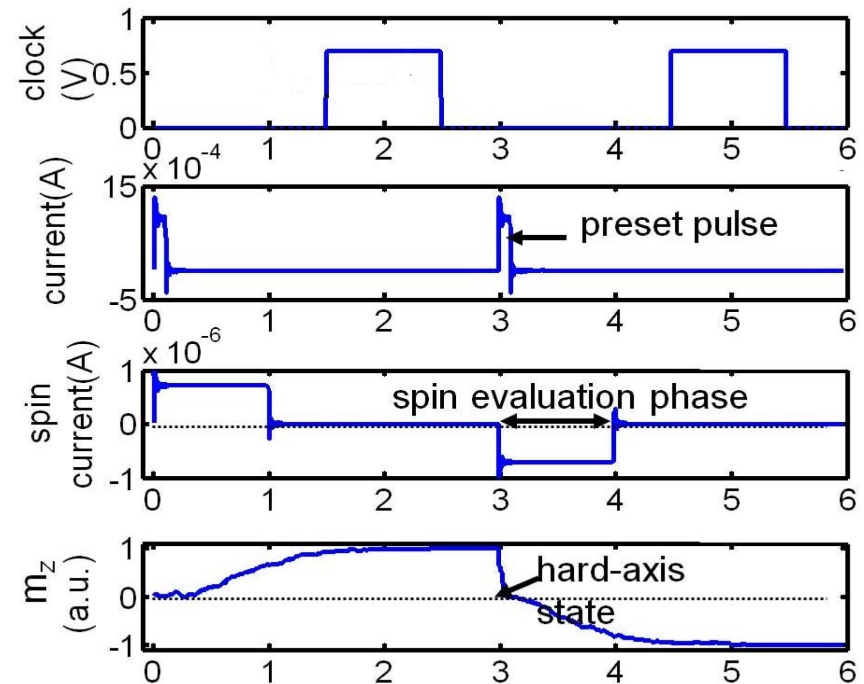
- This structure employs local spin injection, can achieve higher injection efficiency apart from read-write decoupling
- An extended read-port is used for sensing, while write -current is injected into the output lead through the magnet
- Small dimension of m_2 insures mono-domain behavior, despite the read extension

Bipolar Spin Neuron Using Lateral Spin Valve

Device Structure

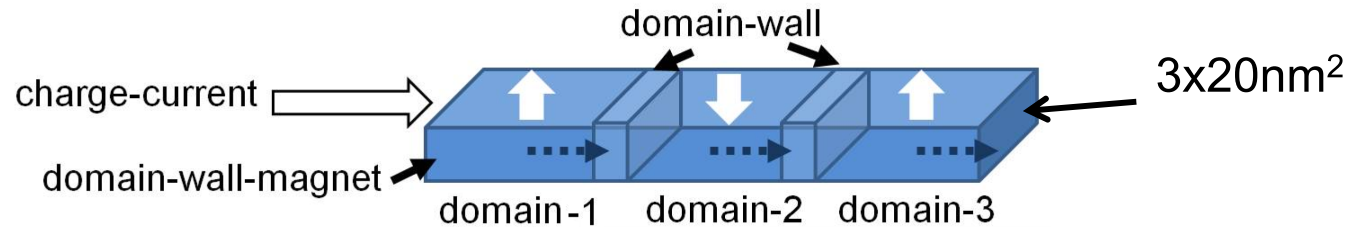


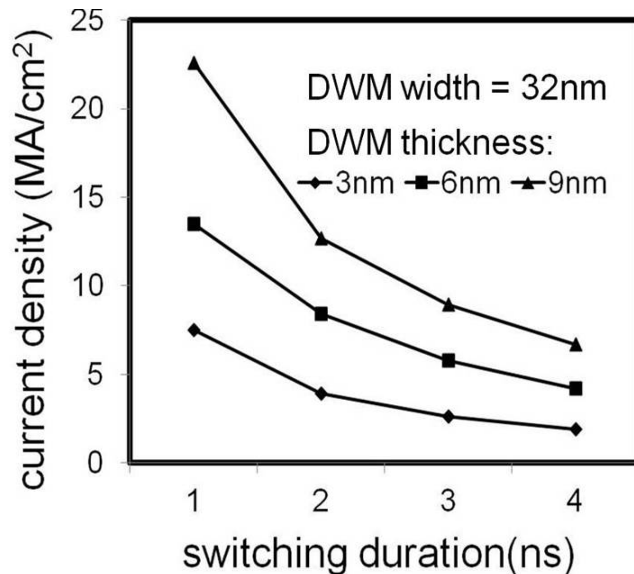
Device operation

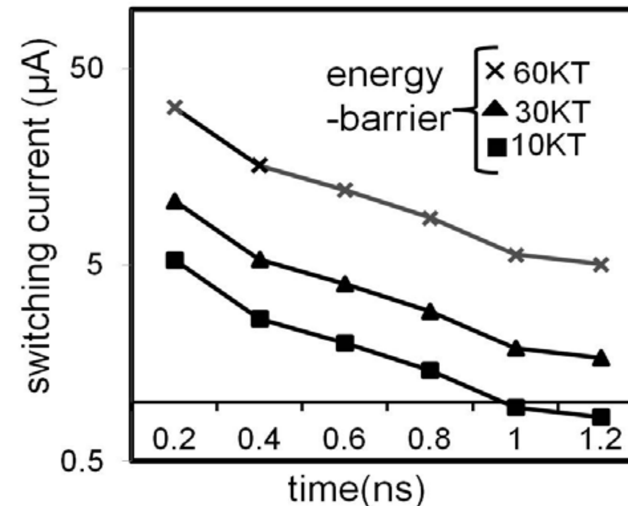


The neuron device essentially acts as an ultra low voltage current comparator and can be employed to perform analog-mode computation

Neuron Models Using Domain Wall Magnets







❑ Properties of DWM favorable for high-speed, low current switching:

➢ **Scaling** (DW width as well as thickness) reduces the critical current for DW-motion [2, 4]

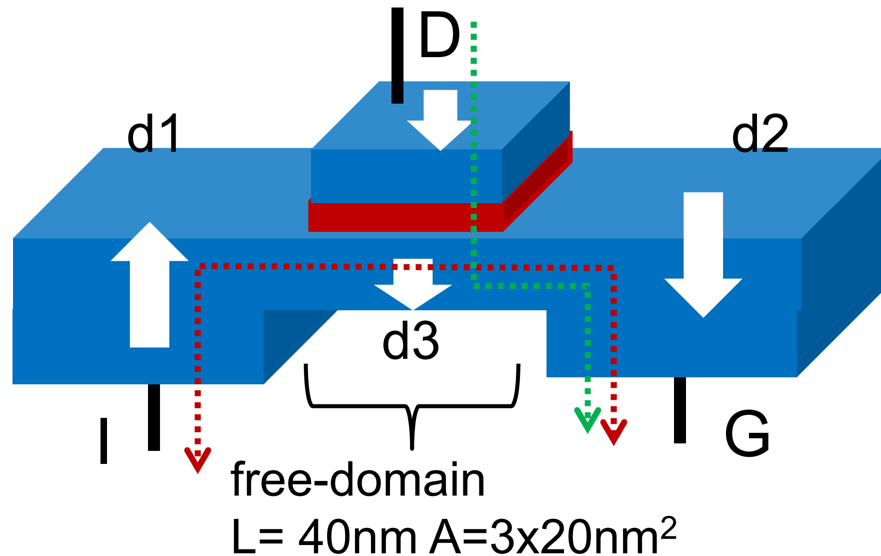
➢ **PMA device** achieve significantly lower critical current density ~10^6 A/cm^2 [4]

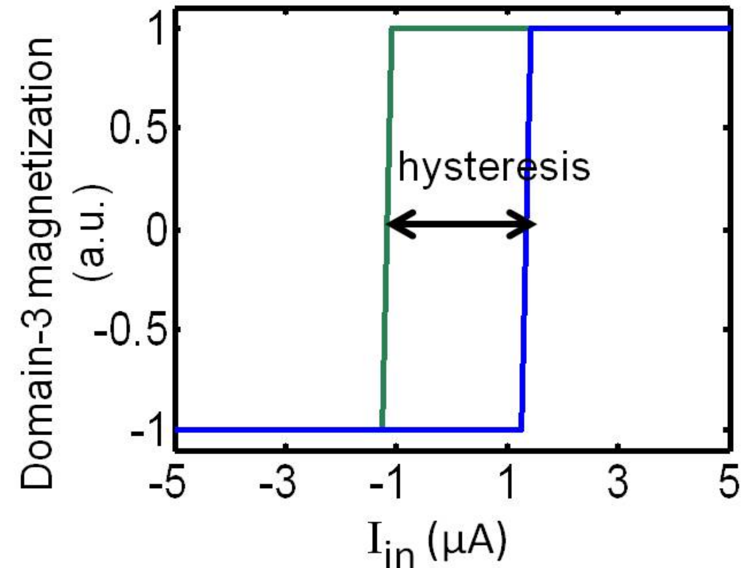
➢ **Lower saturation magnetization** and **higher coercive field** can achieve faster switching [1]

➢ **Non-volatility can be sacrificed** for high speed computing to further reduce the switching current

[1] Duc-The Ngo et al.," *arXiv preprint arXiv:1110.5112* (2011). [2] K. Ikeda et al., " *Applied physics express* 4.9 (2011): 3002.
[3] C. K. Lim et al." *Applied physics letters* 84.15 (2004): 2820-2822. [4] S. Fukami,, et al “*IEEE Symp. on VLSI Tech.,* 2009.

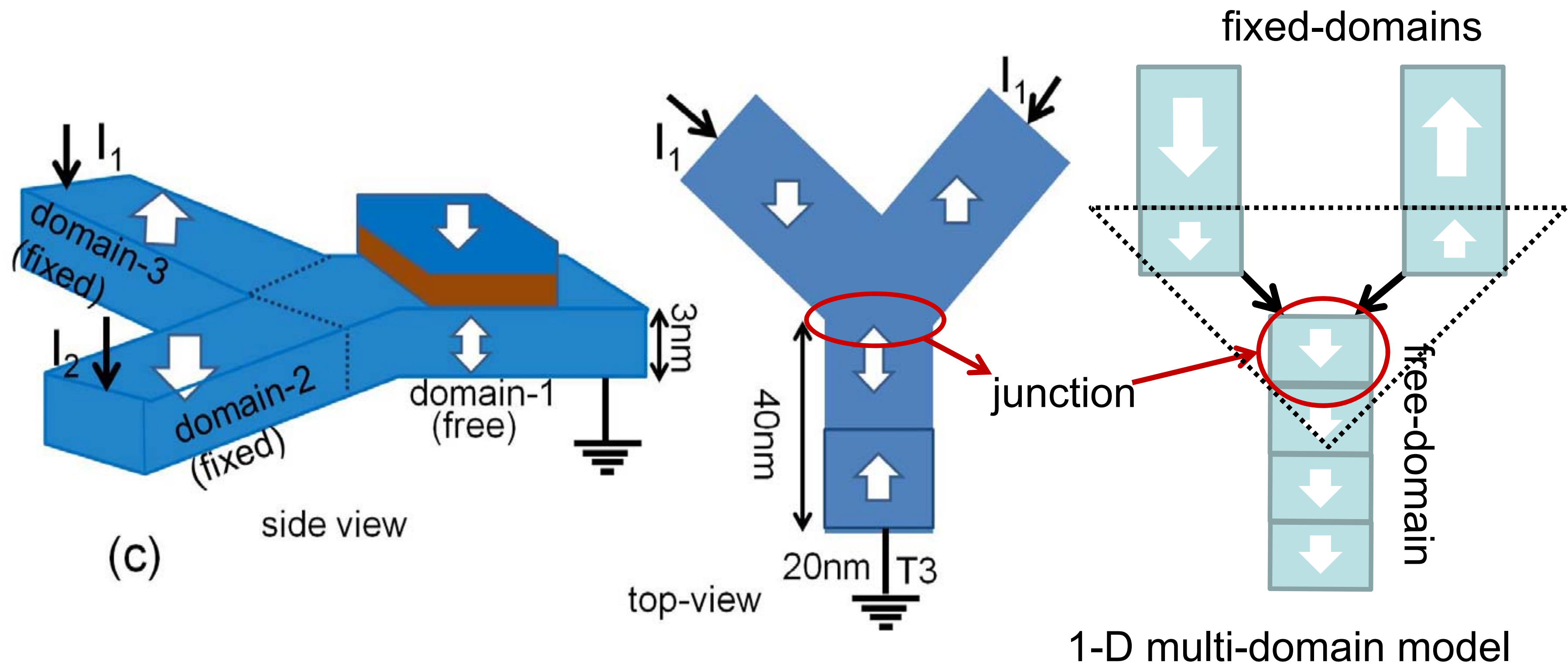
Unipolar Domain Wall Neuron





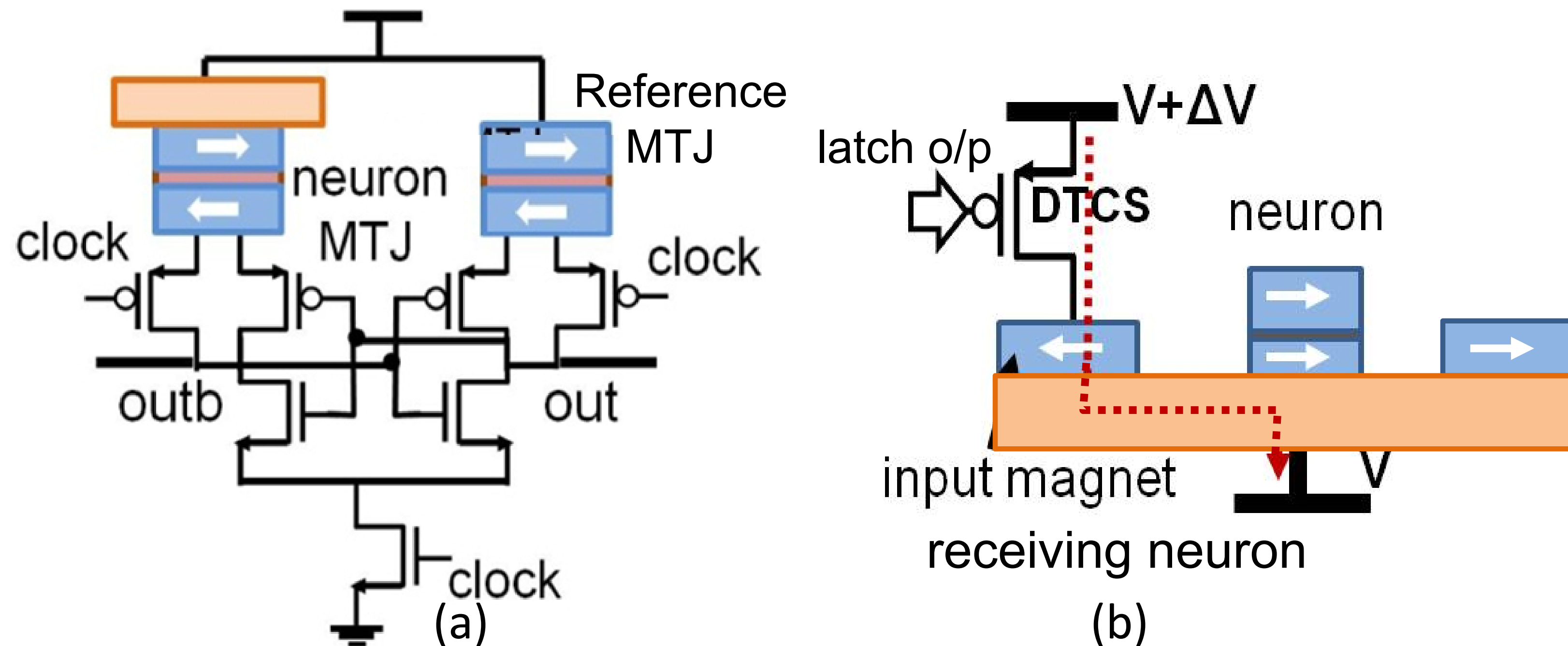
- A thin and short PMA DWM free-layer can be switched with a small current ~1 μA within 1ns
- Such a magneto-metallic device can be used to perform ultra low voltage and low energy current-mode summation and thresholding, like a **"neuron"**

Bipolar Domain Wall Neuron



- BDWN can compare the input currents received through the two input domains
- The resolution is determined by the critical switching current density for DW nano-strip

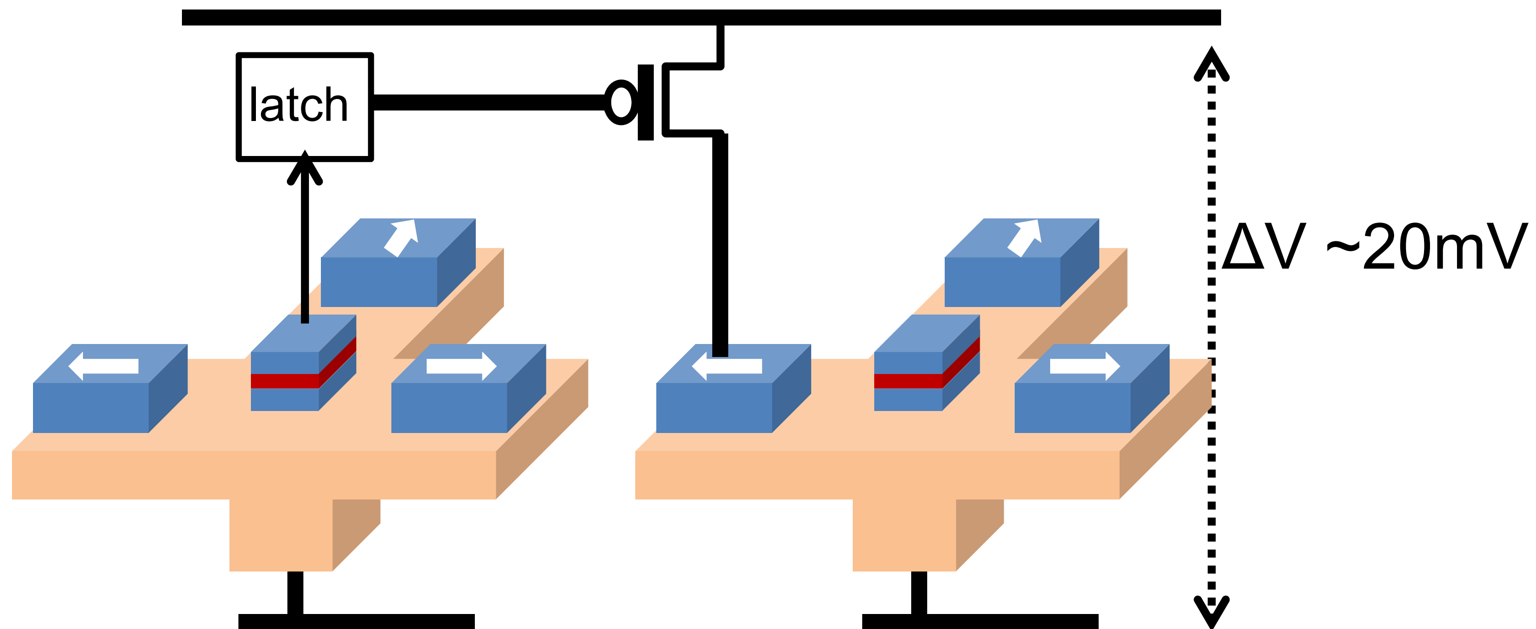
Communication between Neurons



- CMOS latch detects the state of neuron-MTJ without static current injection
- Deep-triode current source (DTCS) transistor driven by an output latch transmits current mode signal to receiving neurons
- Computation current flows across a terminal voltage of ΔV

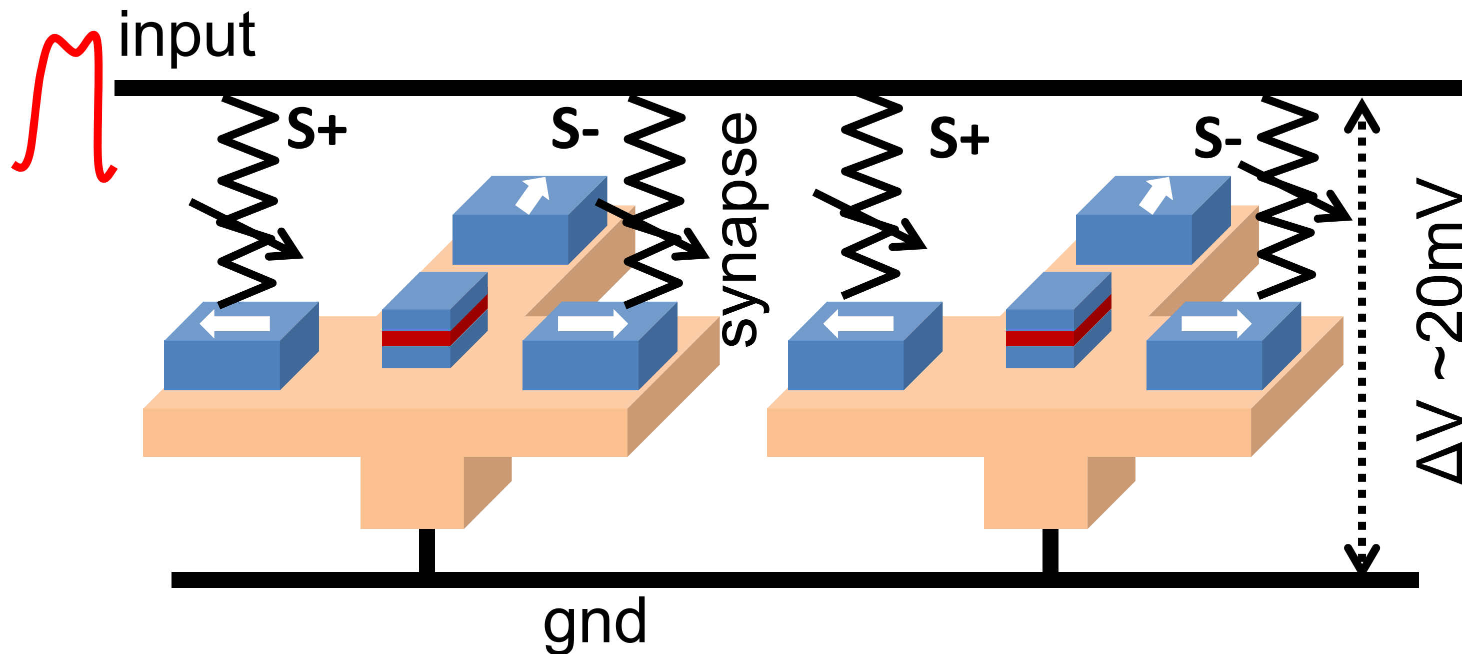
Communicating Neurons

Neurons can be interconnected using weighted DTCS (Deep Triode Current Source) transistors.



- Depending upon the polarity of inter-neuron weight, output of a source neuron connects to one of the inputs of the receiving neuron.
- Current-mode, inter-neuron signaling takes place through DTCS transistors operating at ~20mV drain-to-source voltage resulting in low computation power

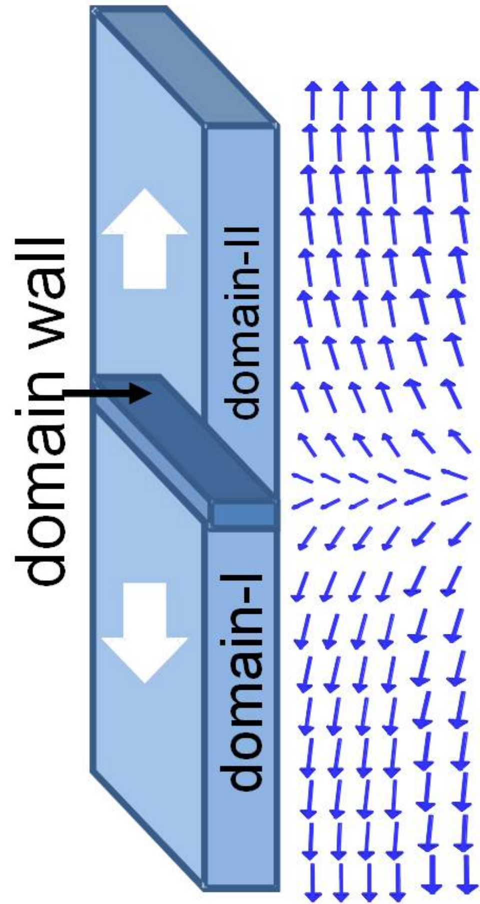
Programmable Synapses: Memristors/PCM

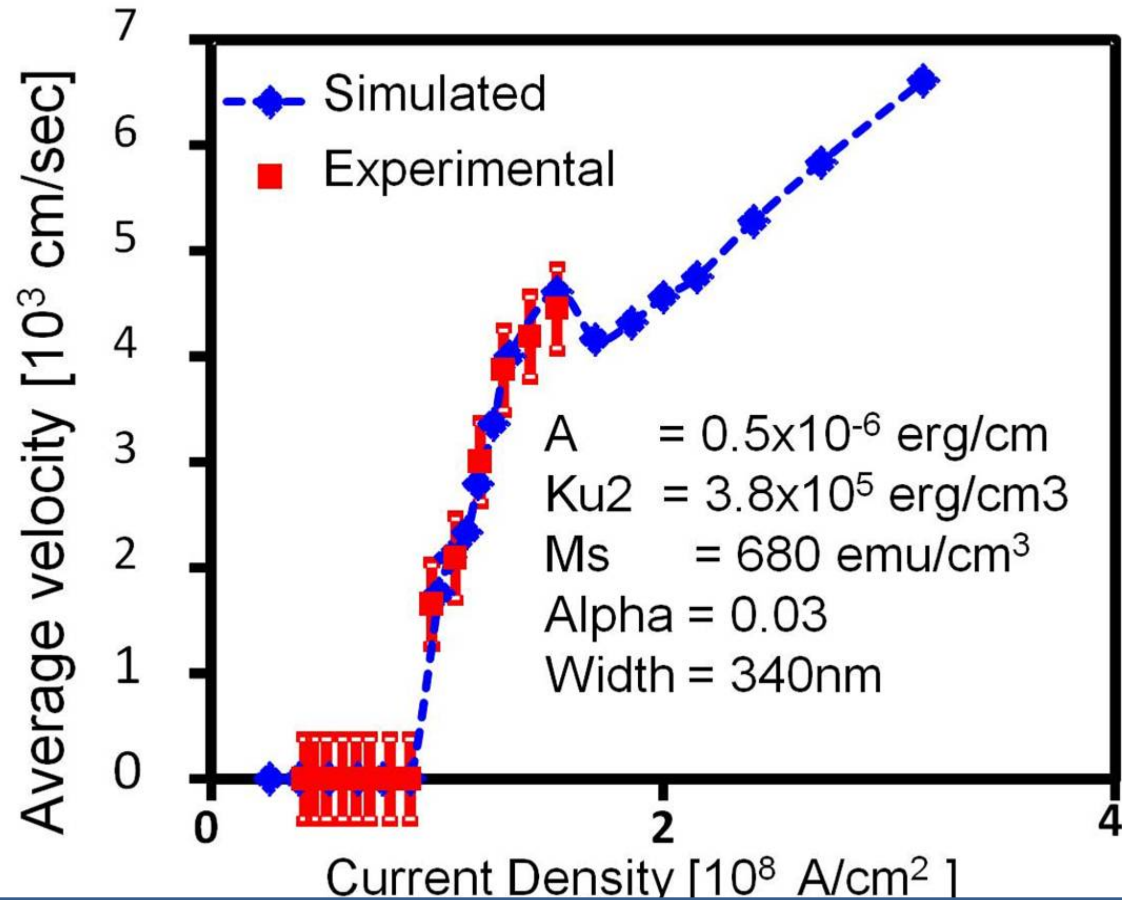


- Memristors/PCM/DWM/ can be used for realizing low power neuromorphic computation array using bipolar spin neuron

- The magneto-metallic neurons facilitate input voltage levels of ~20mV resulting in low computation power

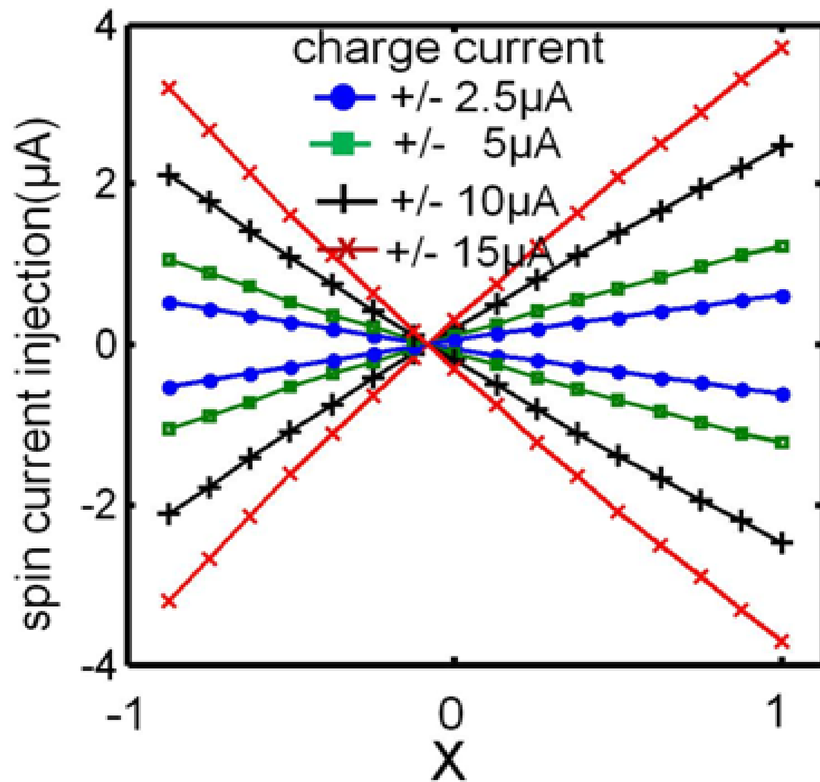
Synapse: Domain Wall Magnet

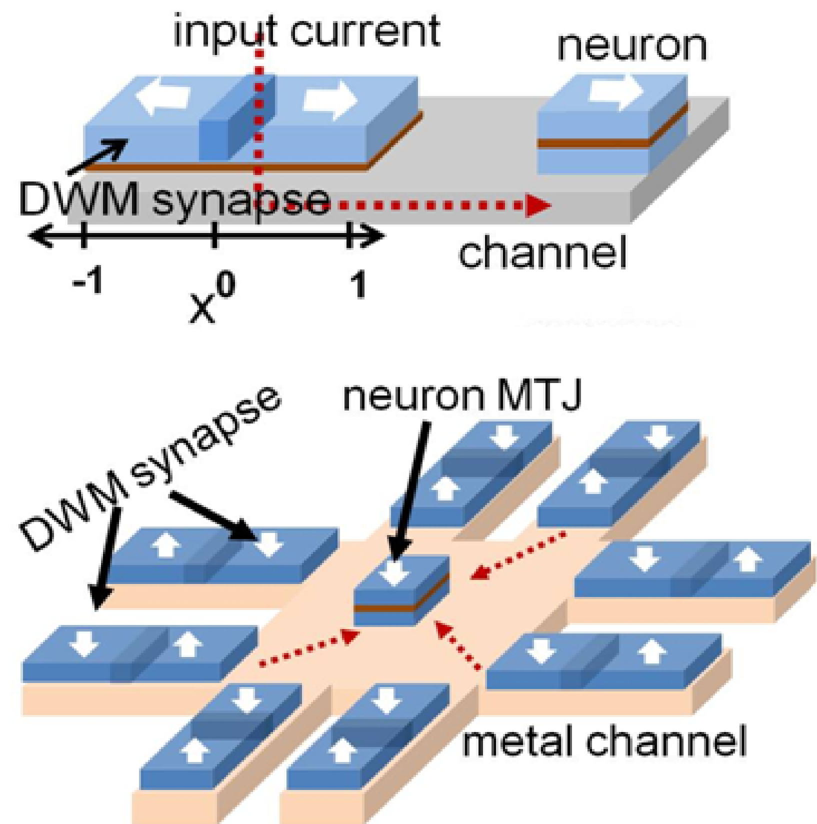




A DWM consists of opposite polarity domains separated by a Non-magnetic region call the domain wall which can be moved by charge injection/ magnetic field

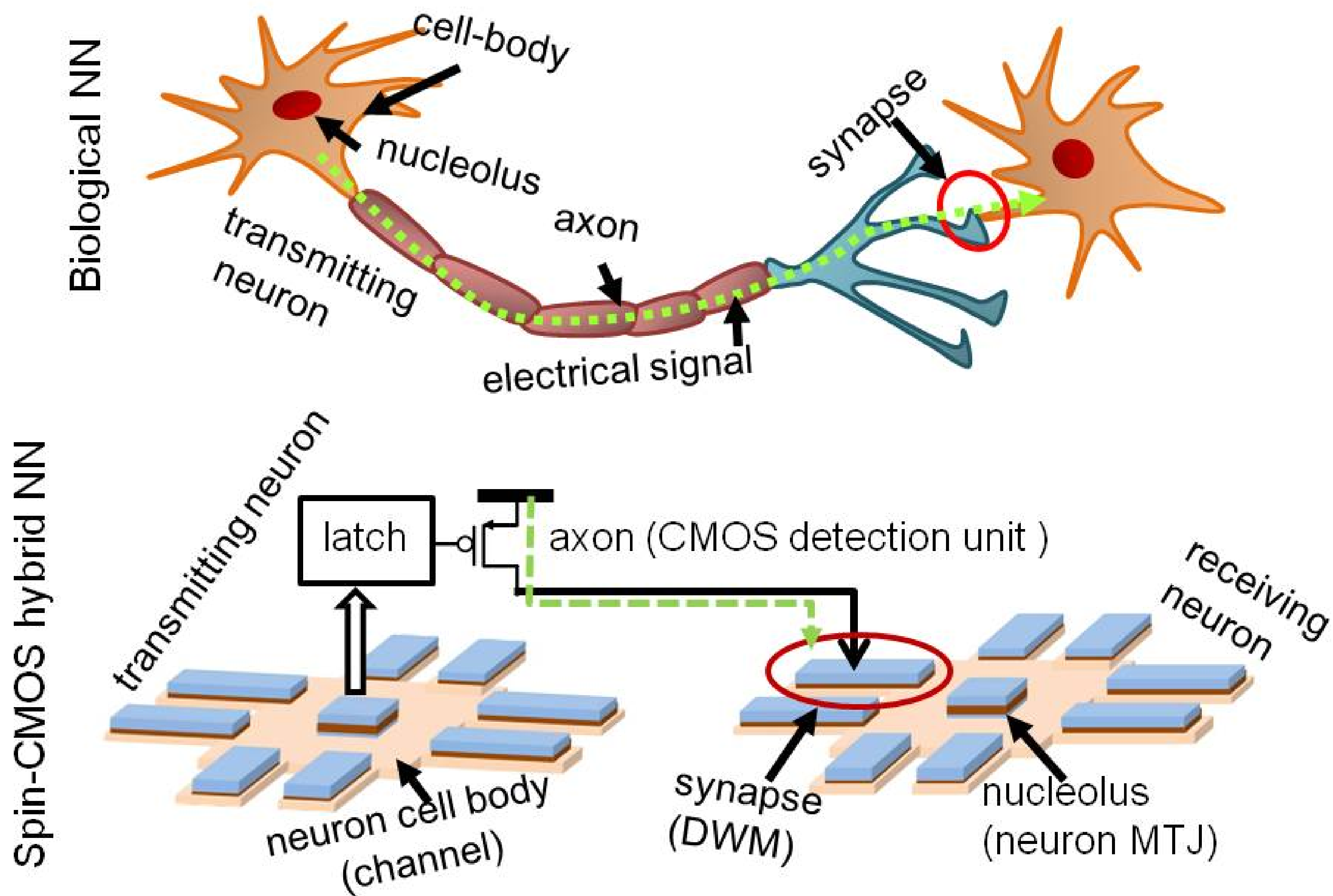
Device level Programmability using Domain Wall Magnet as Synapse





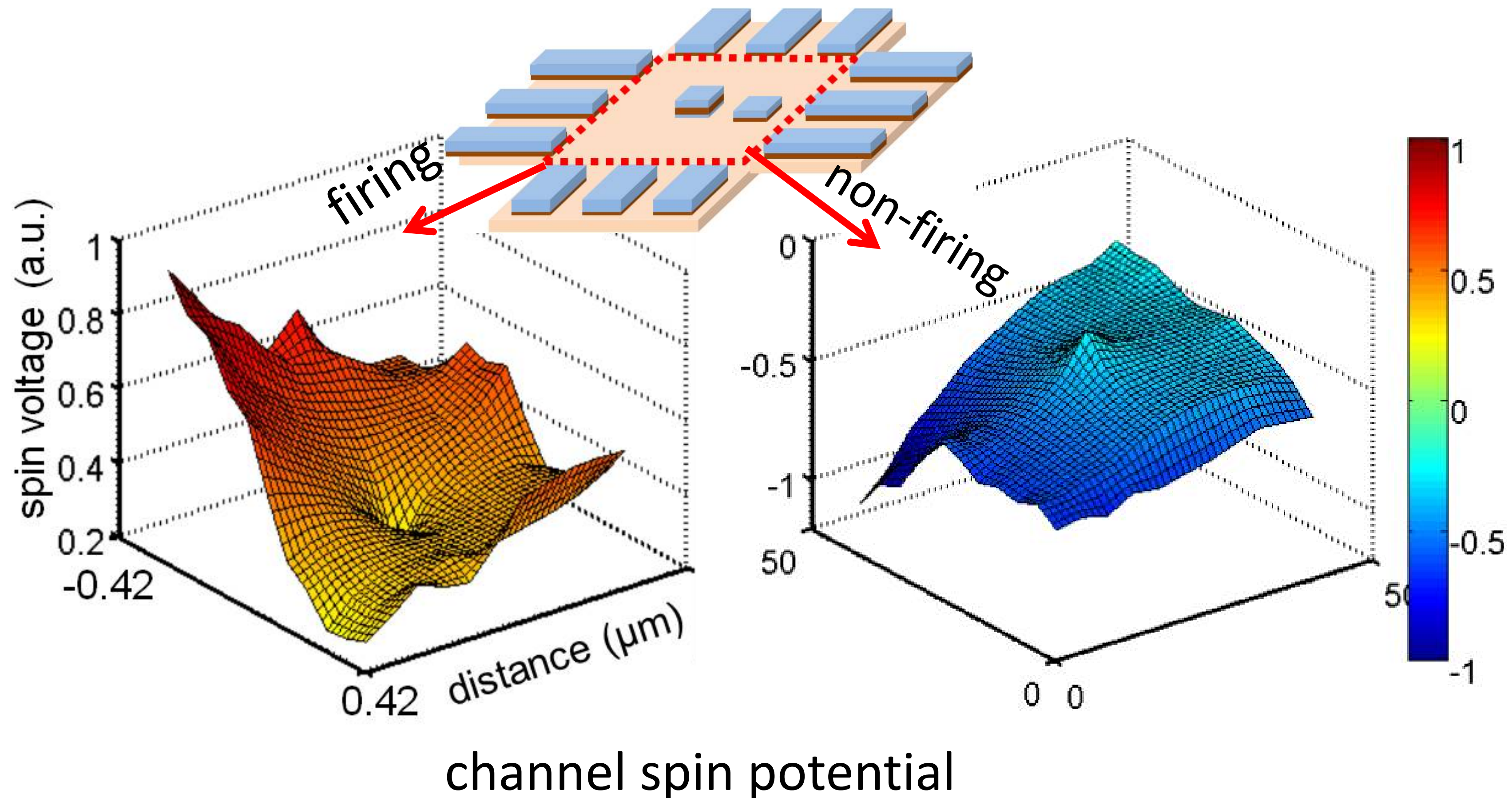
Neuron with small number of programmable DWM inputs can be employed to realize configurable data processing array of cellular neurons

Drawing Analogy with Biological Neural Network!



DWM Based Neuron-Synapse Unit: Modeling

Relative spin potential in the 2-D channel for neuron with 24 input synapses and charge current ~10μA per synapse

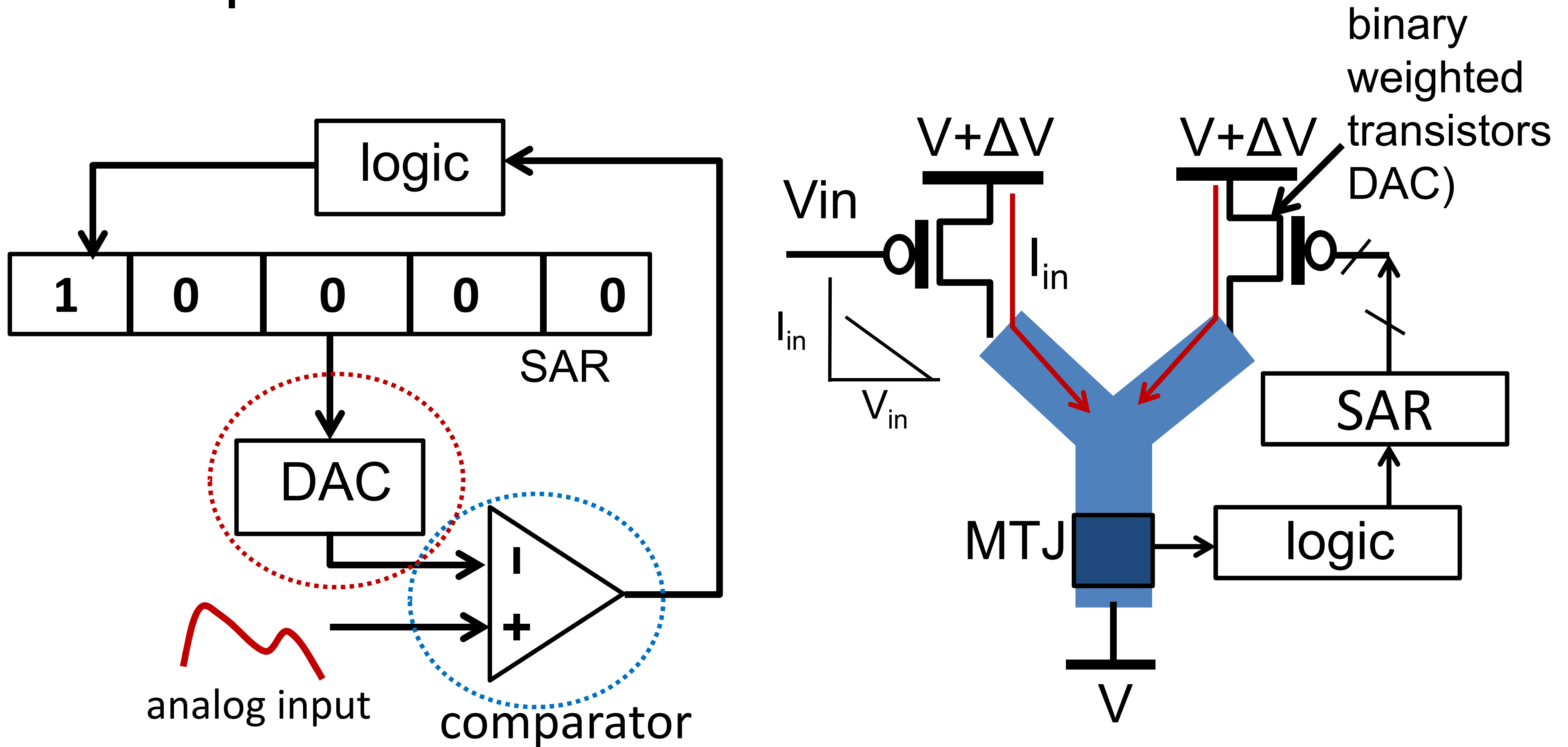


channel spin potential

Neuron is simulated using self consistent solution of 2-D spin transport in channel and LLG for magnets

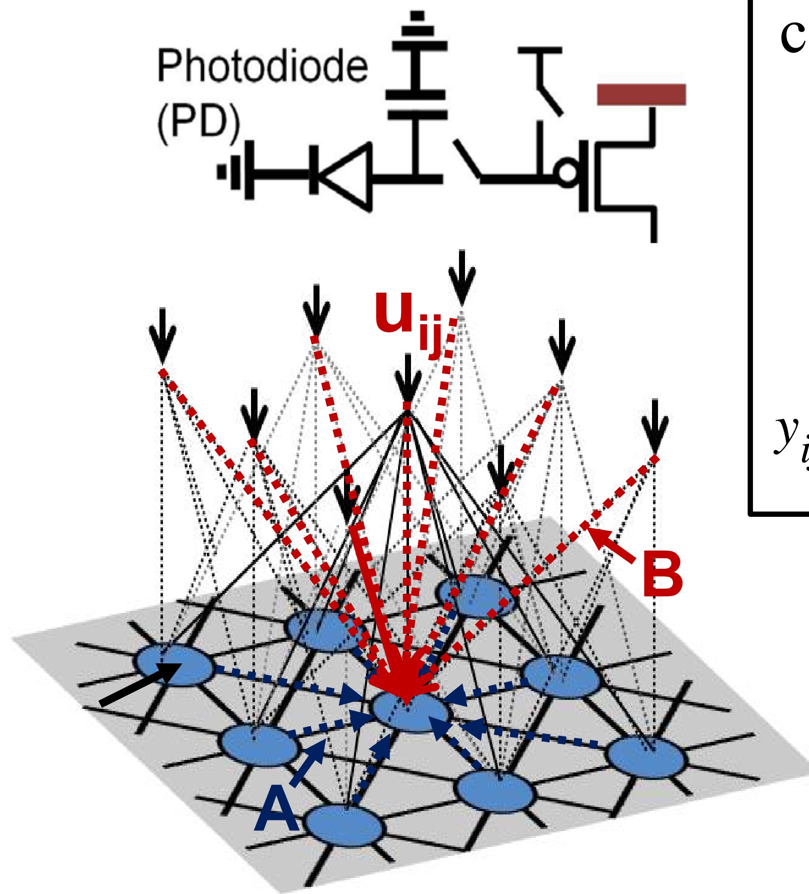
Application Examples

Example : Ultra Low Power SAR-ADC



➢ SAR ADC employs recursive evaluation akin to CNN equation and hence can be implemented using the bipolar spin neuron

Ultra low energy Analog signal acquisition and processing



cell state equation for Discrete-Time CNN

$$x_{ij}(n) = \sum_{(k,l)\in N(i,j)} A(i,j;k,l).y_{kl}(n) + \sum_{(k,l)\in N(i,j)} B(i,j;k,l).u_{kl}(n) + z(i,j)$$

$$y_{ij}(n) = f'(x_{ij}(n-1)) = \begin{cases} 1 & \text{if } x_{ij}(n-1)>0 \\ 0 & \text{if } x_{ij}(n-1)<0 \end{cases}$$

X(n) : cell state at n_{th} time step

A: 3x3 feedback template

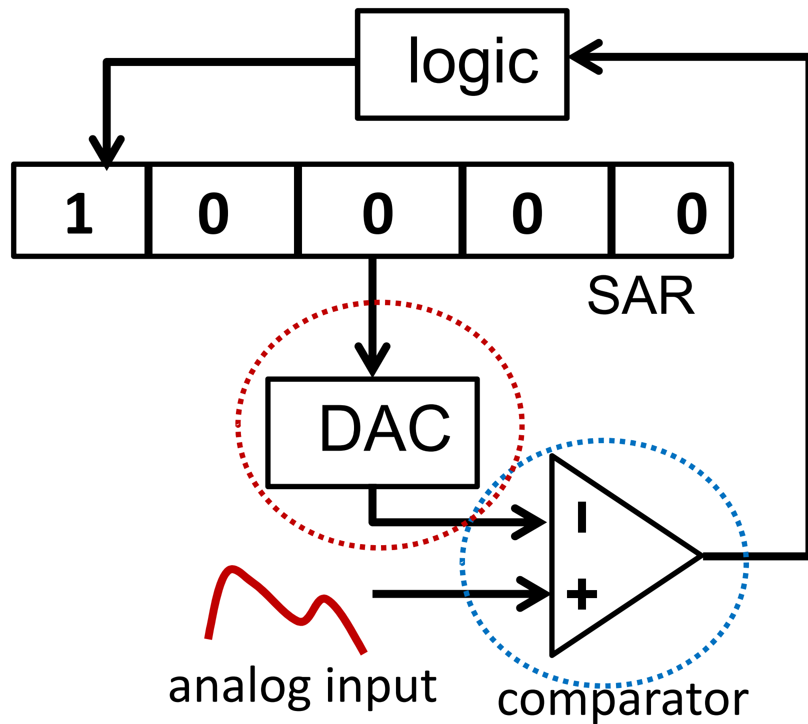
B: 3x3 input template

U(n) :3x3 neighborhood input at T= n

Z : cell bias; y(n): cell output at T=n

Hardware based on Cellular neural networks can be employed in several image processing applications

Example : Ultra Low Power SAR-ADC

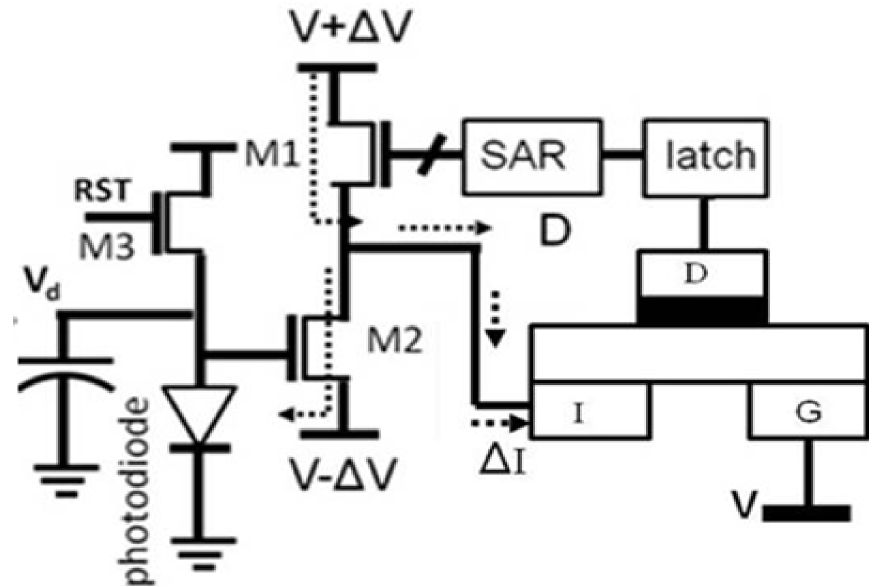


$$x_{ij}(n) = \sum_{(k,l)\in N(i,j)} A(i,j;k,l).y_{kl}(n) +$$

=0 for k≠i, l≠j

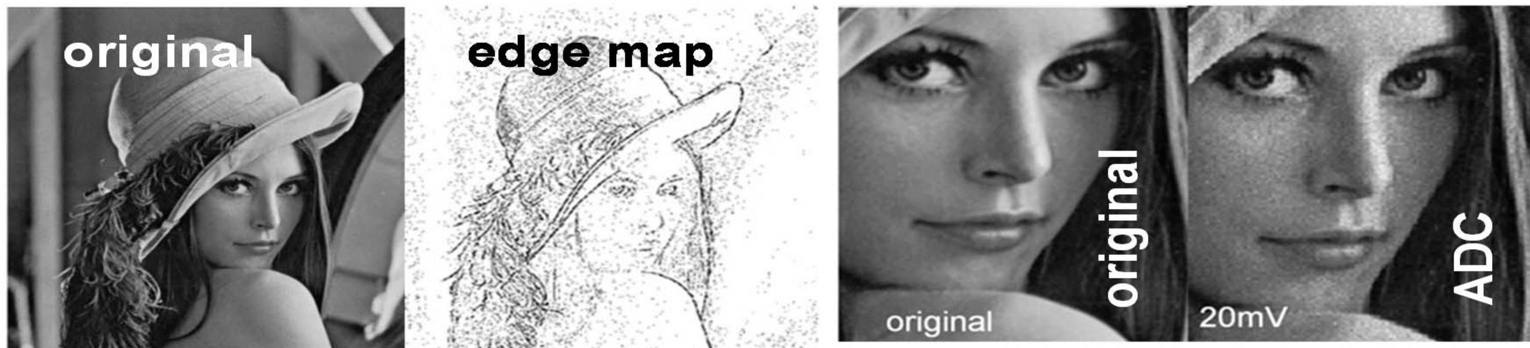
$$\sum_{(k,l)\in N(i,j)} B(i,j;k,l).u_{kl}(n) + z(i,j)$$

=0 for k≠i, l≠j



➢ SAR ADC employs recursive evaluation akin to CNN equation and hence can be implemented using the bipolar spin neuron

Ultra low energy Analog Signal Acquisition and Processing: Performance



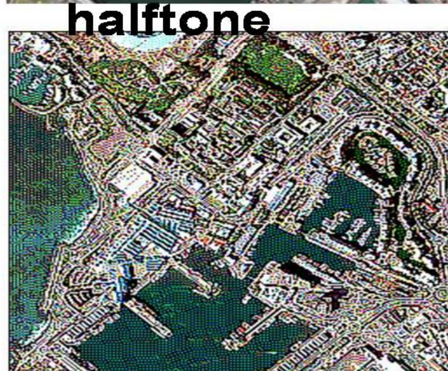


Table-I CMOS vs. spin based feature extraction IC

Ref	CMOS Tech	E(CMOS) /E(spin)
[23]	0.35μ	253
[24]	0.35μ	560
[25]	0.25μ	470

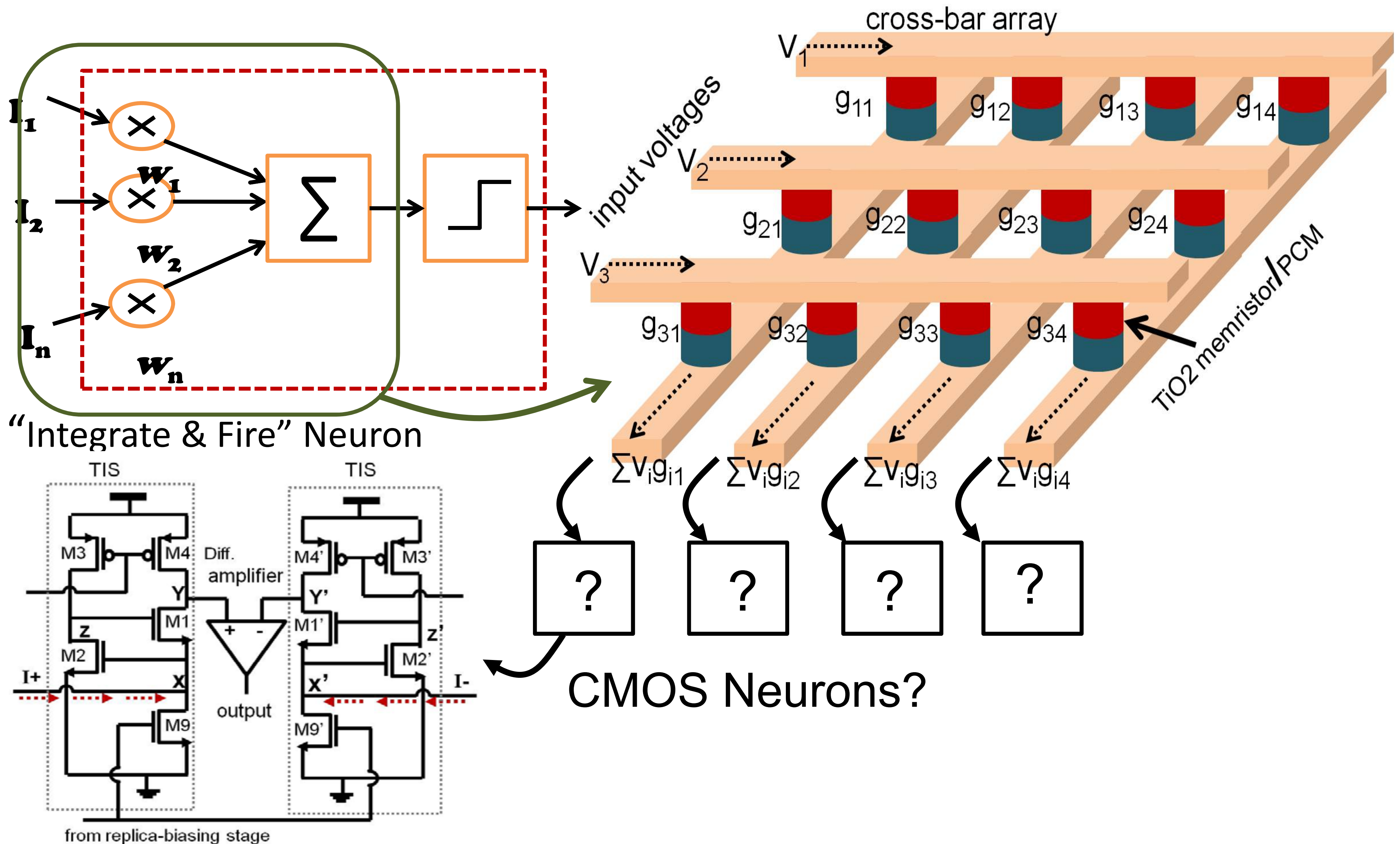
E= (total power) / (S^2x#Pixels x Fps)

Table-II CMOS vs. spin based ADC

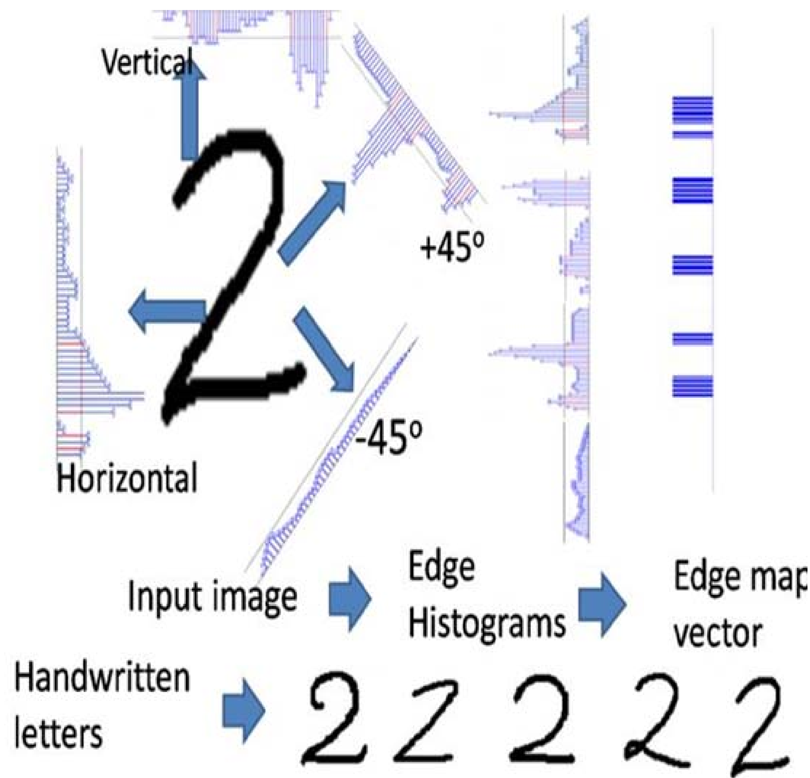
Ref	CMOS Tech	E(CMOS) /E(spin)
[26]	0.18μ	133
[27]	0.90μ	70
[28]	0.90μ	72

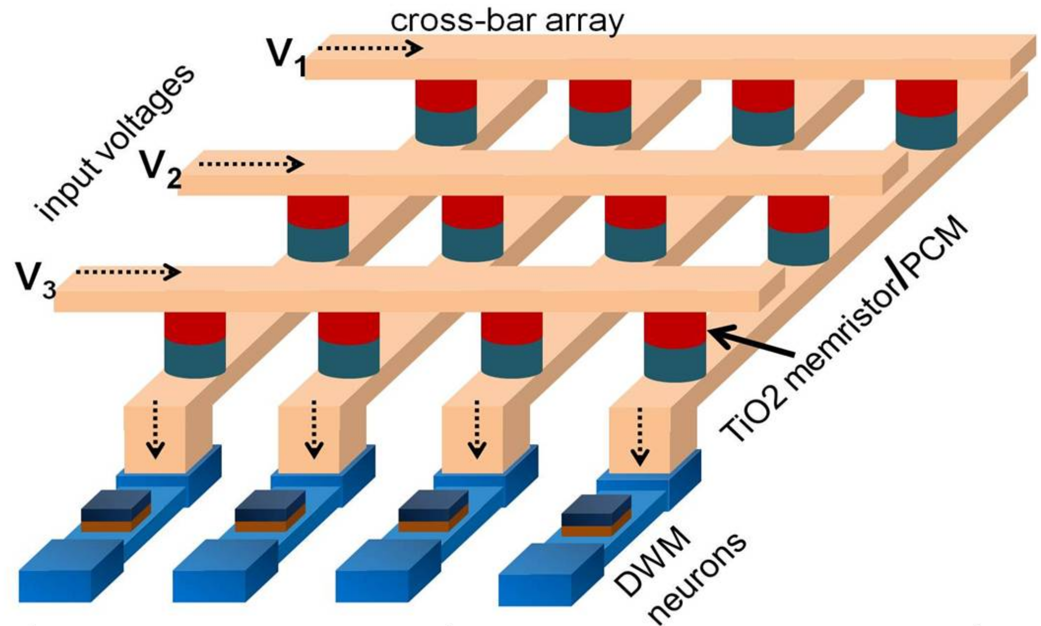
S : technology ratio
fps : frames/sec

Spin Based Neuron for Cross-Bar Neural Network



Neural Computing With Spin Neurons and Resistive Crossbar Memory





Network size	32x64	
Weight levels	16 (4 bits)	
PCM conductance	5K to 100K	
frequency	500MHz	
32 element analog associative memory using PCM cross-bar	Spin neuron:	0.06mW
	CMOS neuron	9mW

The spin based neuron unit achieves ~100x improvement in power consumption for cross bar ANN architecture Based on memristor/PCM

Interconnects

STT based Energy-Efficient Global Interconnects

STARnet

C-SPIN

Motivation:

❑ Global Interconnects like data-buses and memory bit-lines can account for more than 90% power for on-chip memory

❑ Emerging CMPs may dissipate ~50% power for global communication among memory and multiple processors

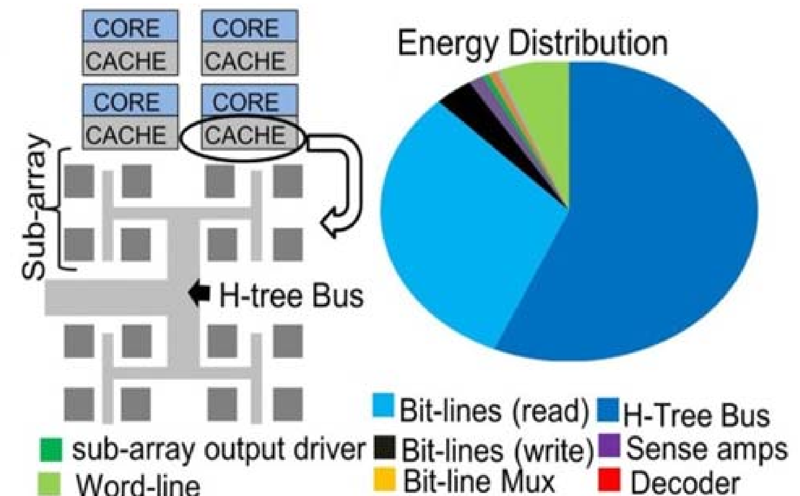
Technology/circuit solutions:

❑ On-chip transmission line

❑ CMOS Current-mode interconnects

❑ Low voltage swing

❑ Optical, plasmonic, graphene, CNT



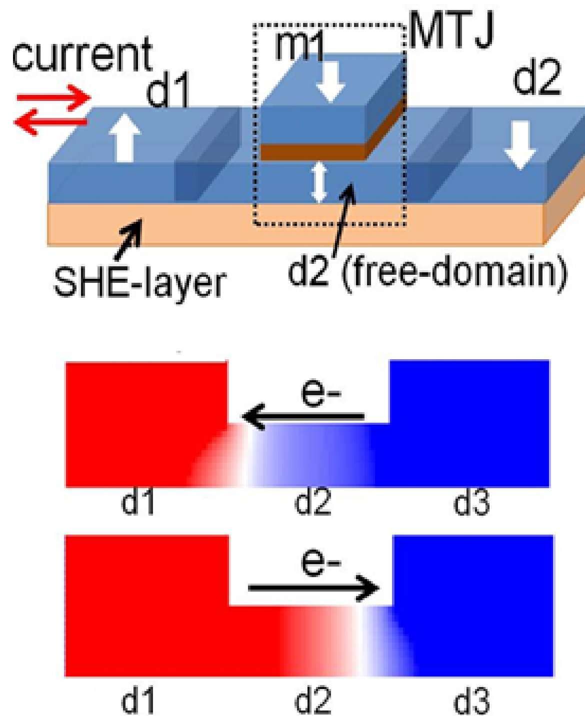
Our goals and approaches:

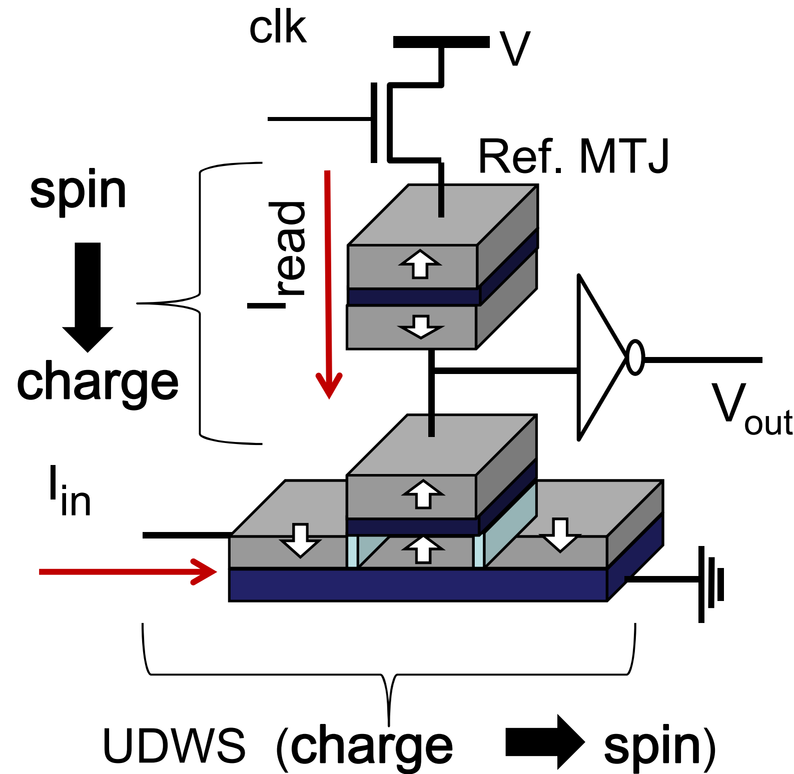
❑ Emerging spin-torque phenomena, like Spin Hall Effect (SHE), may lead to high-speed, low-voltage current-mode switches based on nano-scale magnets.

❑ We propose and analyze spin-torque switches in the design of energy-efficient and high-performance current-mode on-chip global-interconnects.

❑ Simulations show up to two order of magnitude higher energy-efficiency

Unipolar Domain Wall Switch for Interconnect



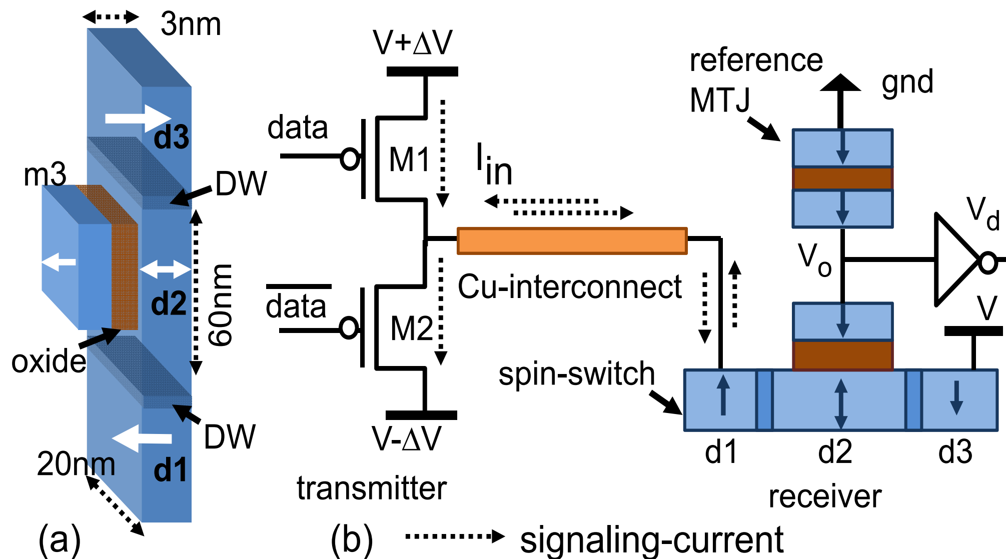


Unipolar Domain-Wall Switch

DWS as a trans-impedance converter

- ❑ DWM motion (with SHE assist can be used to realize a two-terminal current – mode STT switch
- ❑ Such a switch can convert an ultra-low voltage current-mode input signal into full swing output voltage in **two steps**: **charge to spin conversion through DW-motion , followed by spin-to charge conversion through MTJ**

Interconnects Using Spin-Torque Switches



Interconnect design using domain wall switch

- Global interconnects may account for large portions of total power in future processors.
- Emerging STT phenomena may facilitate high-speed (100fs), low-voltage current-mode magnet-switching along with efficient transimpedance conversion.

For 2Gbps signaling over a 10mm on chip interconnect:

Conventional CMOS:

Voltage mode: $0.5CV^2 =$ 2.5pfx 0.0625 = **150fJ**

Current-mode: 90fJ

S. Lee et al., ISSCC 2013

Spintronic Current-mode:

$E_{signaling} = I_{switch}\, T_{bit}\, \Delta V + I_{MTJ}\, V_{MTJ} T_{bit} + T_{bit}\,(P_{inverter} + P_{driver})$

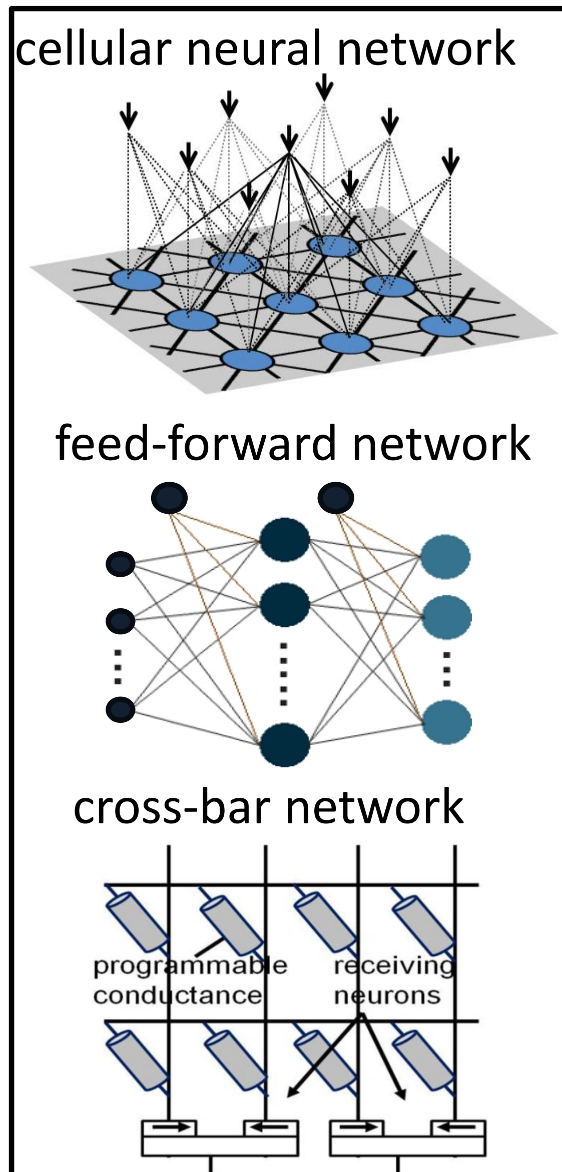
= (20μA x 0.5ns x 100mV)
+(0.7μA x 0.6V x 0.5ns)
+ (0.5ns x 0.7μW)

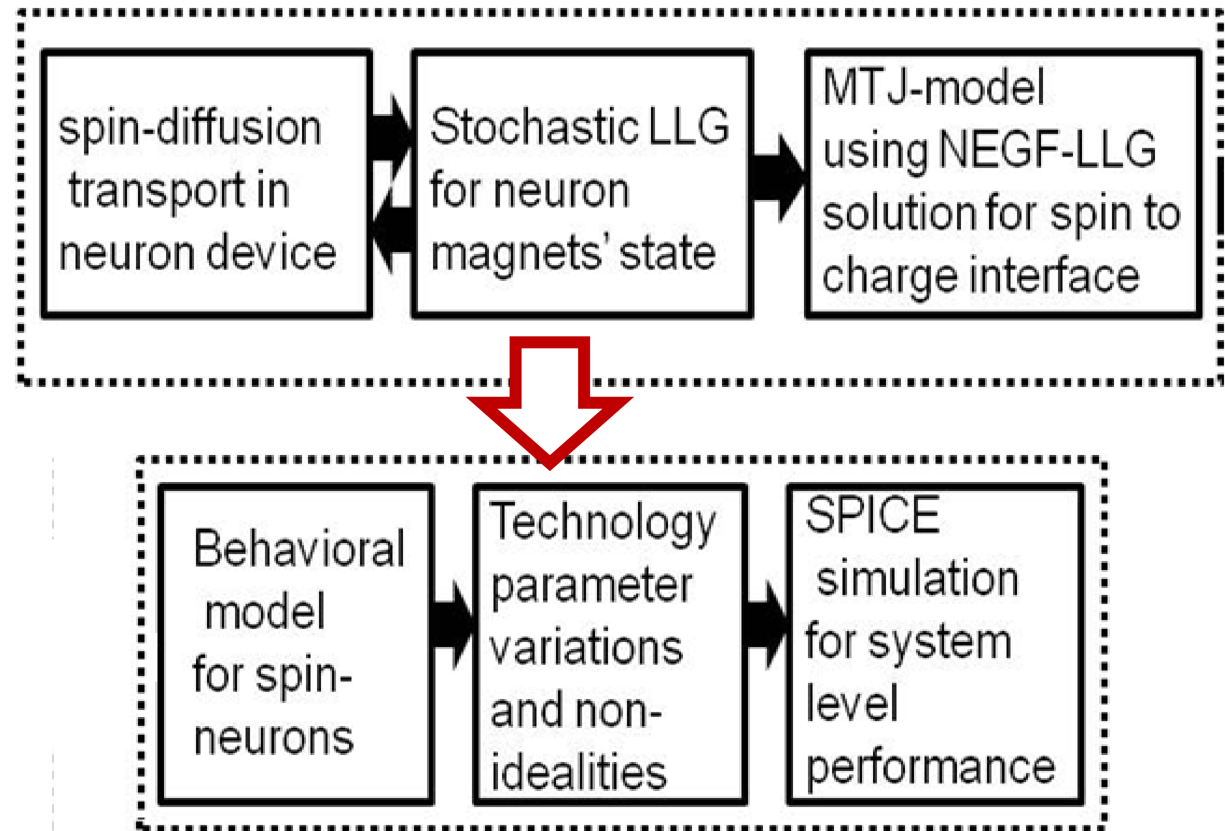
~1fJ

Sharad , Roy , EDL., 2013
Sharad , Roy , IEDM, 2013

- **STT switches can be employed for ultra-low energy and compact current mode global interconnects**

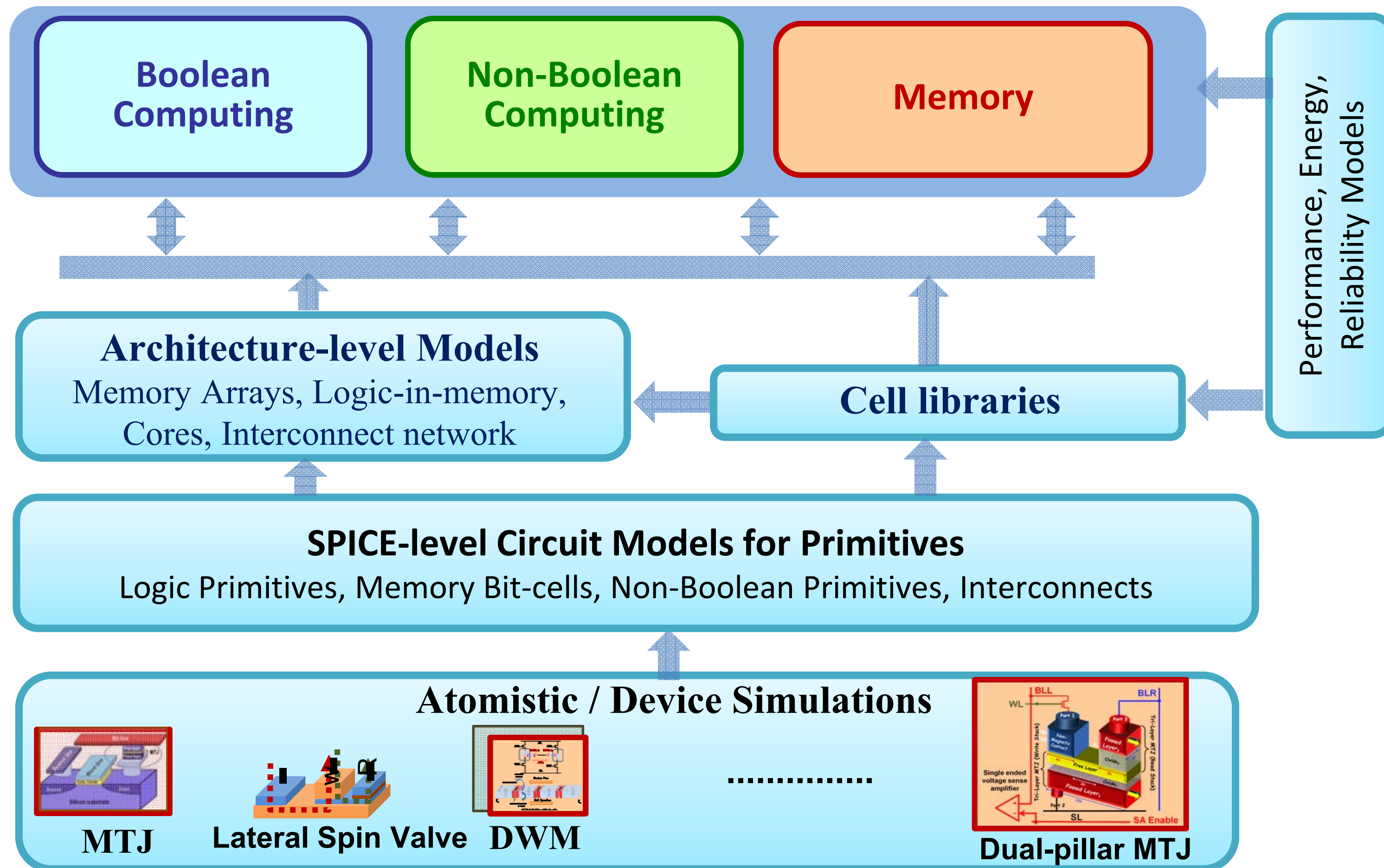
Device-Circuit Co-Simulation-Framework





We employ Device-Circuit- Architecture Co-Simulation-Framework to evaluate the performance of spin based heterogeneous neuromorphic architectures

Modeling, Simulation, and Evaluation Framework



Predictive modeling infrastructure will be co-developed with theme 4

Summary

- Spin-torque memories for on-chip applications are becoming a reality
- Spin-torque devices such as LSVs and DWMs show potential for class of applications that CMOS is not efficient at implementing such as neuromorphic designs, associative computing, semantic analysis, etc.
- Potential for large improvement in energy consumption

References (mostly our work)

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