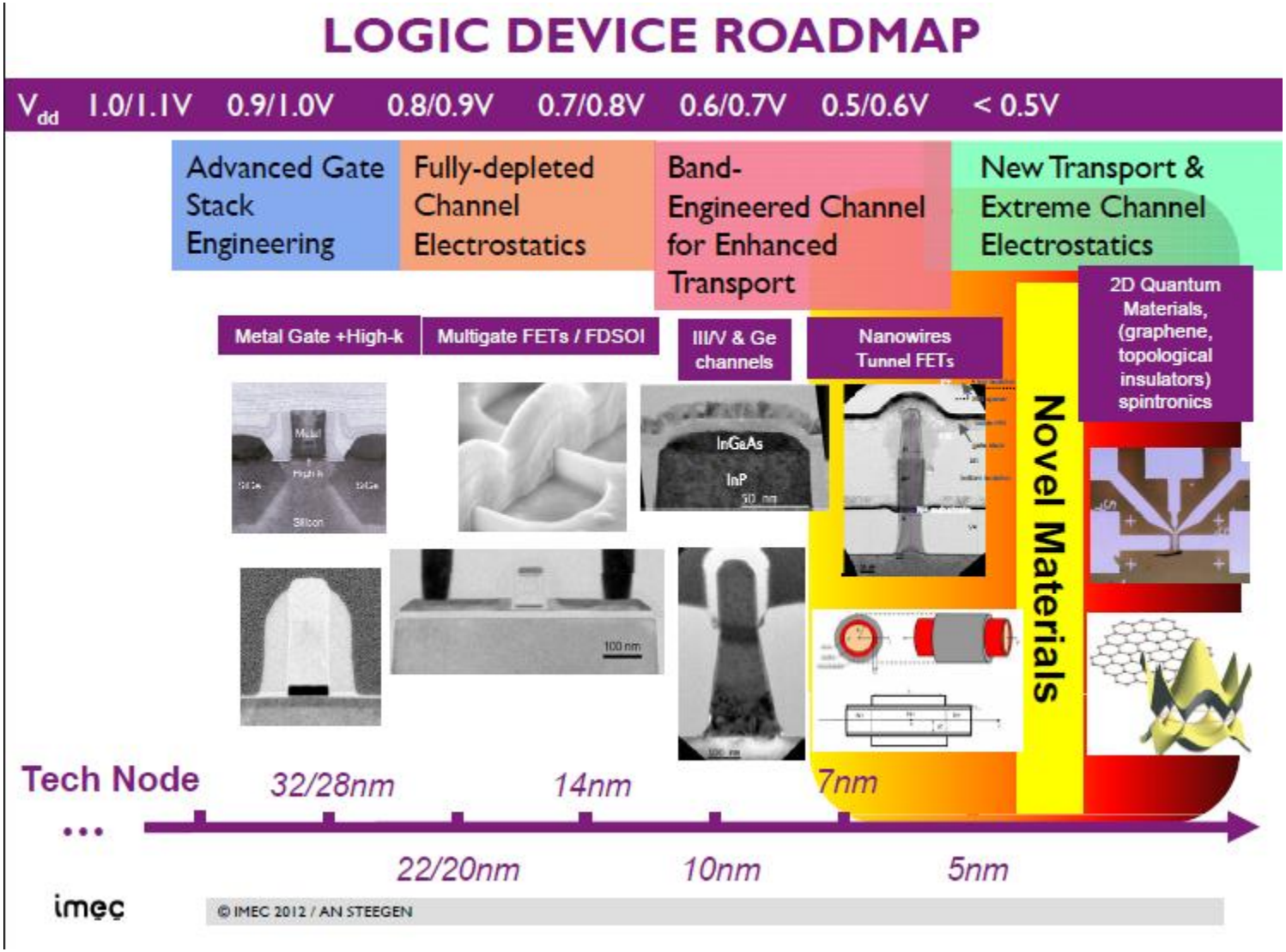
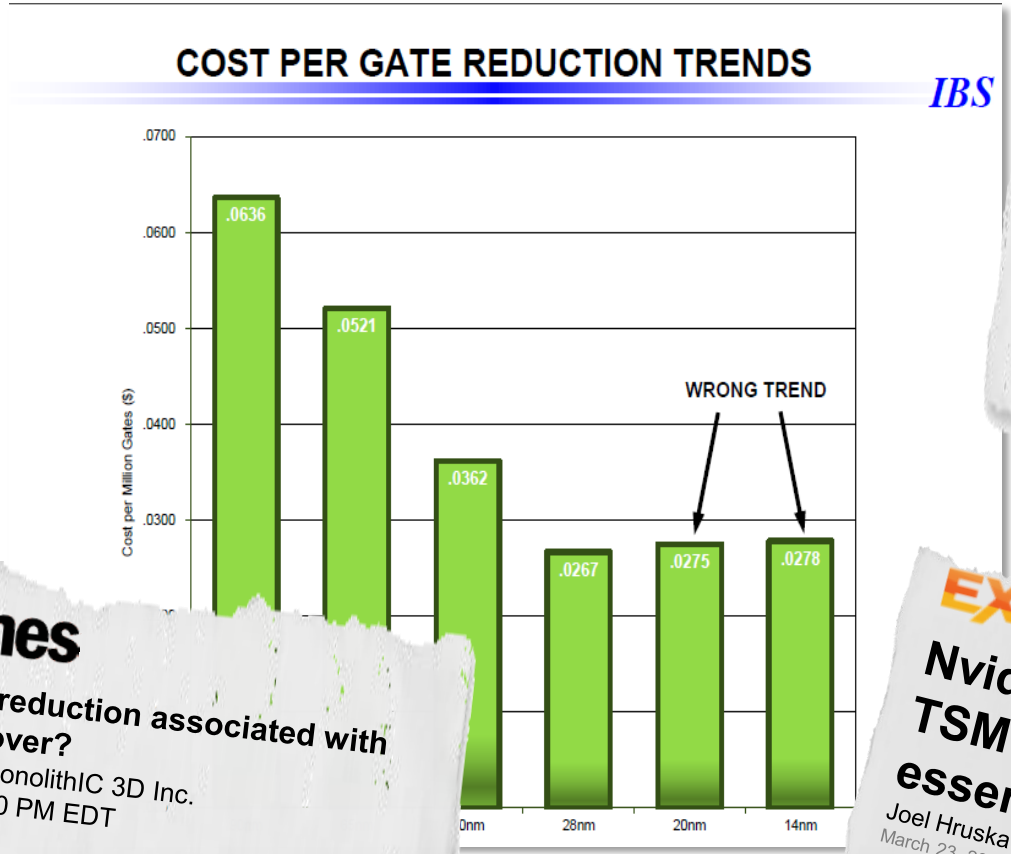
The All Programmable SoC FPGA for Networking and Computing in Big Data Infrastructure

Ivo Bolsens,
Senior Vice President & CTO

Moore's Law: The Technology Pipeline



Industry Debates on Transistor Cost



EE Times

TSMC raises capex to record $8.5 billion, pulls in 20-nm

Peter Clarke
4/26/2012 12:23 PM EDT

LONDON – Taiwan Semiconductor Manufacturing Co. Ltd. has raised its planned capital expenditure for 2012 to between $8 billion and $8.5 billion. The move accompanied the announcement of first quarter financial results and strong second quarter outlook by the foundry.

EE Times

Is the cost reduction associated with IC scaling over?

Zvi Or-Bach, MonolithIC 3D Inc.
7/16/2012 12:20 PM EDT

The last 50 years of the semiconductor industry have been all about the manifestation of Moore's Law with regard to the dimensional scaling of Integrated Circuits (ICs). As consumers of electronic devices, we all love to see better products at a lower cost with each and every new product cycle. But now storm clouds are forming,

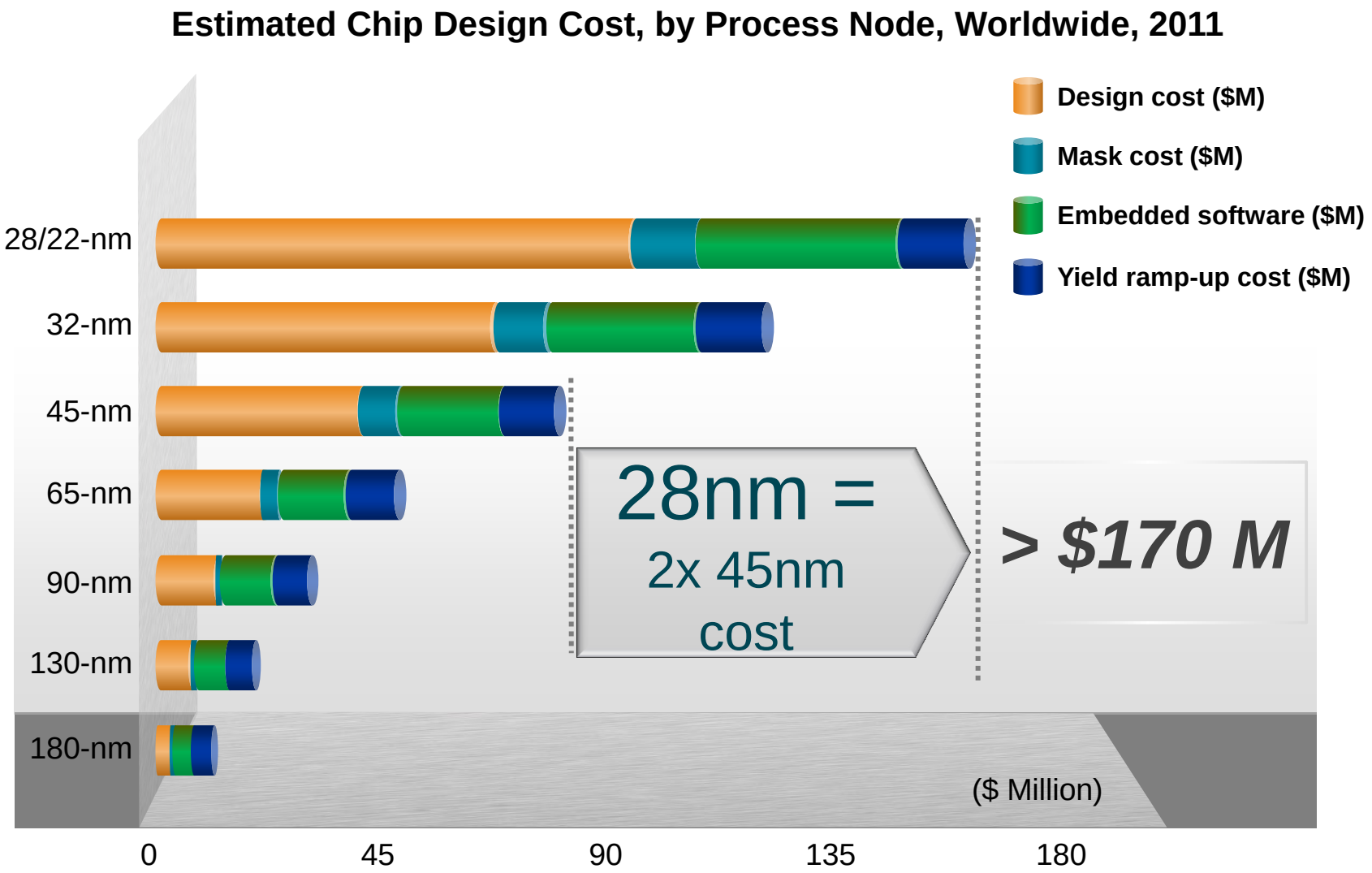
EXTREMETECH

Nvidia deeply unhappy with TSMC, claims 20nm essentially worthless

Joel Hruska
March 23, 2012 at 12:13 pm

One of the unspoken rules of customer-foundry relations is that you virtually never see the former speak poorly of the latter. Only when things have seriously hit the fan do partners like AMD or Nvidia

Design Cost



Growing Problems for ASIC & ASSP Offerings

>50% of Top 16 ASSP Vendors Losing Money

Communications ASSP Vendors	Operating Margin			
	2009	2010	2011	2012 (proj)
A	21%	32%	26%	23%
B	16%	15%	5%	23%
C	12%	33%	31%	23%
D	19%	23%	26%	18%
E	2%	14%	13%	10%
F	-25%	-1%	8%	11%
G	15%	25%	18%	10%
H	12%	19%	10%	1%
I	-21%	6%	-1%	-23%
J	-21%	-2%	-11%	-33%
K	-5%	15%	-5%	-19%
L	-4%	2%	-6%	1%
M	-22%	-18%	-13%	-11%
N	-15%	-7%	-	-
O	-15%	1%	-18%	-24%
P	-11%	-6%	-47%	-98%

Source – Public reports, Xilinx estimates

Growing ASSP Gaps

- Eroding customer confidence in vendors
- High cost burden from over design for diverse needs
- No ability to differentiate or customize

Trend Mobile Infrastructure: Scalable Platforms

Capacity

Indoor

Residential Femto

4-16 Users
<100mW

Home

Enterprise Femto

30-60 Users
<250mW

Office

Picocell

30-200 Users
<1W

Dense Indoor
(Malls, Transport Hubs)

Outdoor

Microcell

Urban Infill

~200 Users
<1-10W
Single Sector

Macrocell

Wide Area

~200 Users/ sector
20-100W
Multi-Sector

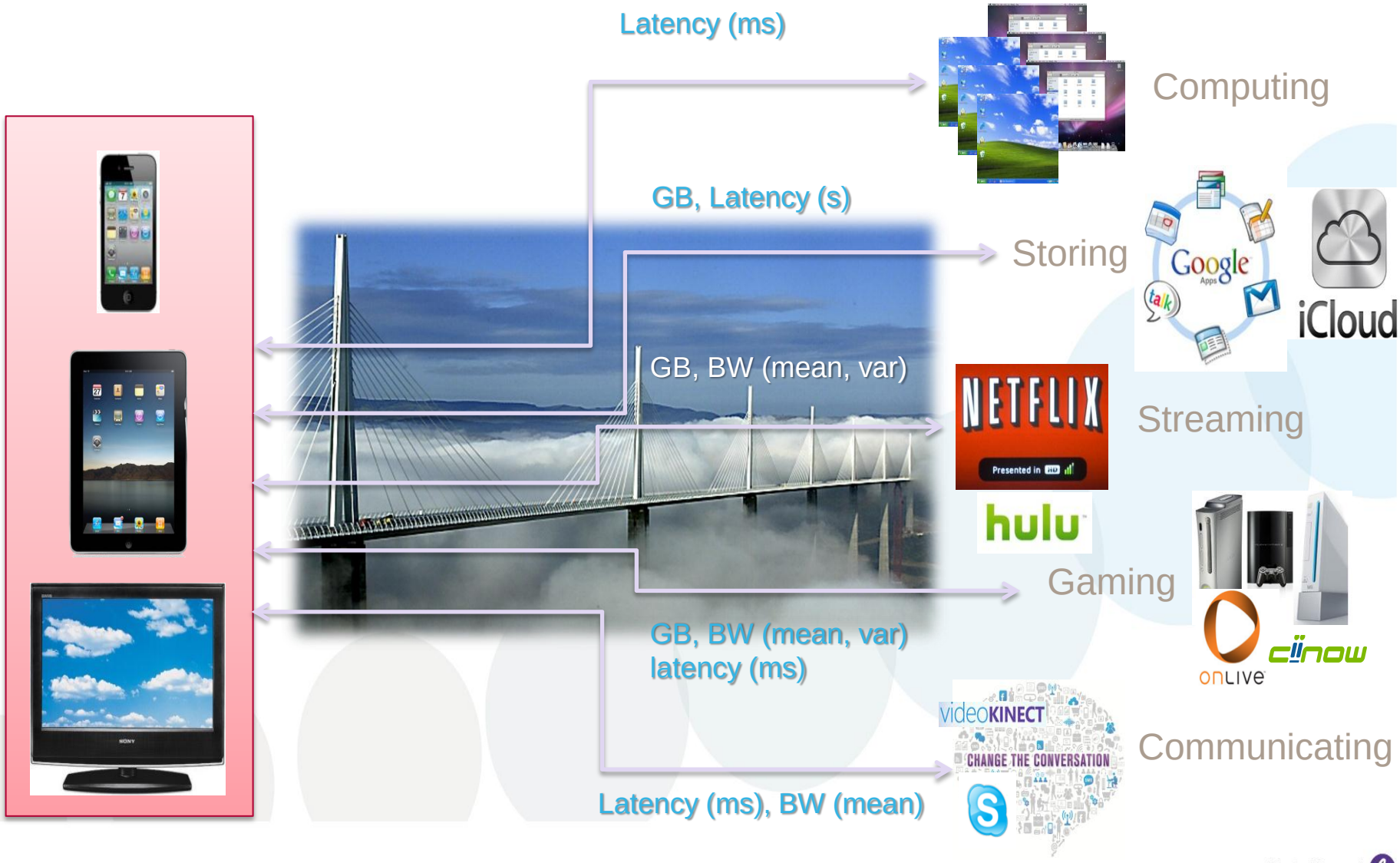
Macrocell + Active Antennas

Wide Area

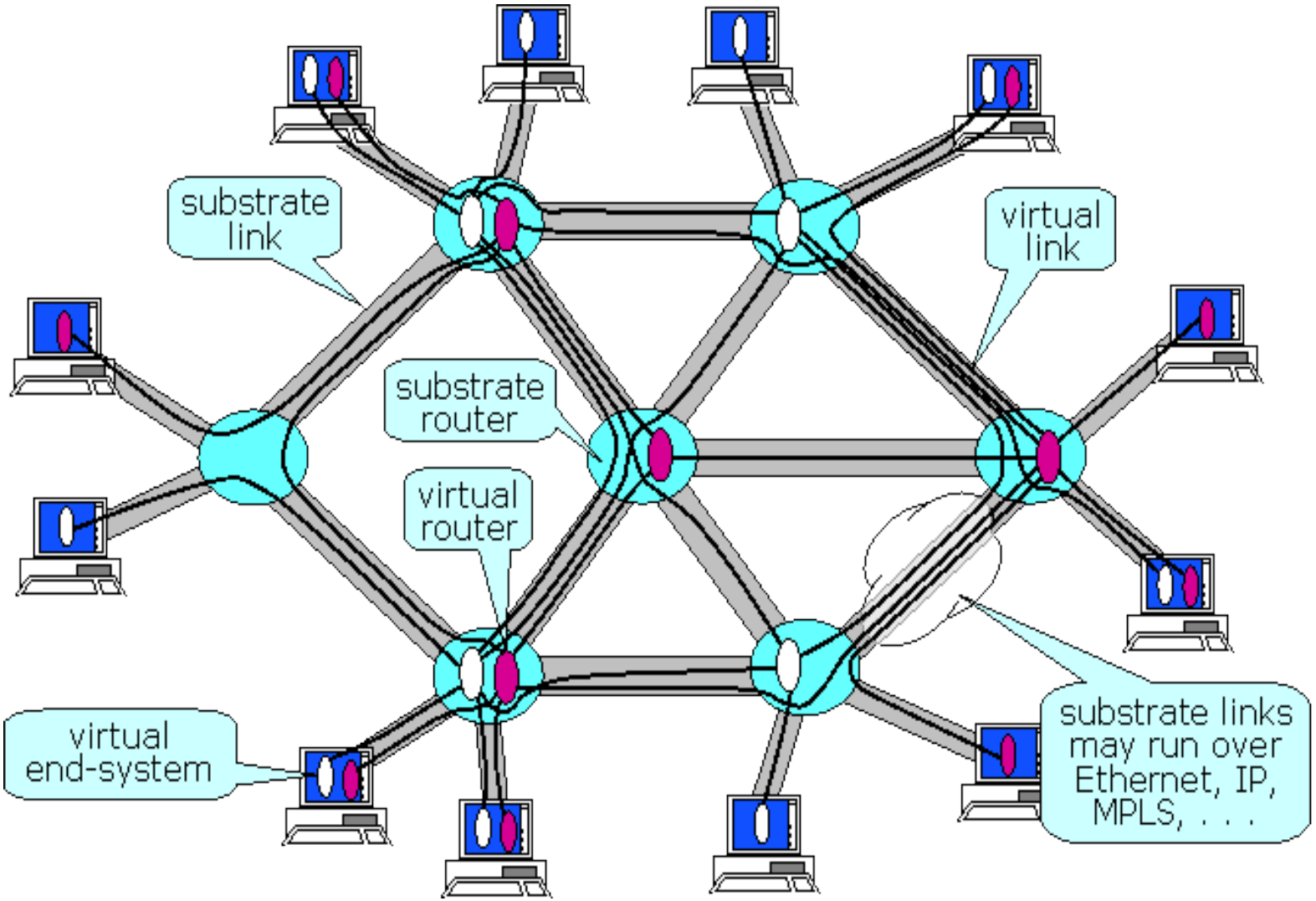
2-3x Data Capacity of RRU

Coverage

Trend Services : Different Figures of Merit

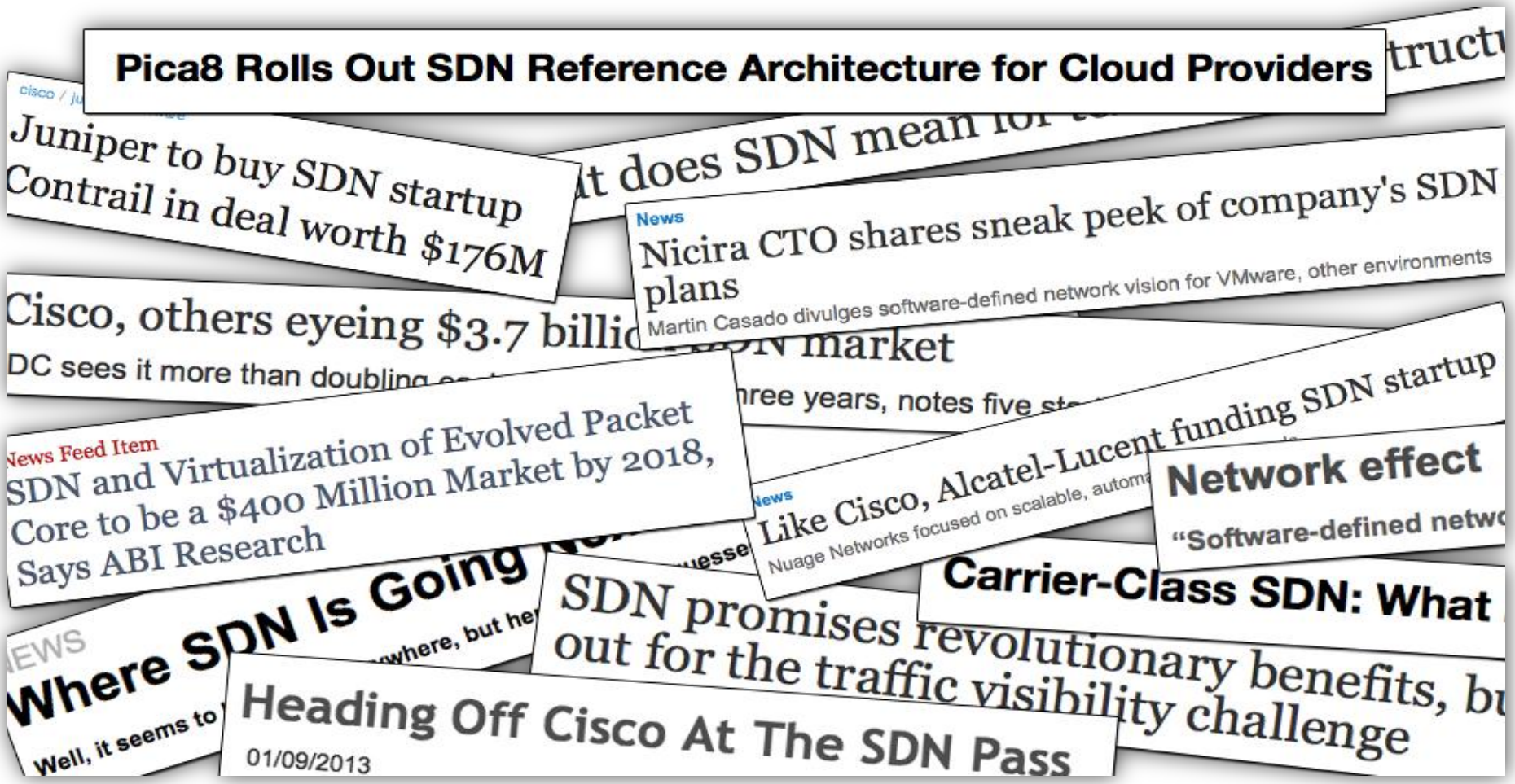


Trend Wired Infrastructure: Software Defined Networks



Slide credit: From “Virtualizing the Net” by Jon Turner (2004)

Software Defined Networking gains industry mindshare



The best thing about OpenFlow or SDN, is that it's brought back a new hope to networking. Networking is cool again- Jayshree, CEO - Arista Networks

Trend Data Center Infrastructure: Cloud Computing

Big Data

Increasing Volume, Velocity, and Variety

Low power

Reduce operation and cooling costs

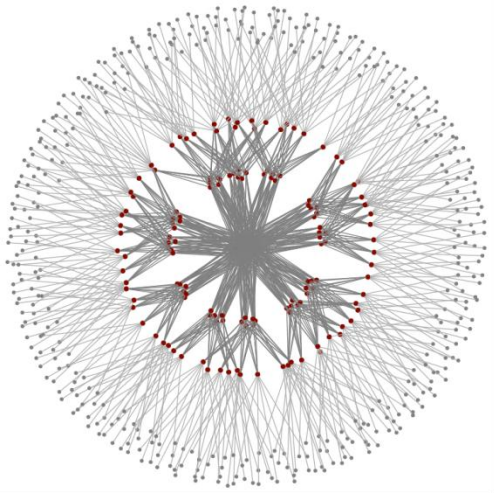
Security

Both outside and inside

Impact of trends
(1) Networking

New network fabrics

- Faster, Fatter, and Flatter



Software defined networking

- Software control plane
- Hardware data plane

Content-aware networking

- Deep packet inspection
- Enhanced security

Impact of trends
(2) Compute

ARM-based microservers

- Improved performance per watt

Hybrid SoC

- CPU+accelerators+fabric
- Cost and power reduction

Larger memory

- Hybrid NVRAM and DRAM
- Latency reduction

Impact of trends
(3) Storage

Specialized functions

- Compression, encryption, memcached

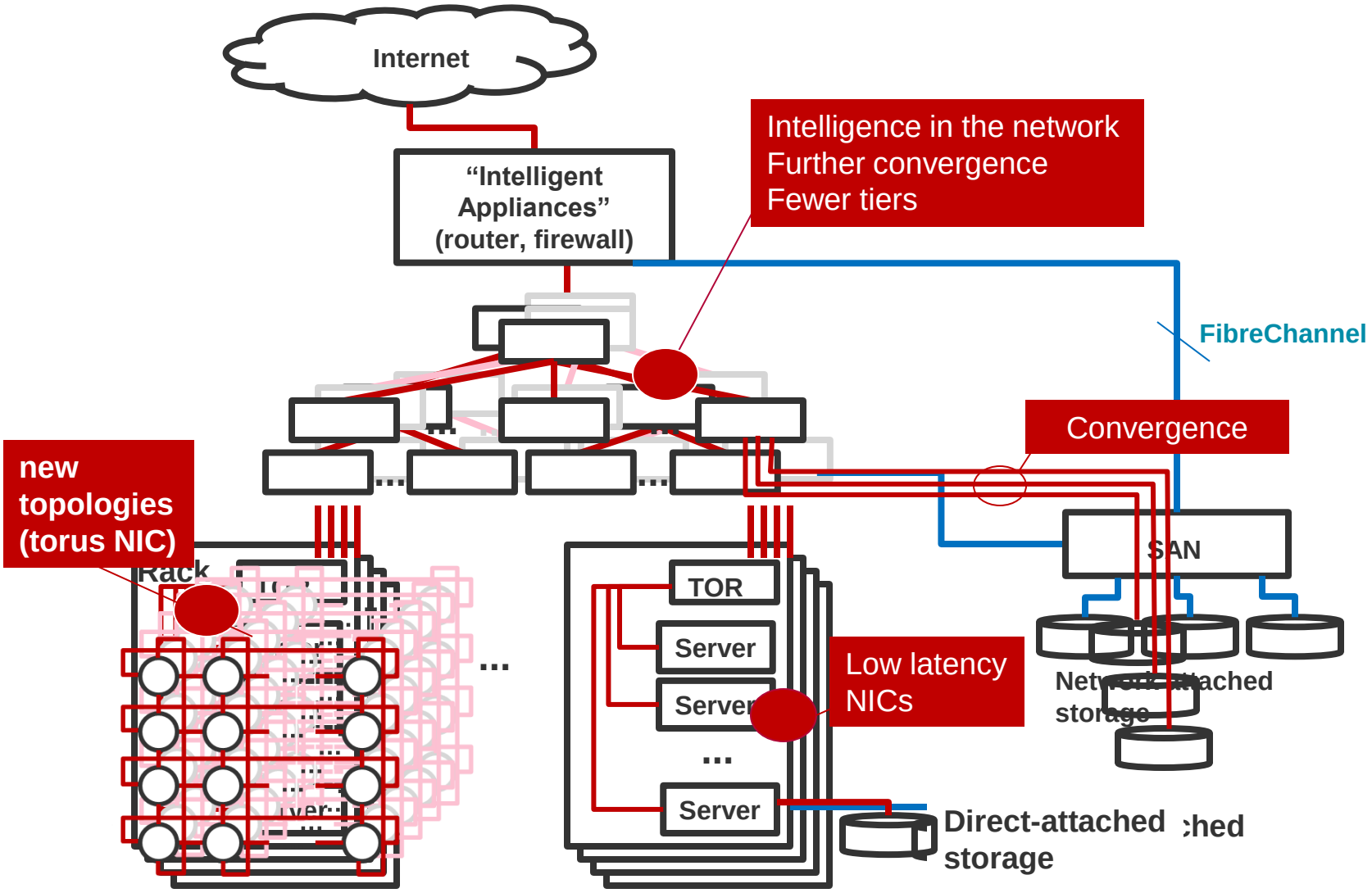
Custom SSD controllers

- Higher performance
- Reduced latency

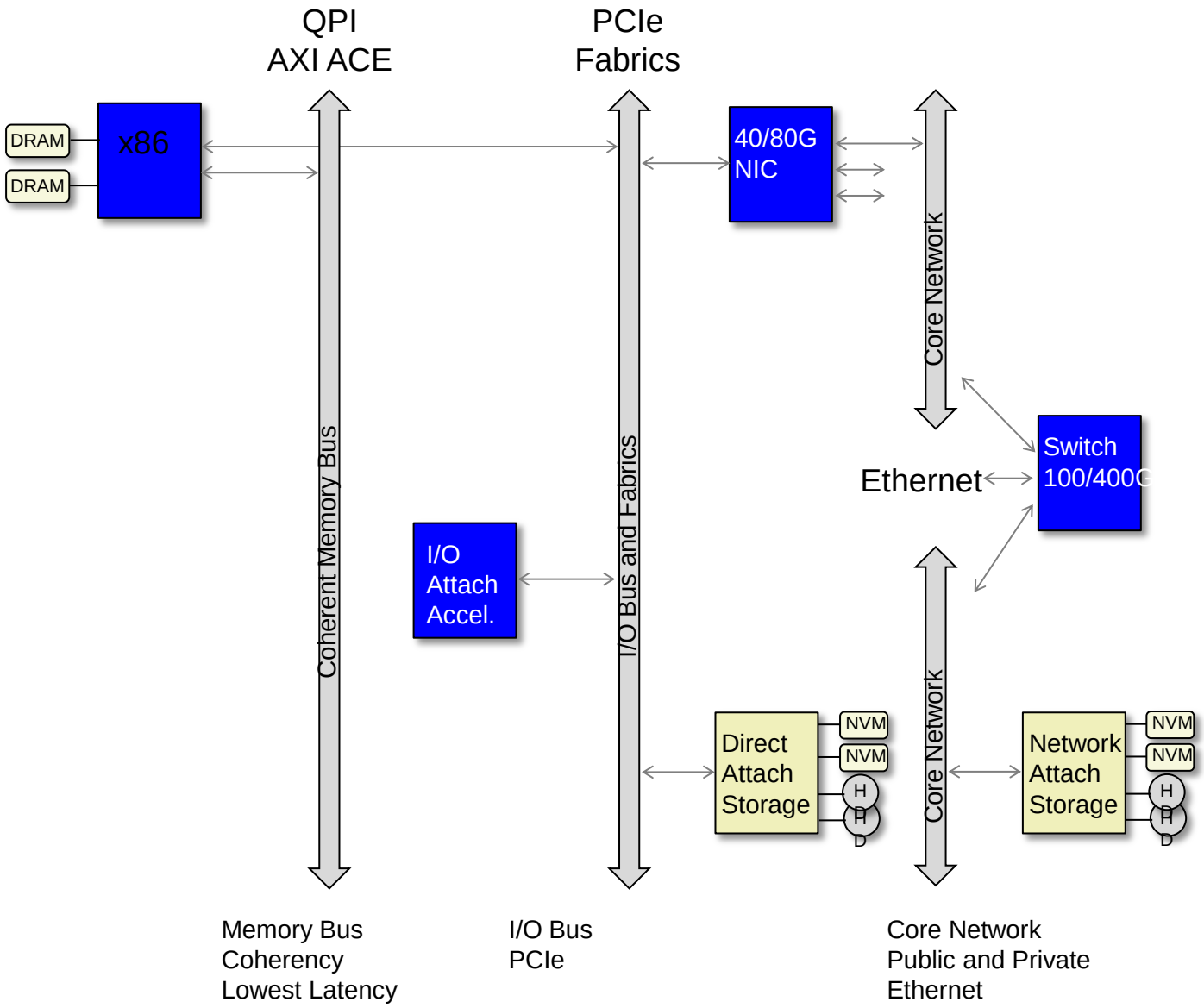
Data-aware storage

- Integrated database support
- Offload from processor

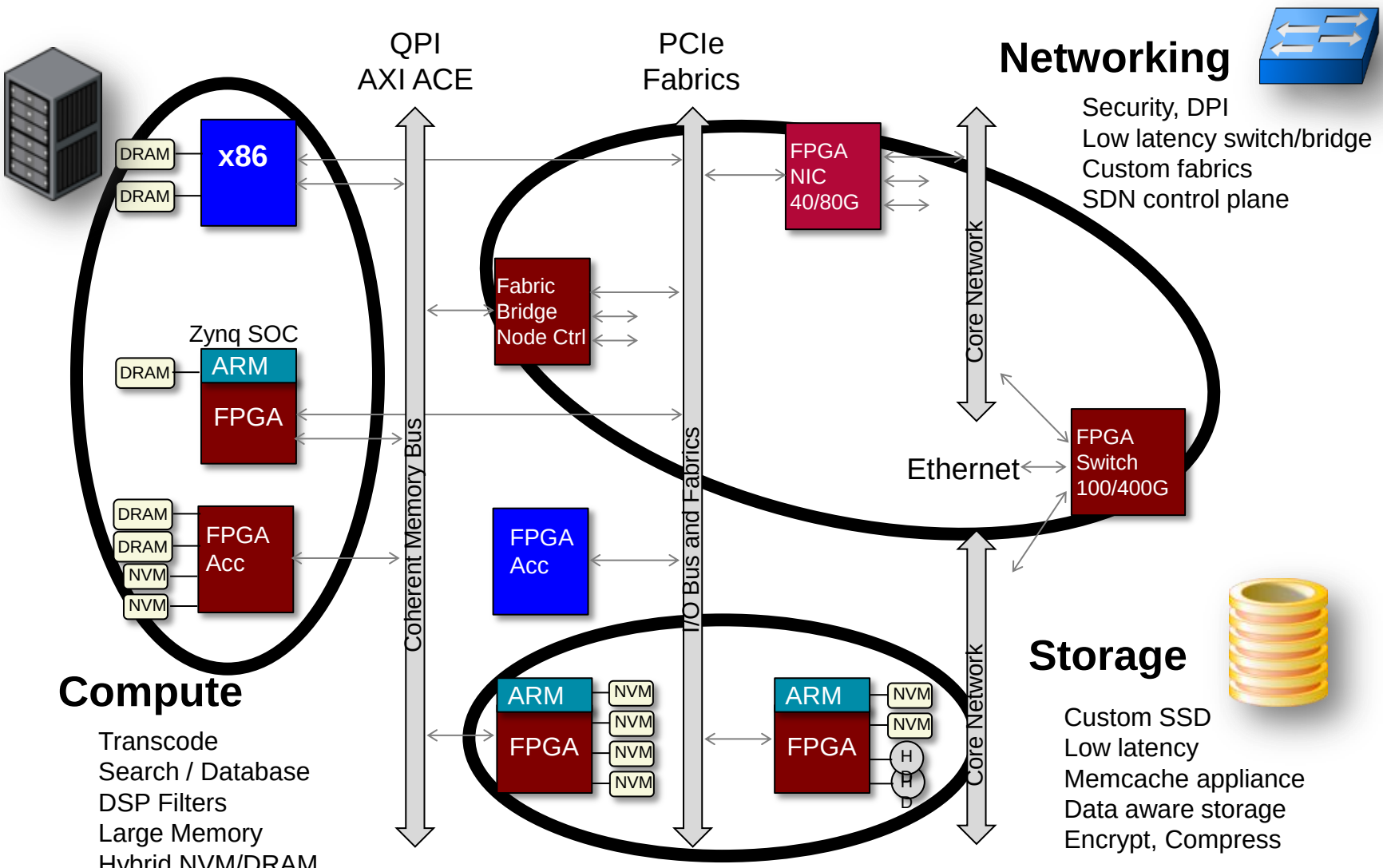
Future Data Centre Architecture



Generic Data Center



The New Data Center



Trend : More Intelligence in Embedded Systems

SMART Data Center Revolution

New Opportunities to Control Costs and Increase Strategic Advantage…

MACHINES THAT UNDERSTAND

embedded VISION ALLIANCE

Smart wireless networks to the rescue

Carriers are turning toward more intelligent network management…

Smart Factories

For factory management in the future, it will become essential to strive to implement smart capabilities…

The Next Big, Digital Economy; 'Smart Energy'

The energy market is undergoing a major transformation…

Page 17

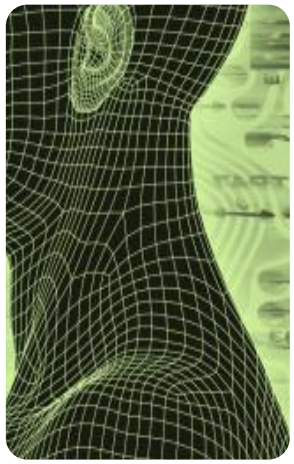
Programmable & Smart Across All Markets

	All Programmable	Smarter
 **Wireless Comms**	• Multiple Spectrums • Multiple Standards (**LTE**, 3G) • Multiple Levels of QoS	• Self Organizing Networks (**SON**) • Cognitive Radio • Smart Antenna
 **Wired Comms**	• Network Function Virtualization (**NFV**) • Multiple Stds (400Gb etc.) • Dynamic QoS Provisioning	• Context Aware Network Services • Self-Healing Networks • **Video** Caching at the Edge
 **Data Center**	• Software Defined Networks (**SDN**) • Multiple Stds (FCoE, iSCSI ...) • Config Storage (SAN, NAS, **SSD**…)	• Data Pre-Processing & **Analytics** • Virtualized Resource Optimization • Intelligent **Appliances**
 **Embedded**	• Changing Resolutions (MPixel, Fps) • Emerging Video Stds (**UHD**, 8K/4K) • Evolving Video Processing Algorithms	• Object Detection & Analytics • Automotive Collision Avoidance • Industrial Machine **Vision**

Industry Mandates

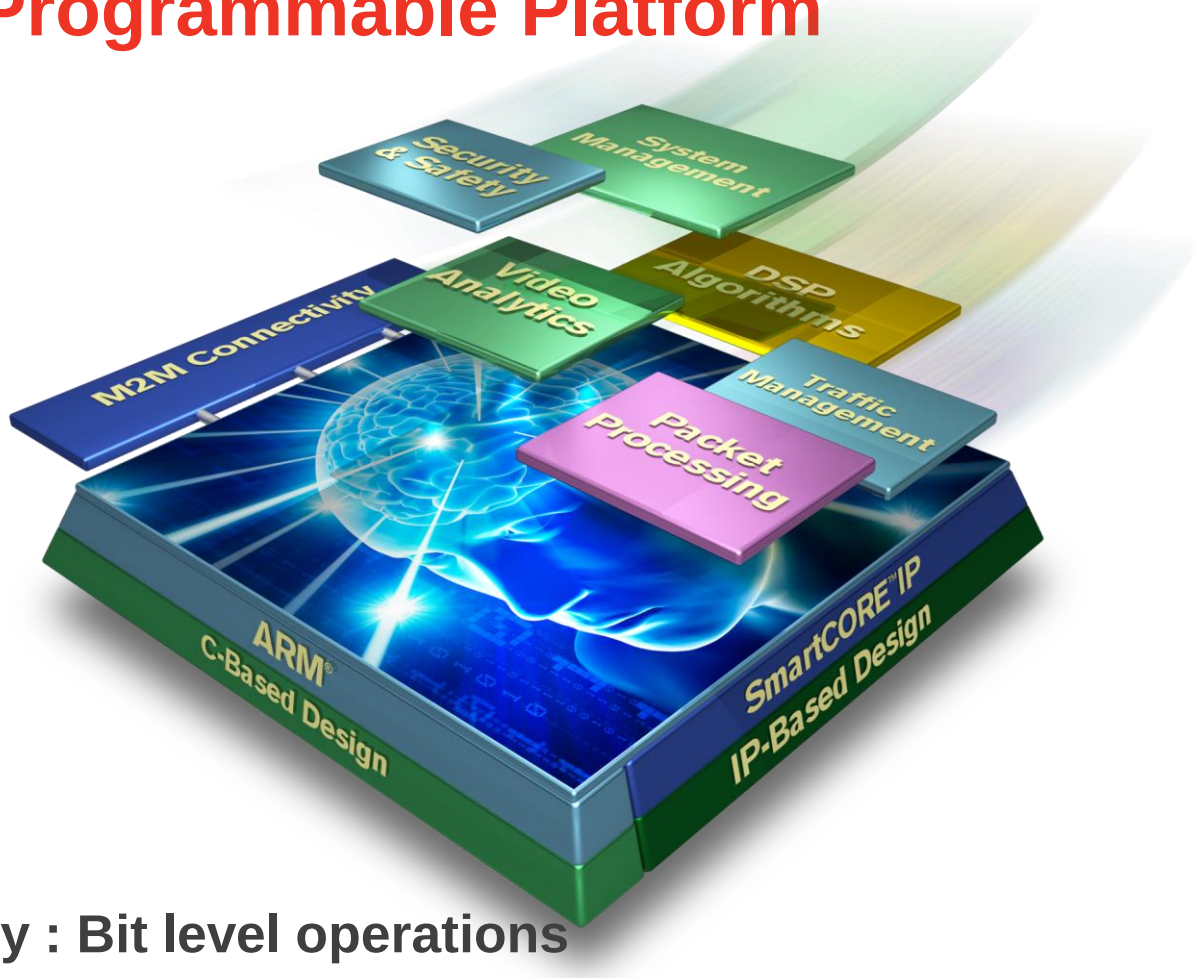
Programmable Imperative

Programmable Systems Integration



Insatiable *Intelligent* Bandwidth

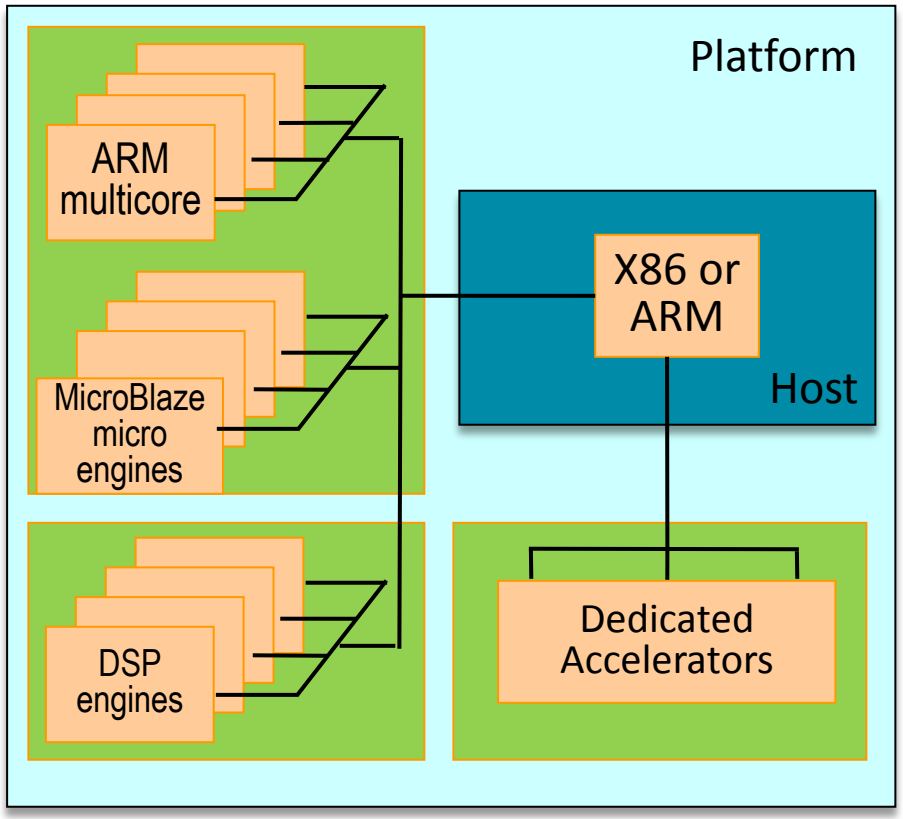
The All Programmable Platform



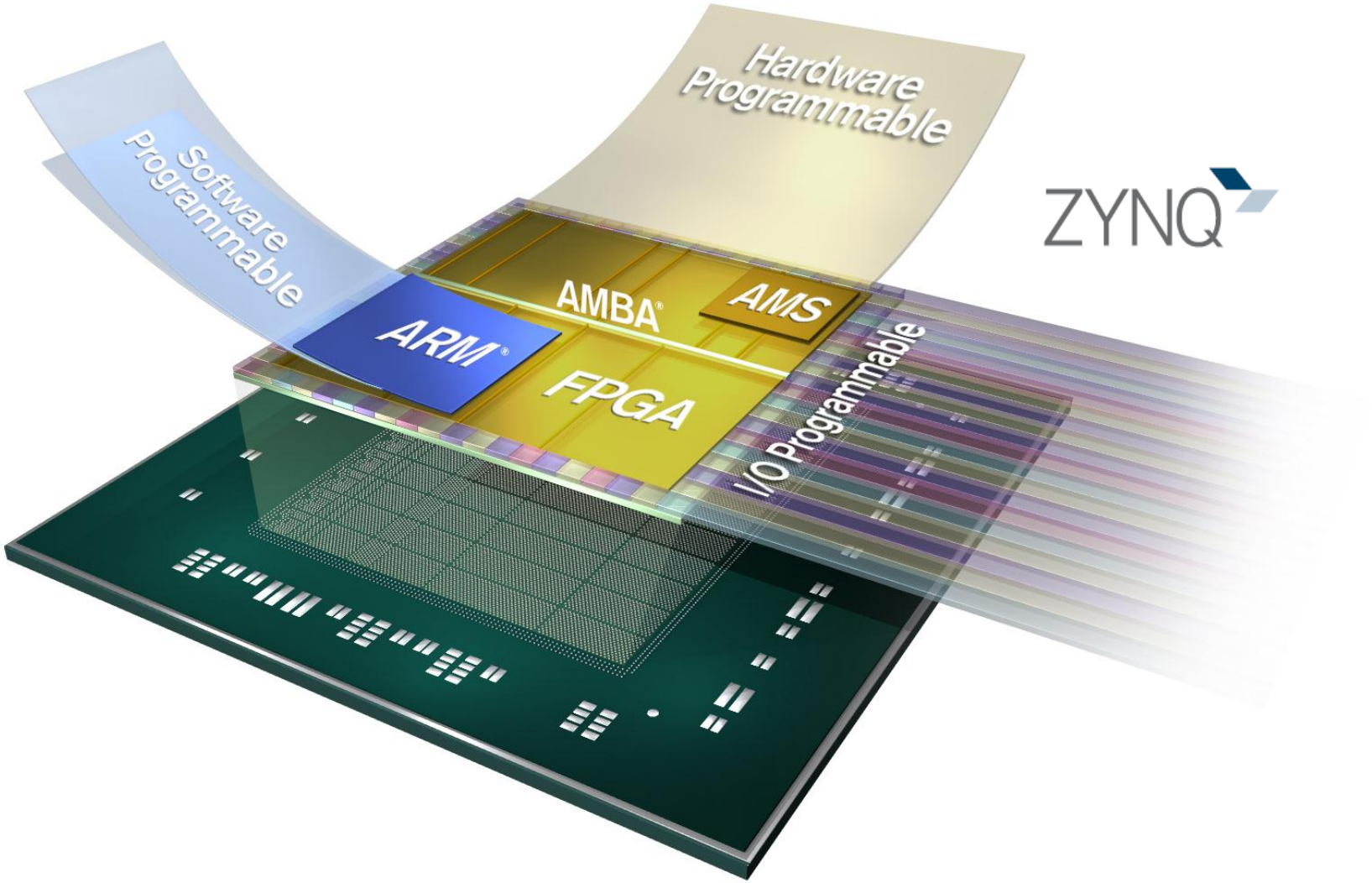
- Security : Bit level operations
- Packet Processing : Wide Datapaths
- DSP Processing : Pipelined Datapaths
- Graphics Processing : Parallel Micro-Engines
- System Management : Finite State machines

The Heterogeneous MPSoC

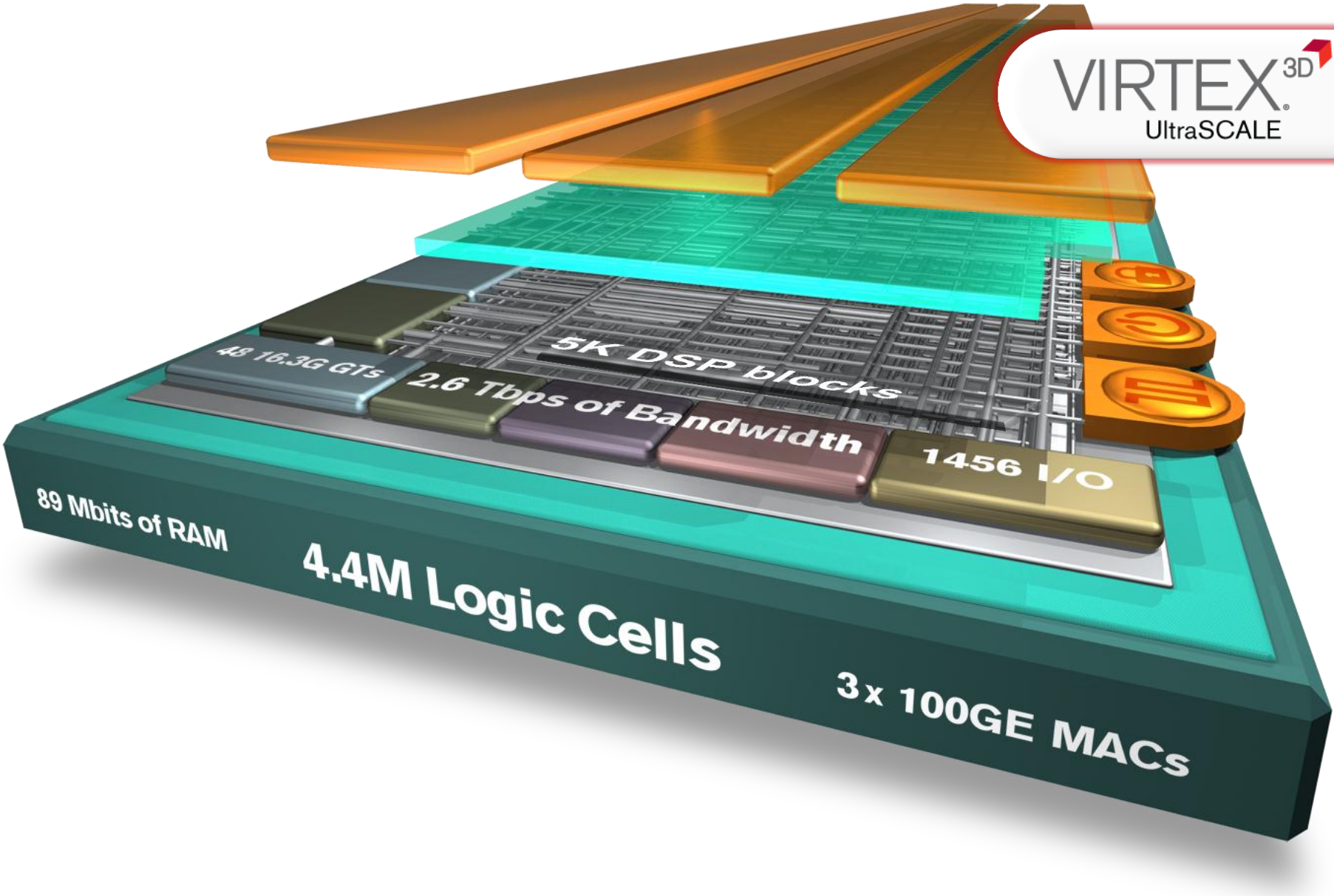
- Heterogeneous
- Connected
- Scalable
- Parallel
- Configurable



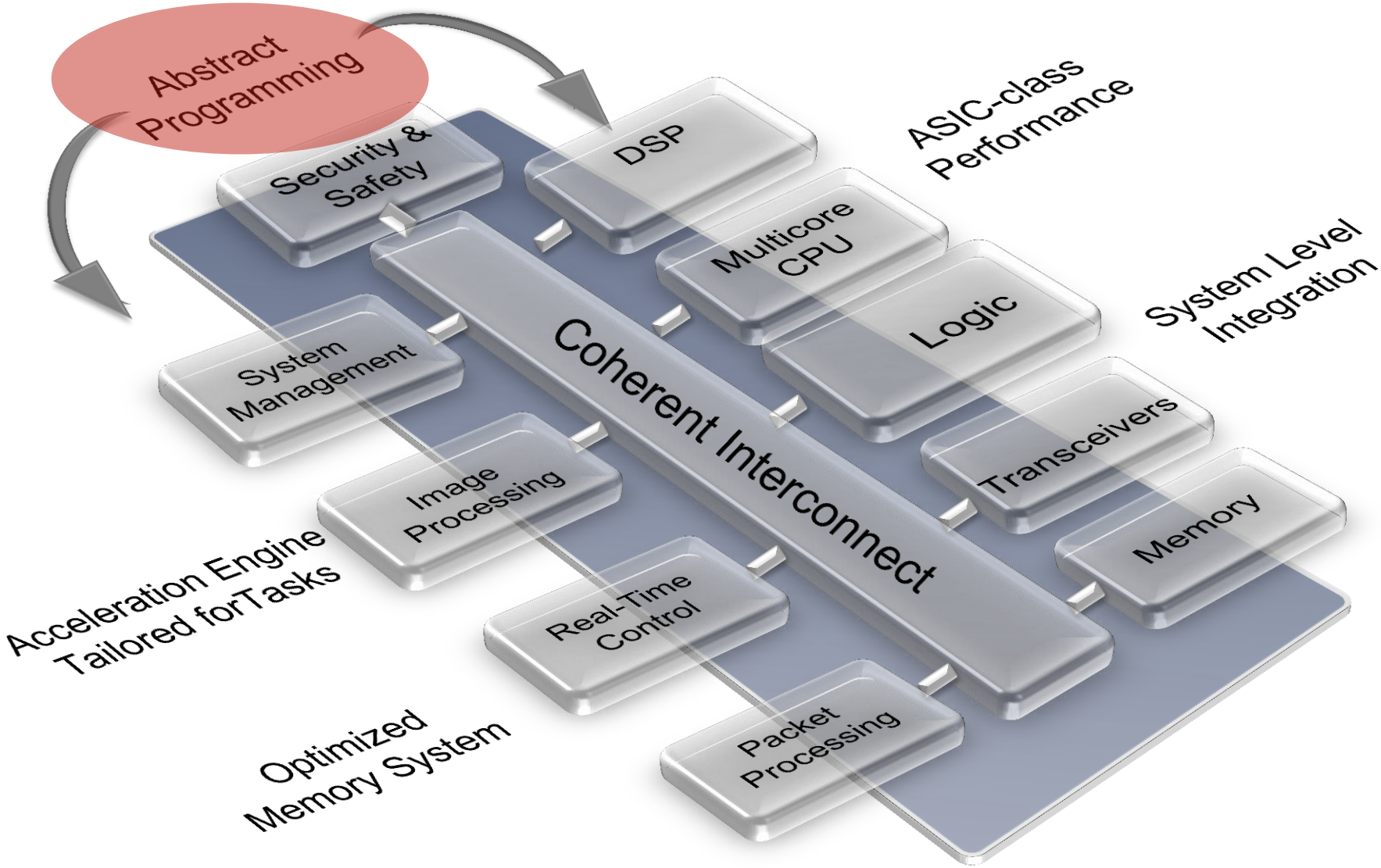
The Era of Heterogeneous Processing Unit



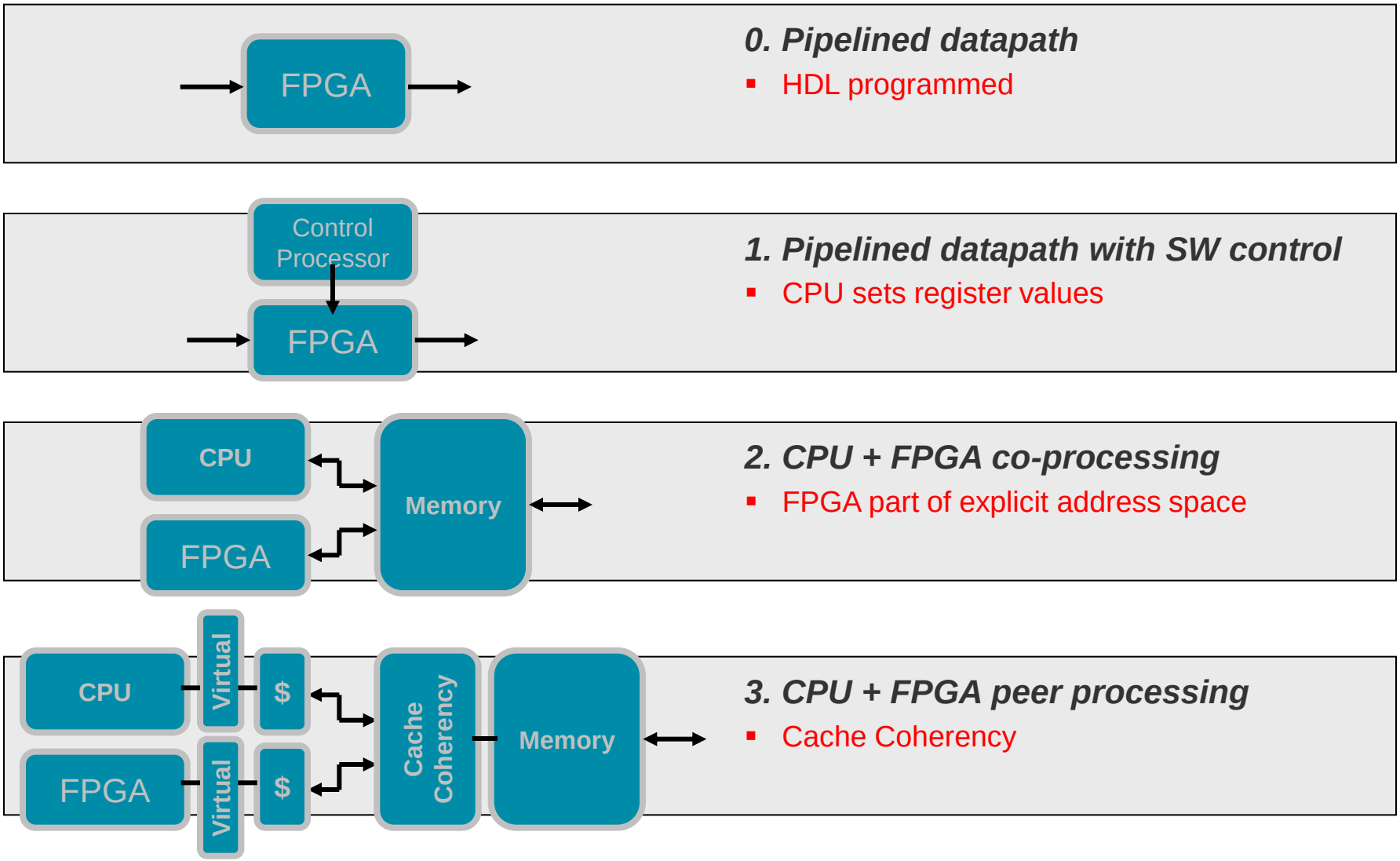
The UltraSCALE FPGA SoC



Programming the Heterogeous SoC

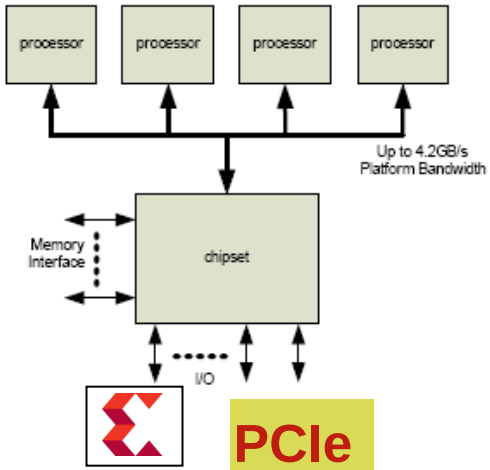


CPU + FPGA Use Models

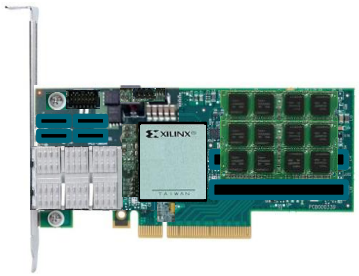


CPU + FPGA Evolution

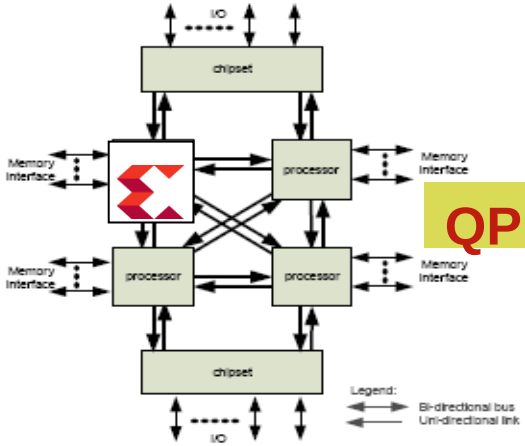
IO-Connected



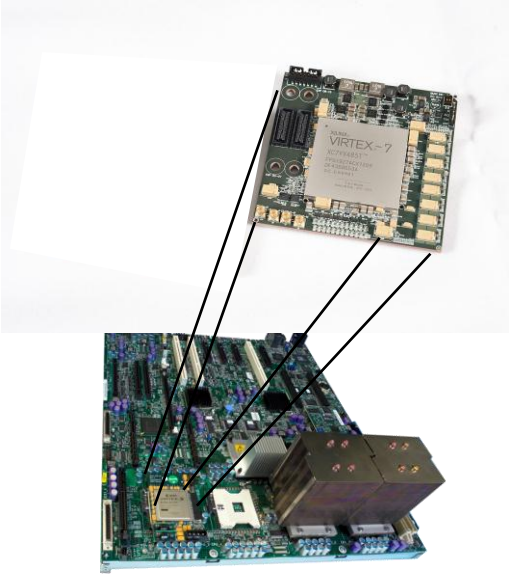
PCIe



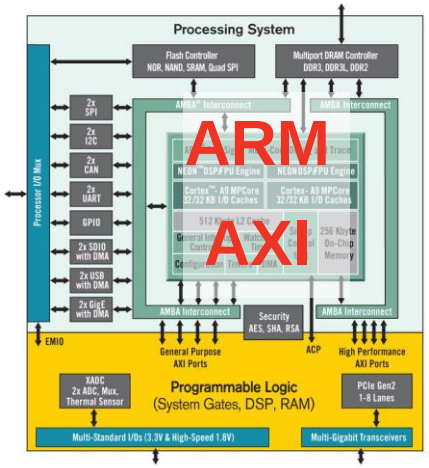
Coherent

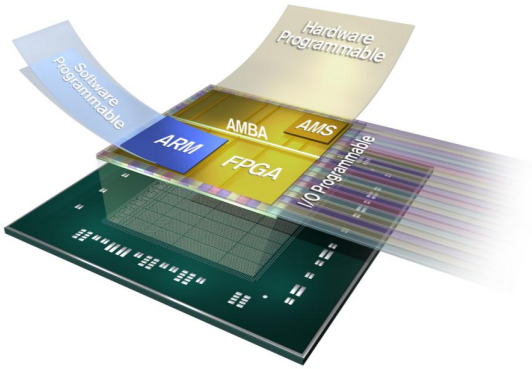


QPI

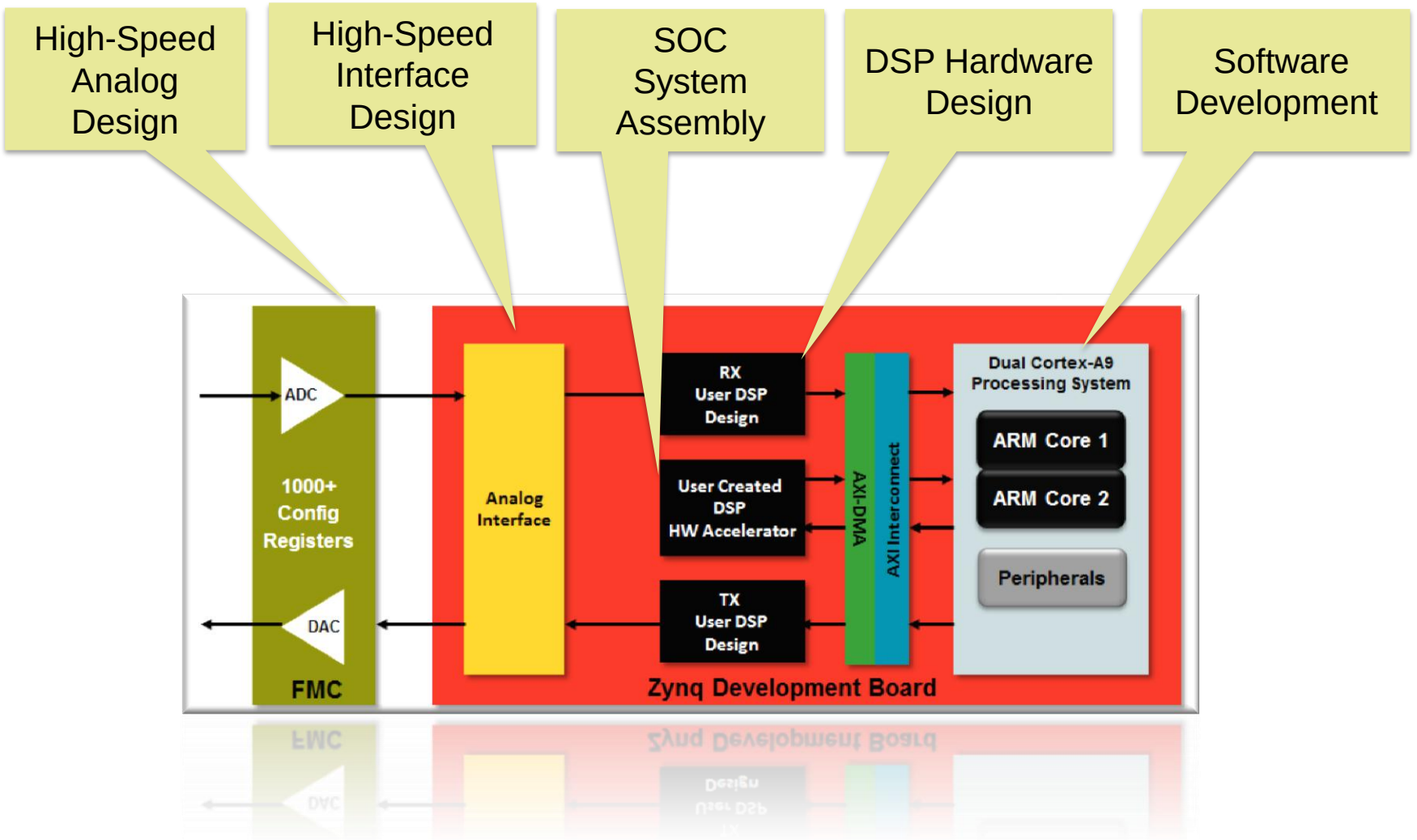


Integrated



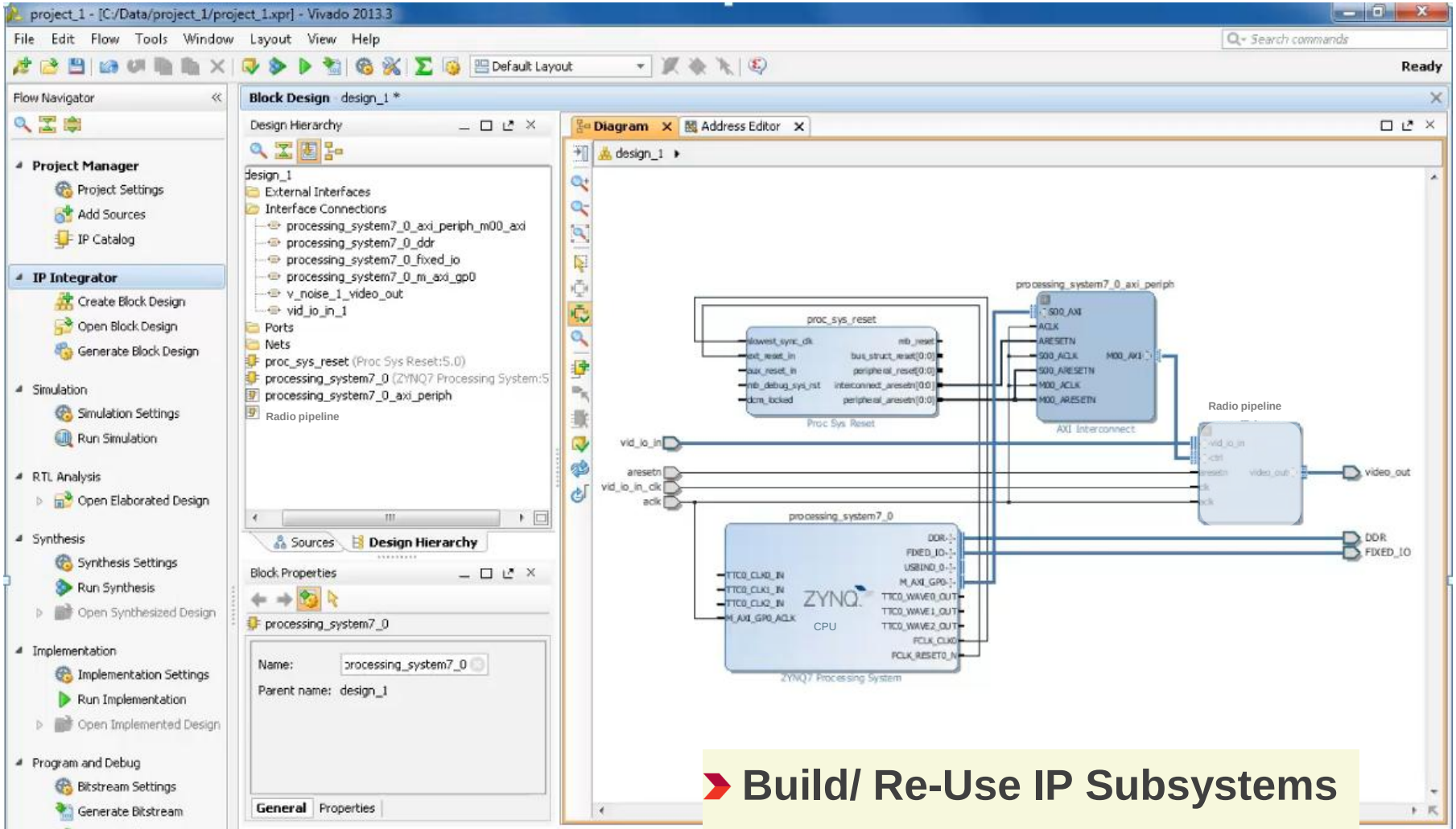


Complexity of building MPSoC systems



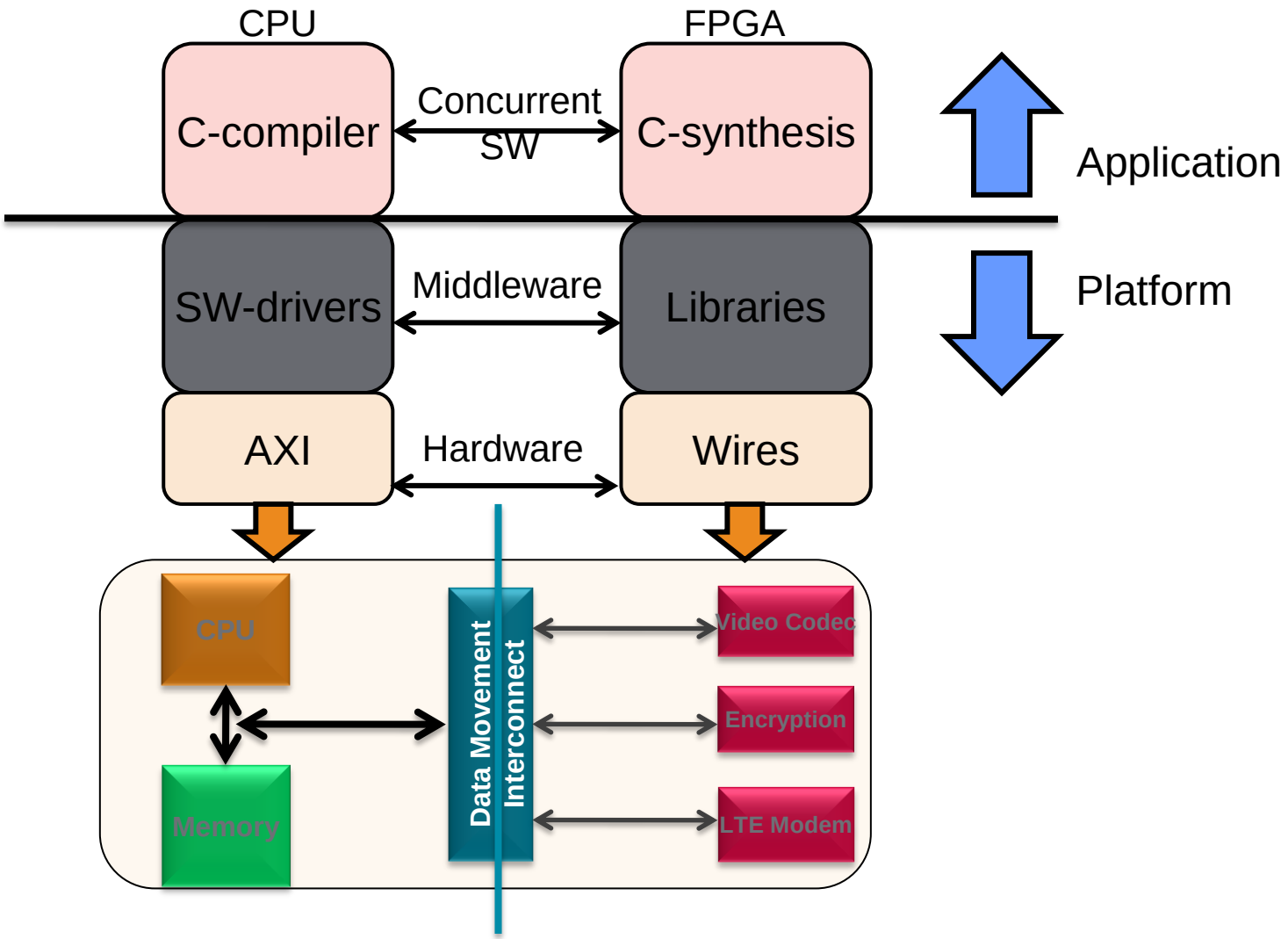
Requires distinct design skills!

Platform IP Integrator

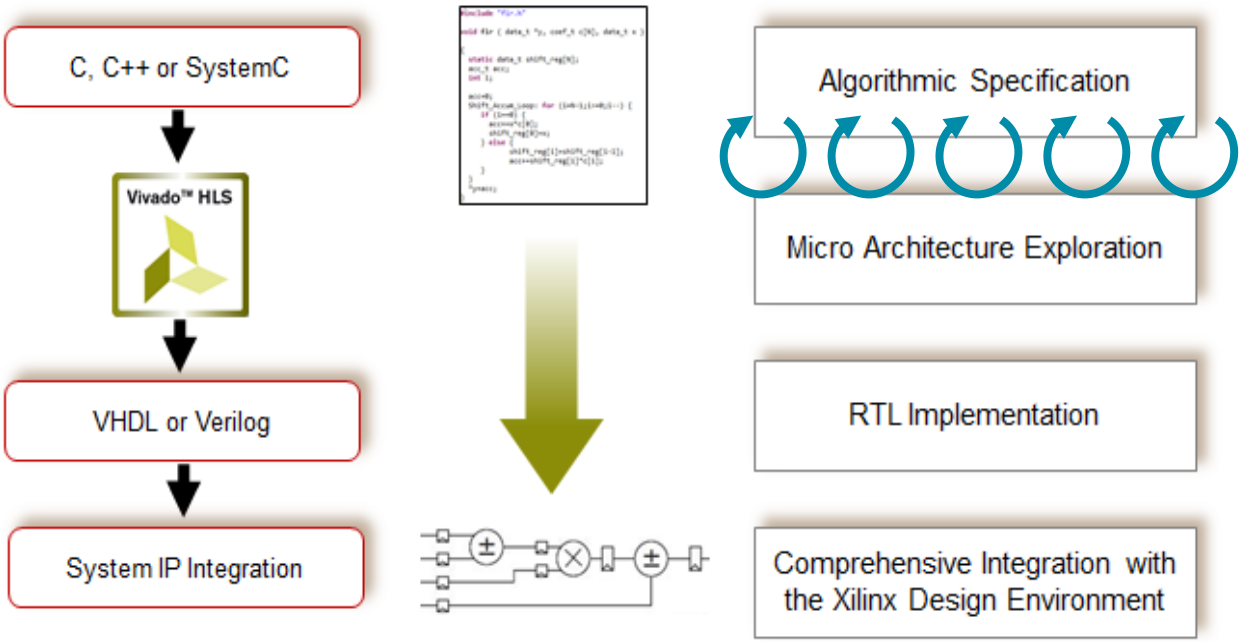


- Build/ Re-Use IP Subsystems
- Link/Assemble Subsystems
- Generate SW Drivers

HW/SW Design Flow

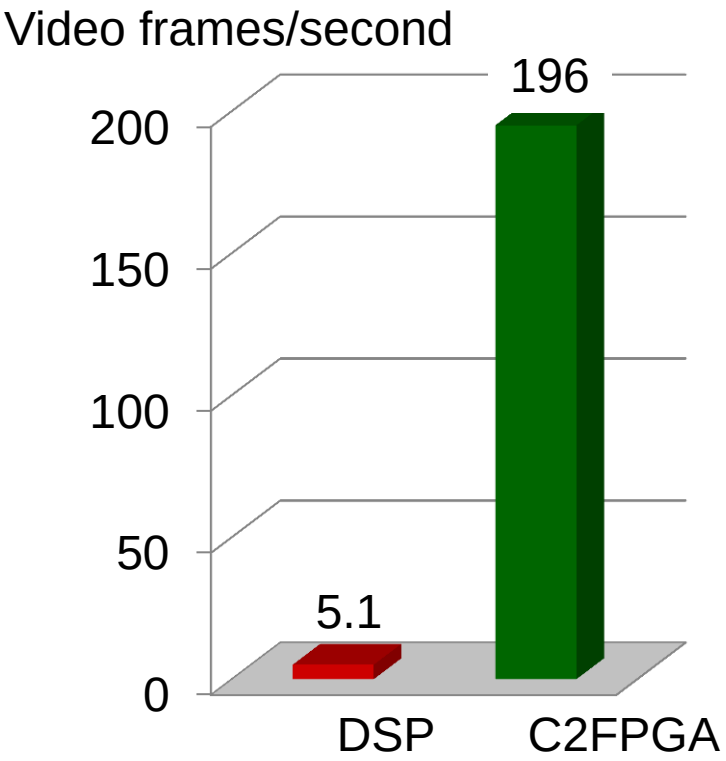


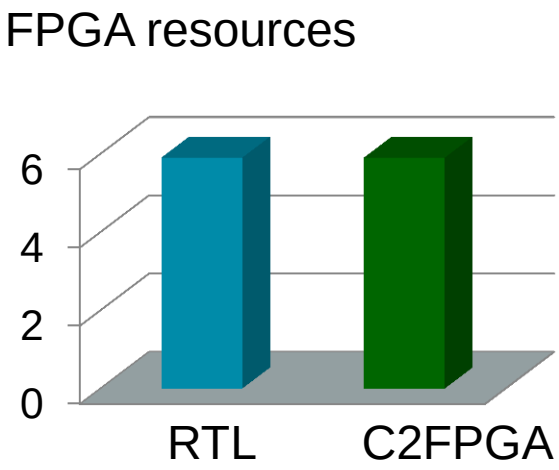
High Level Synthesis (HLS)



- Create IP from C/C++/System C algorithm specification
- Abstract algorithm verification to the specification level
- Traditional FPGA design experience not required

Quality of Results



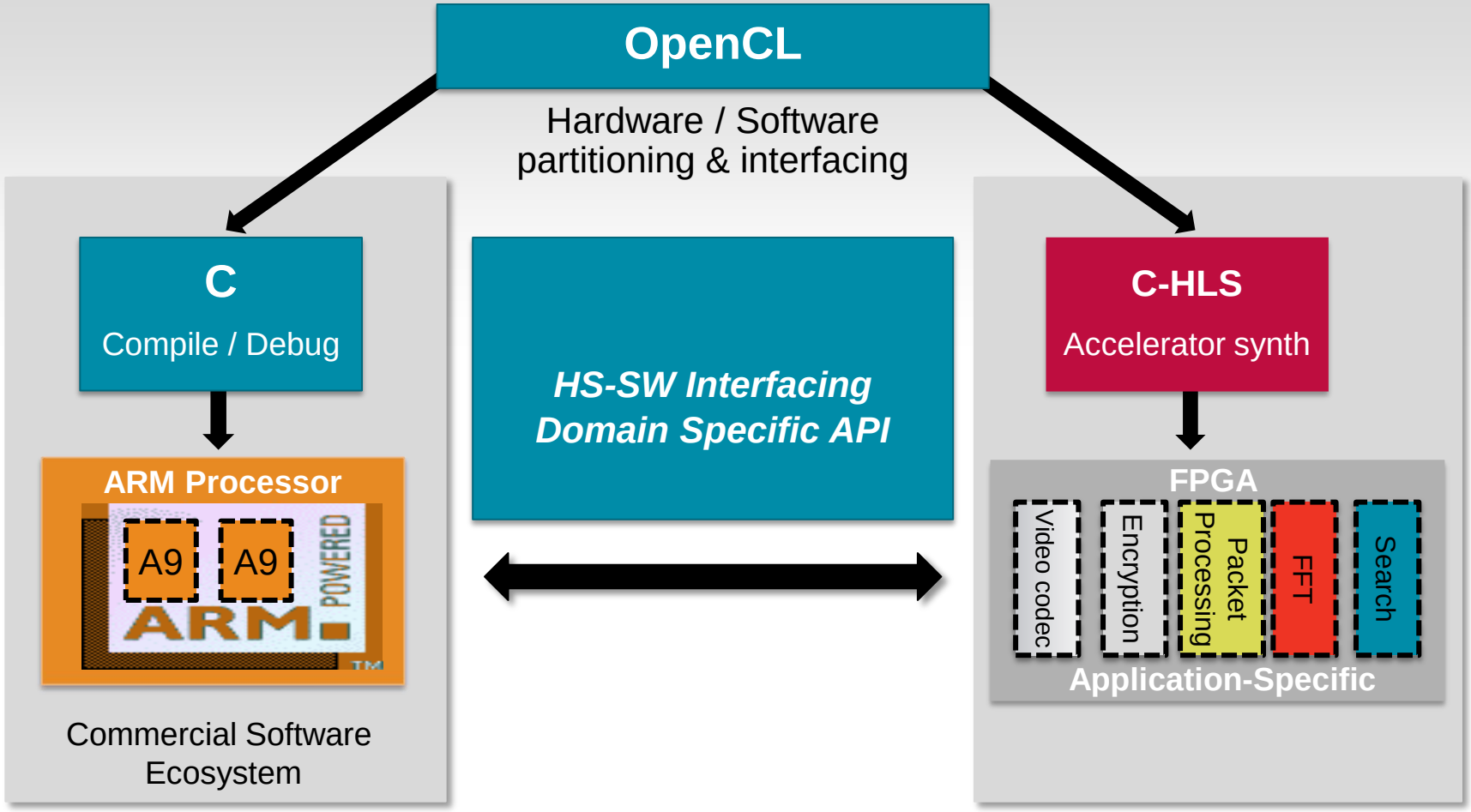


FPGA: >38 times better performance than DSP video processor

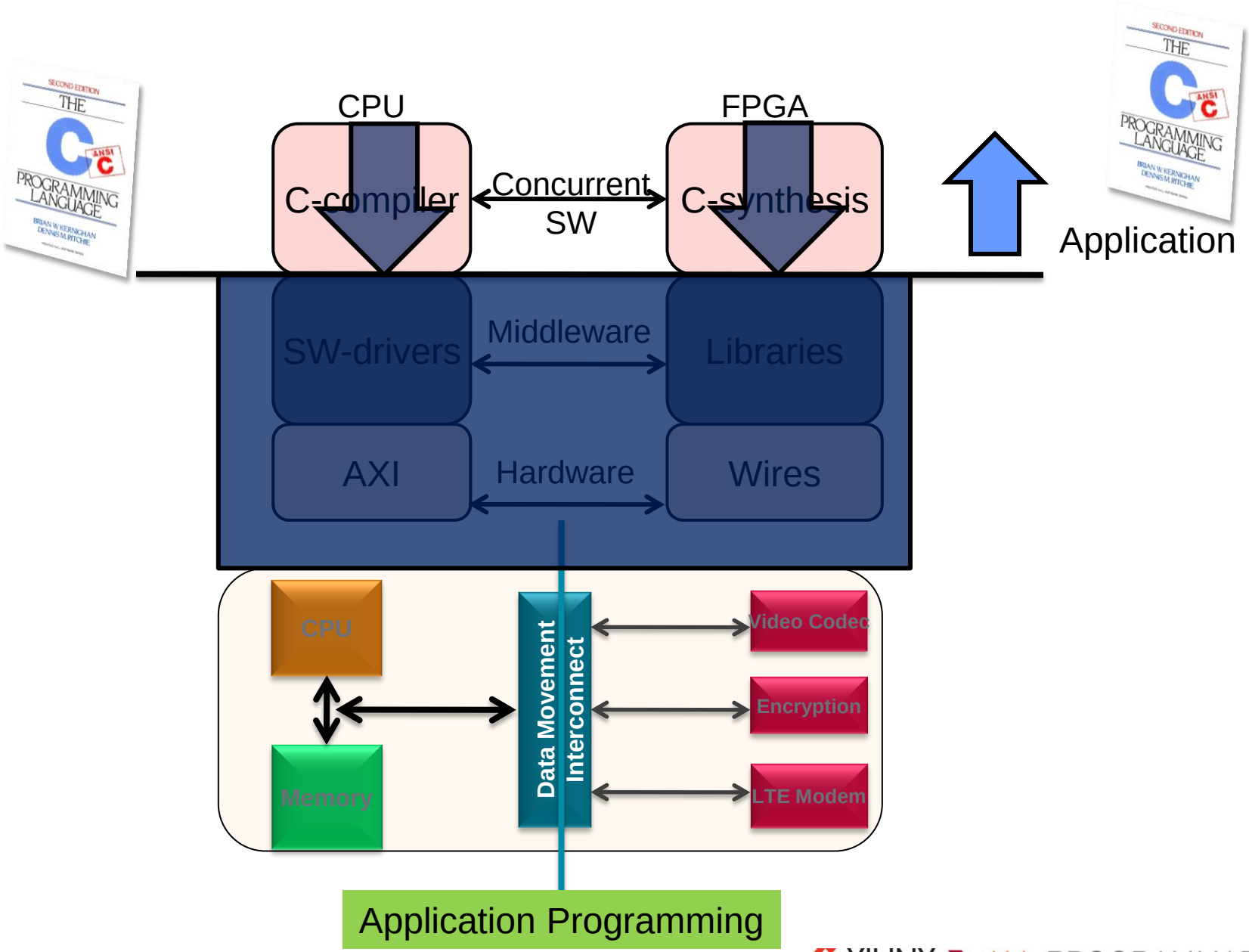
QOR: C2FPGA equal to or better than RTL synthesis

Ease-of-use: C2FPGA 2x fewer lines of C code than DSP processor

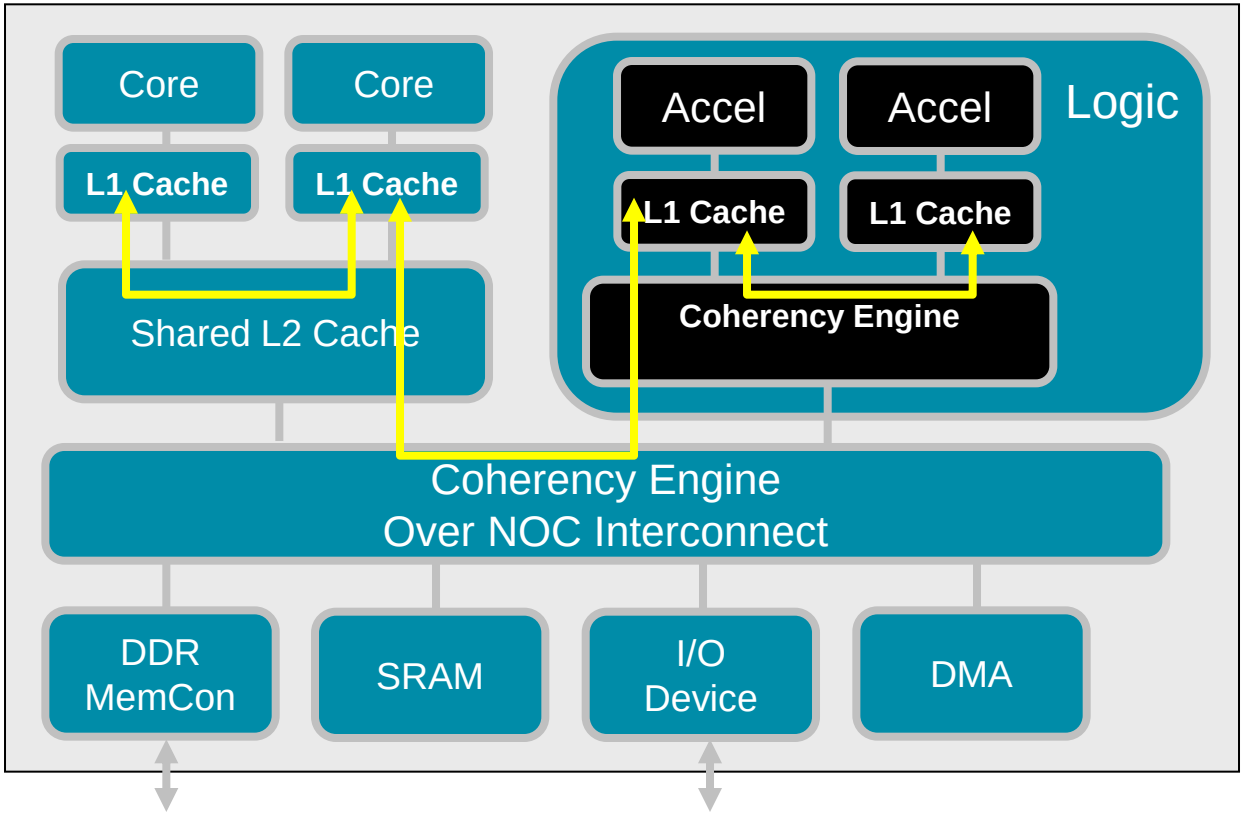
Programming Heterogeneous Multi-core



HW/SW Design Flow: SW Programmer View



Programmable Platform: CPU + FPGA Peer Processing



Capabilities

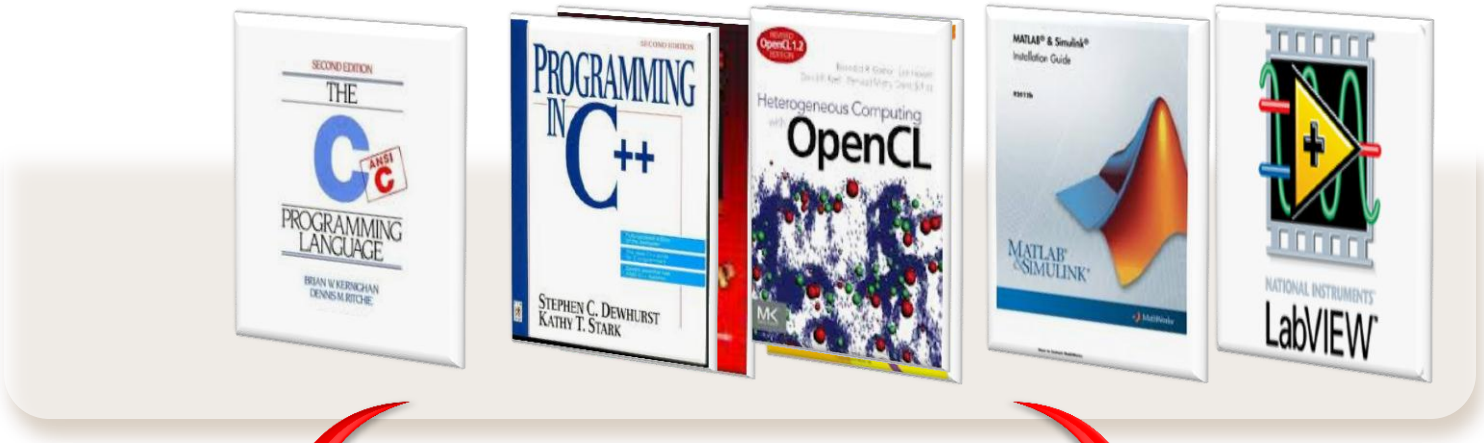
- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management

Coherency Benefits:

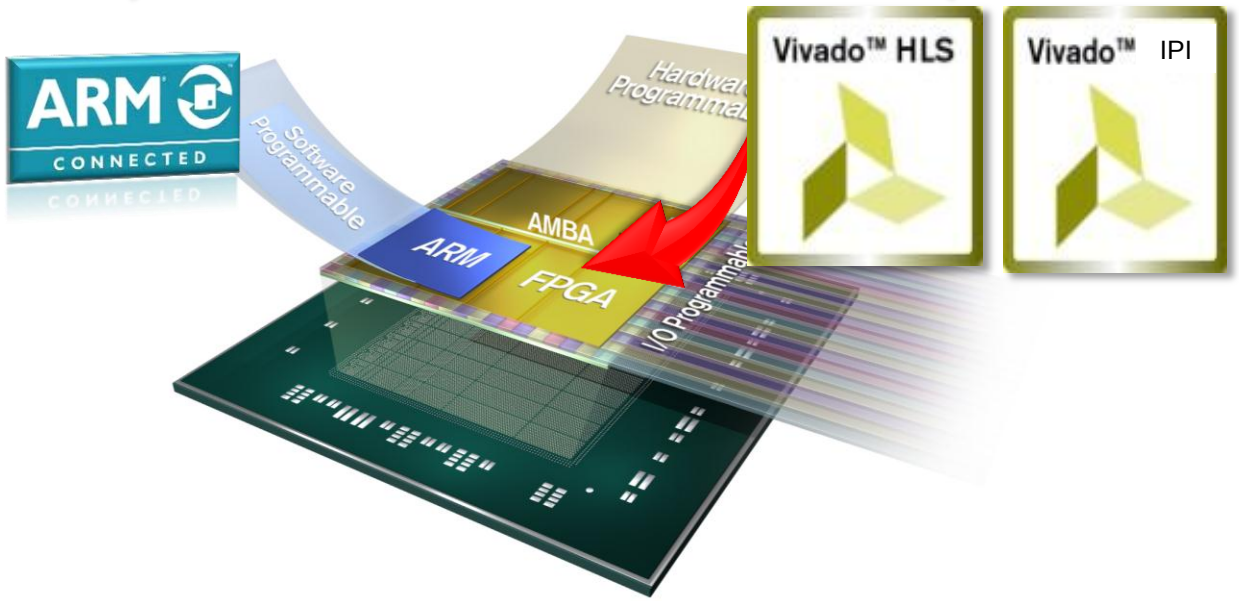
- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed

Domain Specific Abstractions

Abstraction

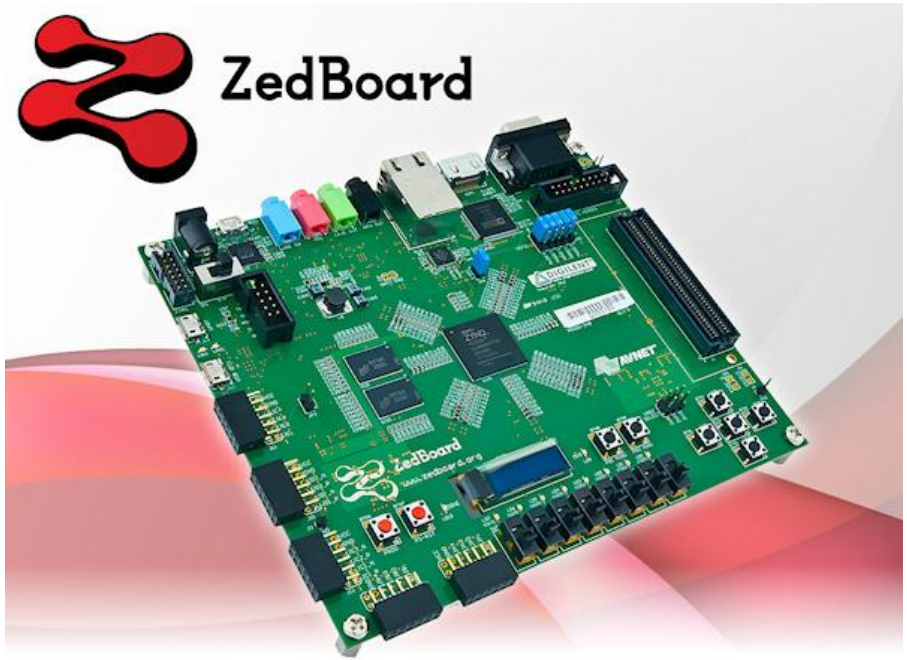


Automation



ZED Board

- **ZED Board**
  - Zynq Evaluation and Development Kit
  - Low cost Zynq based community board (XC7Z020)
  - Partnership between Avnet, Digilent, Xilinx
  - Digilent will fulfill academic market for Xilinx University Program
- **www.ZEDboard.org**
- **Open source SW and IP**
  - Linux
  - Eclipse based IDE
  - Vivado HLS: C to FPGA
  - Reference designs



Conclusions

- New Markets Require Heterogeneous Multi-Core SoC
- Modern FPGA are All Programmable SoC
- Software Centric Design Flow Becoming Possible
- Democratizing SoC Design : Targeted Teaching Platform