A 950μW 5.5-GHz Low Voltage PLL with Digitally-Calibrated ILFD and Linearized Varactor

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Background

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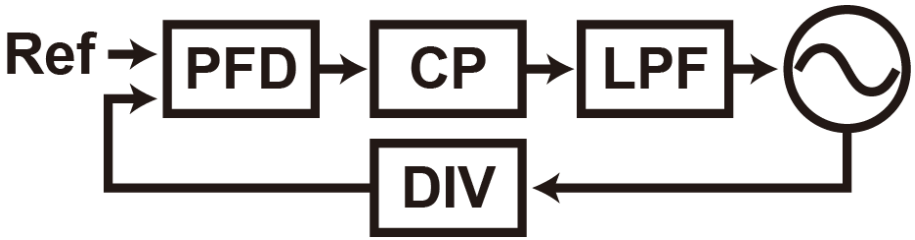
- Wireless Sensor Network (WSN)
  - req. :longer lifetimes and smaller volumes

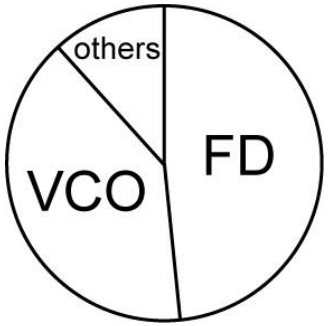
- High power consumption in high freq. RF circuits
- Small size antenna in high freq.
- Low gain in small size antenna [1]

[1] S. Oshima, et al., VLSI 2013

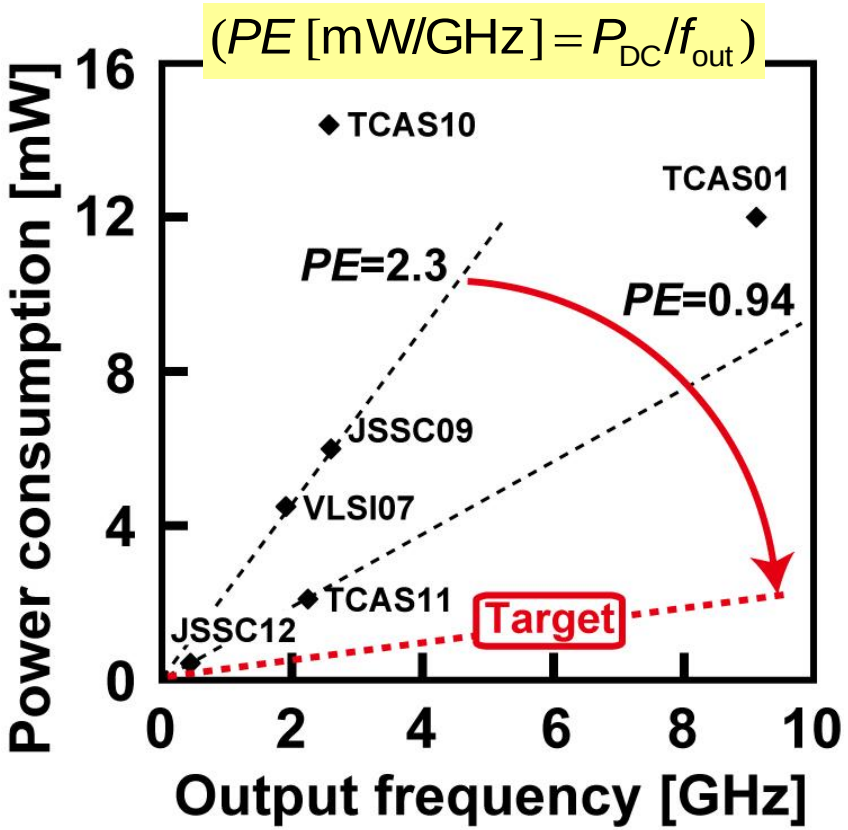
Research purpose

Ultra-low-power PLL





Power distribution



- **Challenges for low power PLL**
  - **Frequency divider, VCO**

Proposed PLL

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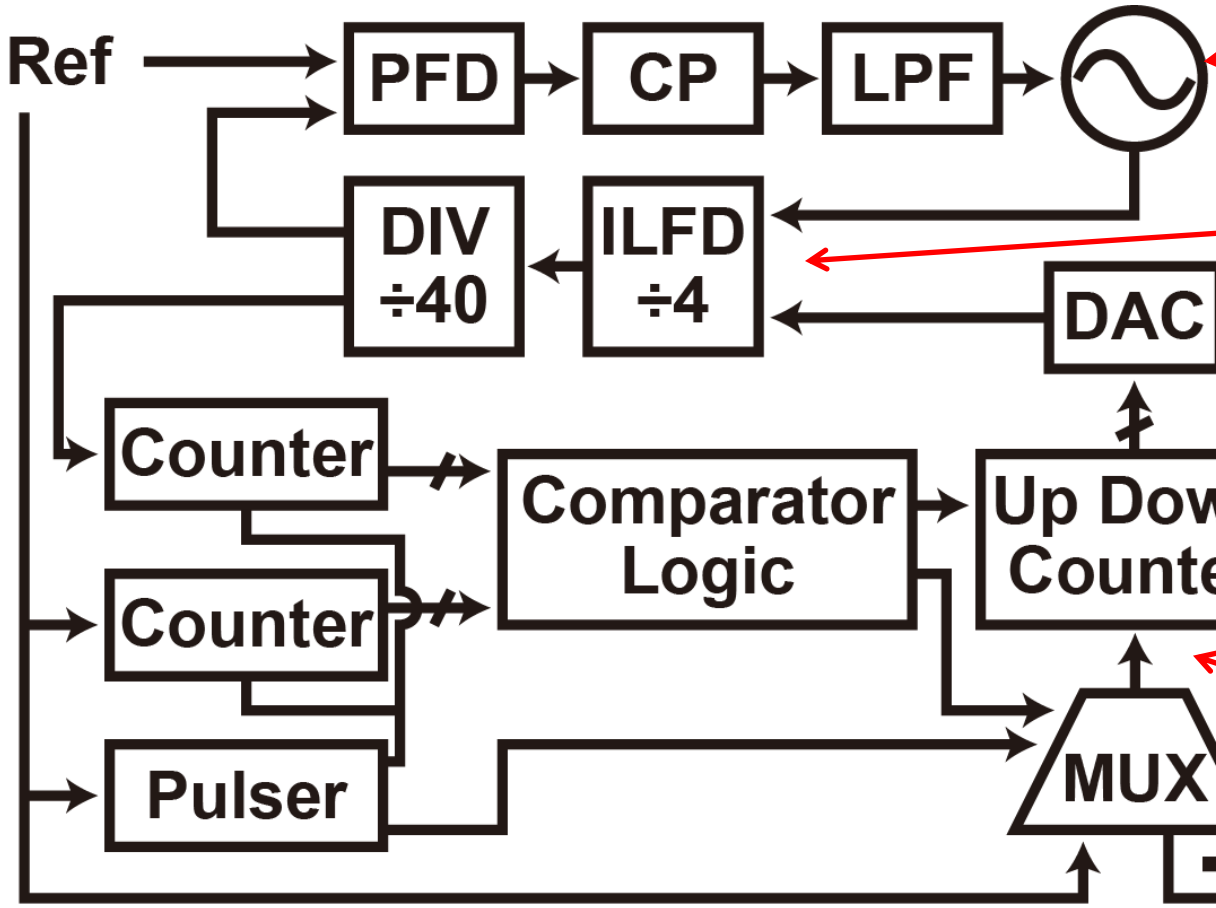
Power Supply voltage: 0.5V



Class-C
&
linear varactor

Ultra-low power
divider

Digital calibration

Results

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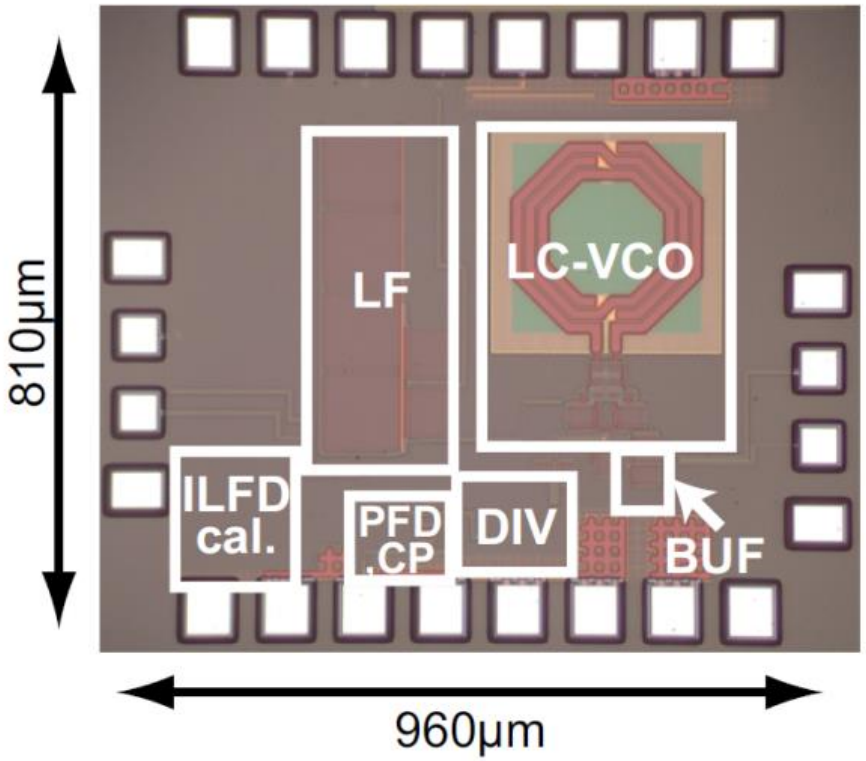

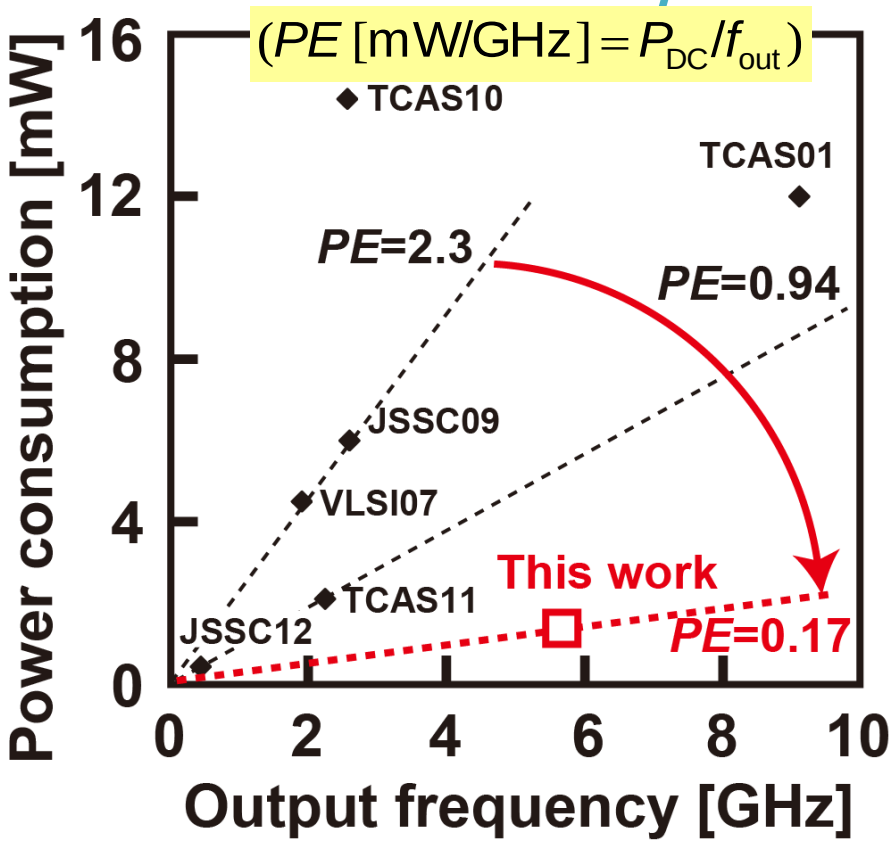

Superior power efficiency have been achieved!

Poster number : 1A-2