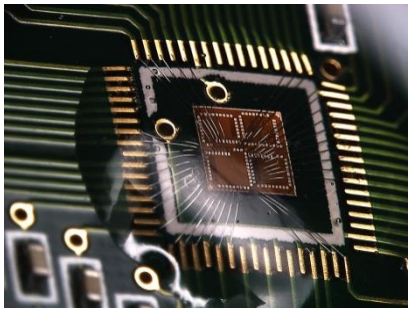

An 8b Extremely Area Efficient Threshold Configuring SAR ADC

Kentaro Yoshioka, Akira Shikata,
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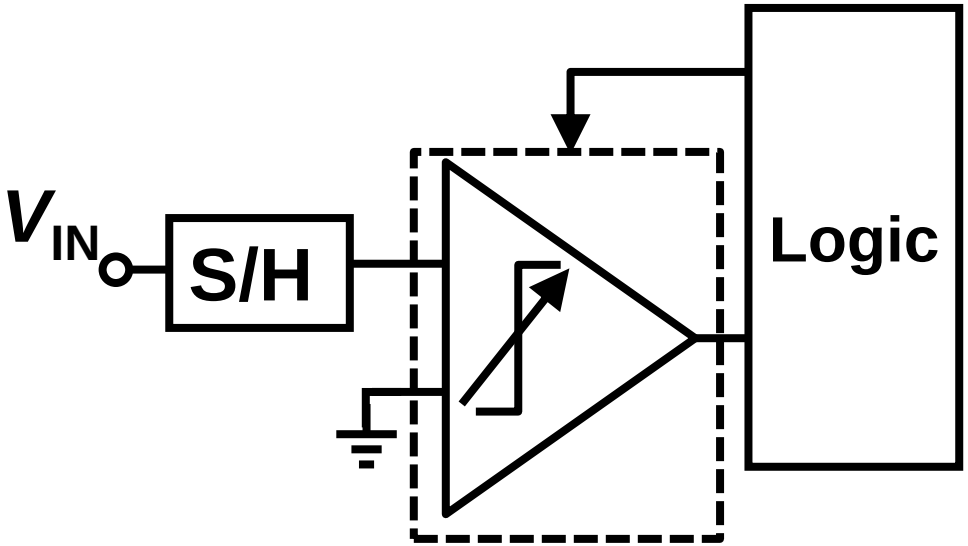
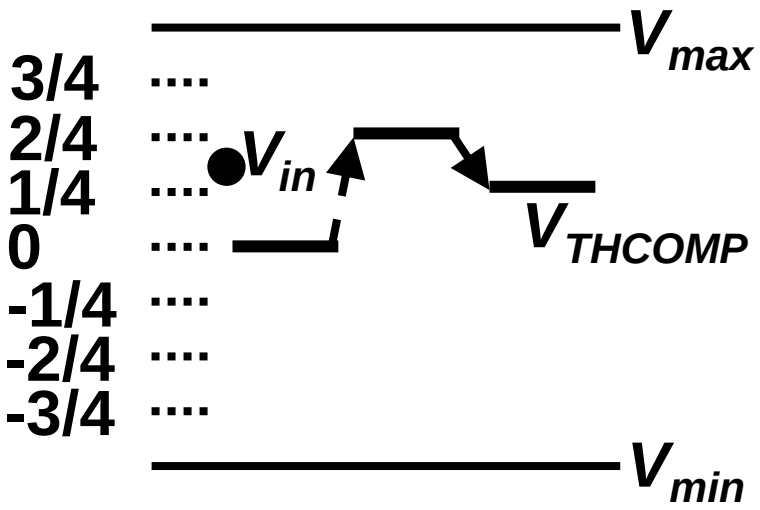
Keio University

Channel ADC design approach





Threshold configuring comparator

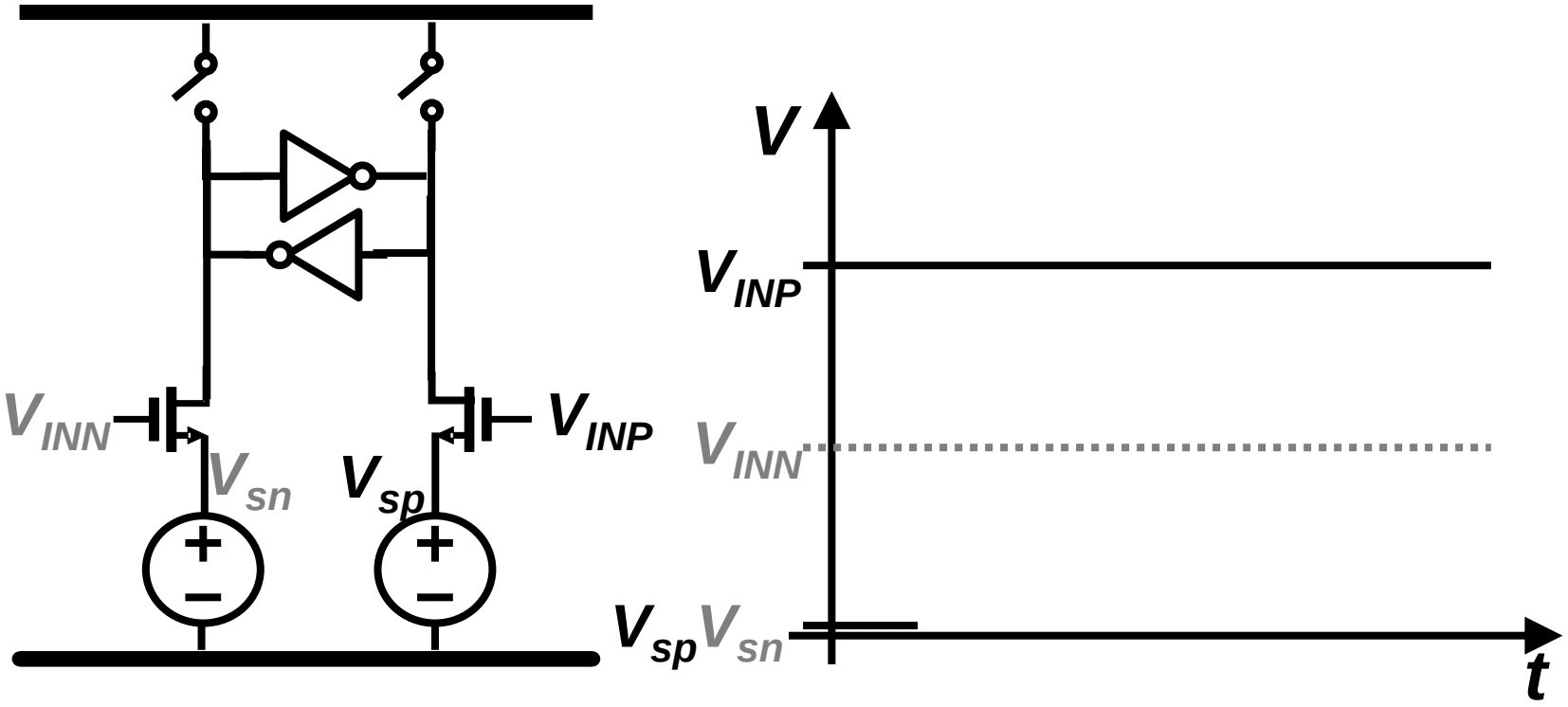
- **SAR ADC without C-DAC**
  - ◆Extremely small area
- **Threshold Configuring ADC**
  - ◆Control complex than C-DAC

VLSI Symp. 2009, P.Nuzzo

Resolution	Control Lines Required	
	C-DAC	Capacitor offset
6bit	12	63
7bit	14	127
8bit	16	255

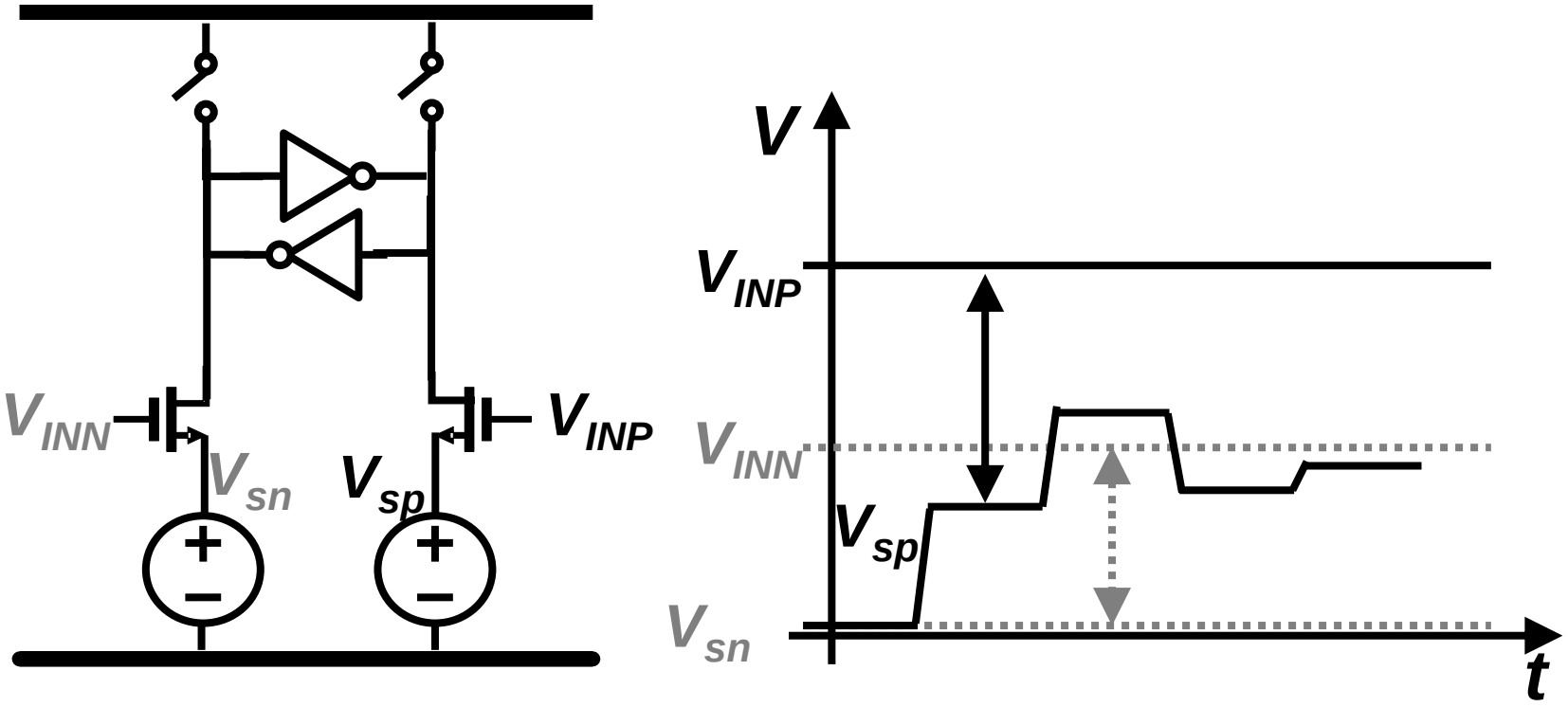
Proposed Source Voltage Shifting

- **Comparator w/source voltage shifter**
  - **One side of source voltage shifter activated**



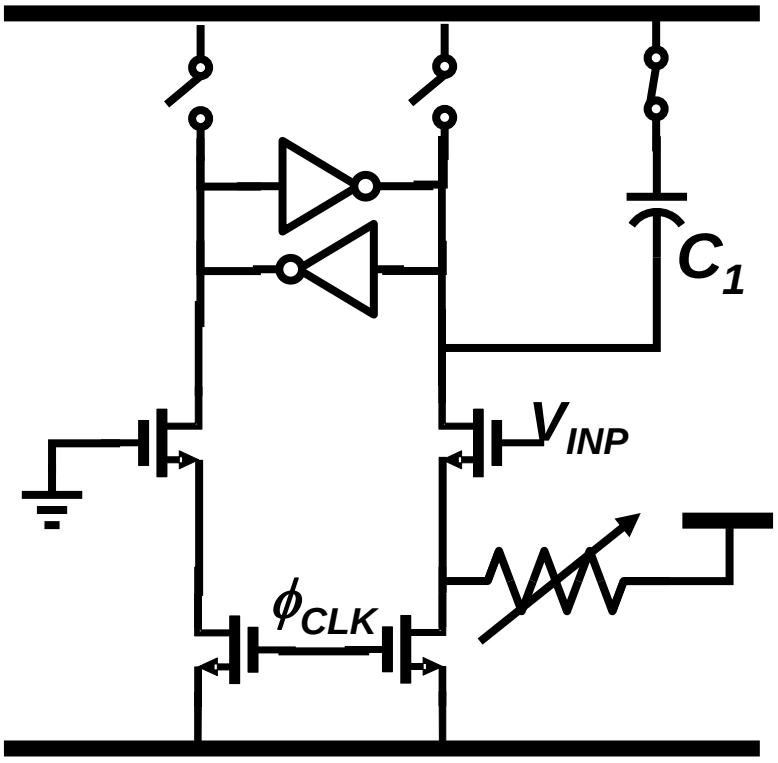
Proposed Source Voltage Shifting

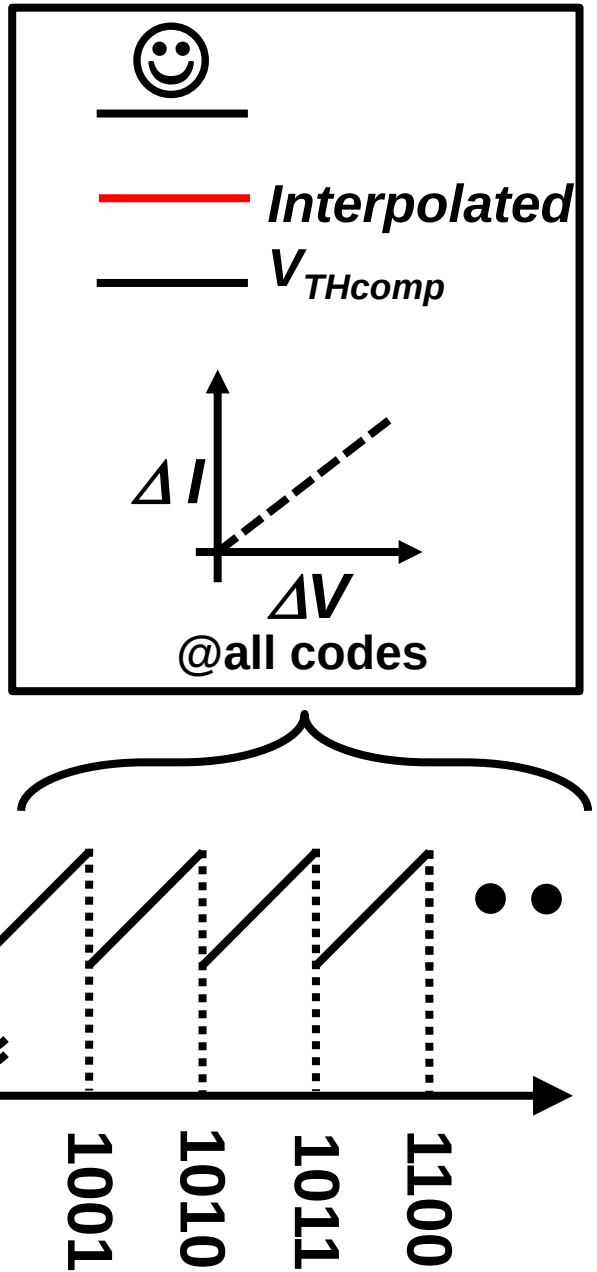
- **Comparator w/source voltage shifter**
  - **One side of source voltage shifter activated**
  - **Compares V_{GS} of input transistor**



Threshold Interpolation

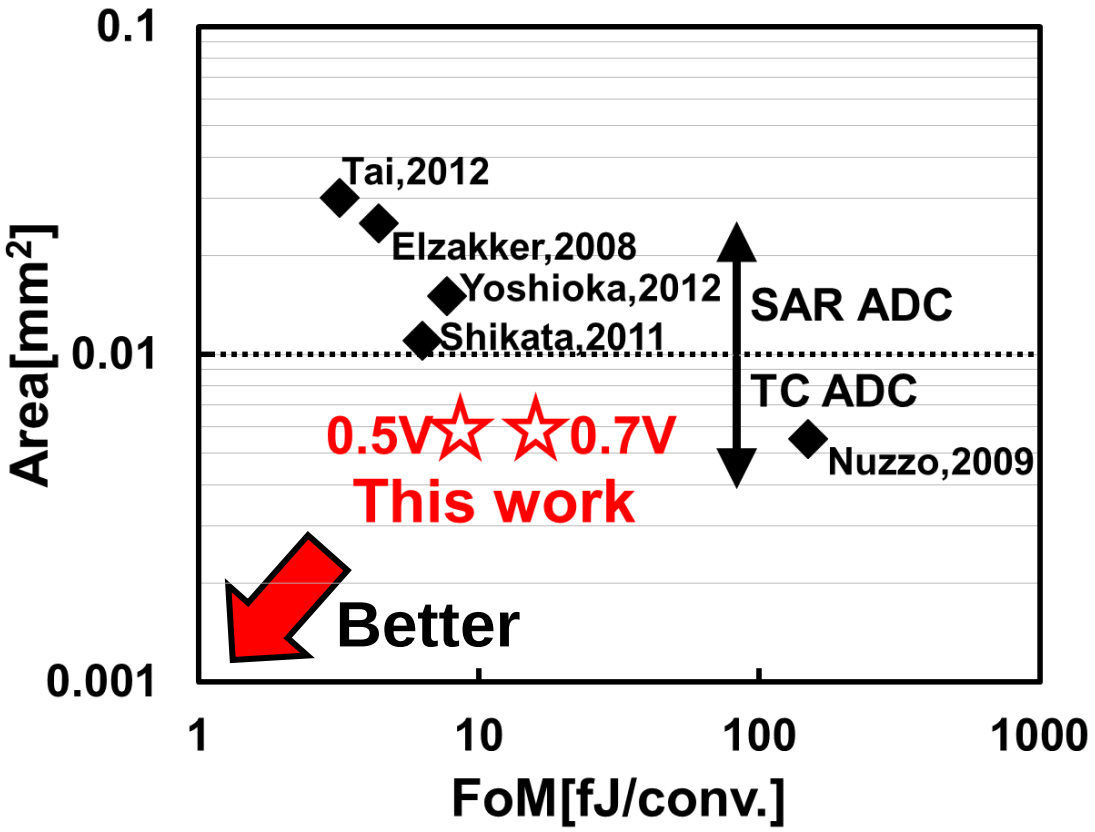
- With source voltage shift
  - Folded current characteristic
    - Desired interpolated V_{THcomp} @all codes





Measured results

- **FoM as low as SoA SAR ADCs achieved**
  - **TC-ADC occupies 50% less area**
  - **15x FoM improvement compared to conv. TC-ADC**



Technology [nm]	40	
Total Area [mm^2]	0.0058	
Architecture	TC-ADC	
Supply Voltage [V]	0.5	0.7
F_S [MS/s]	2.048	24.576
SNDR [dB]	41.5	44.2
Power [μW]	1.9	54.6
FoM [fJ/conv.]	9.8	17