Comprehensive Die-Level Assessment of Design Rules and Layouts

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Introduction

- Impact of new **technologies** on **design** is inferred from **Design Rules (DRs)**
- Process of evaluation of **DRs** is largely unsystematic and empirical
- Interaction of DRs with layouts, performance, margins, yield requires a **fast** and **systematic** evaluation method

Prior Work

UCLA_DRE *(ICCAD'09 ,TCAD'12)*

- A framework for early exploration of design rules, patterning technologies, layout methodologies, and library architectures
- Standard cell-level evaluation

Shortcomings

- Not every change in cell area results in a corresponding change in chip area
- Chip area can be affected by buffering and gate sizing to meet timing constraints

Prior Work

UCLA_DRE *(ICCAD'08-TCAD'12)*

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- S…

Chip-Level Design Rule Evaluation (Chip-DRE)

Sho…

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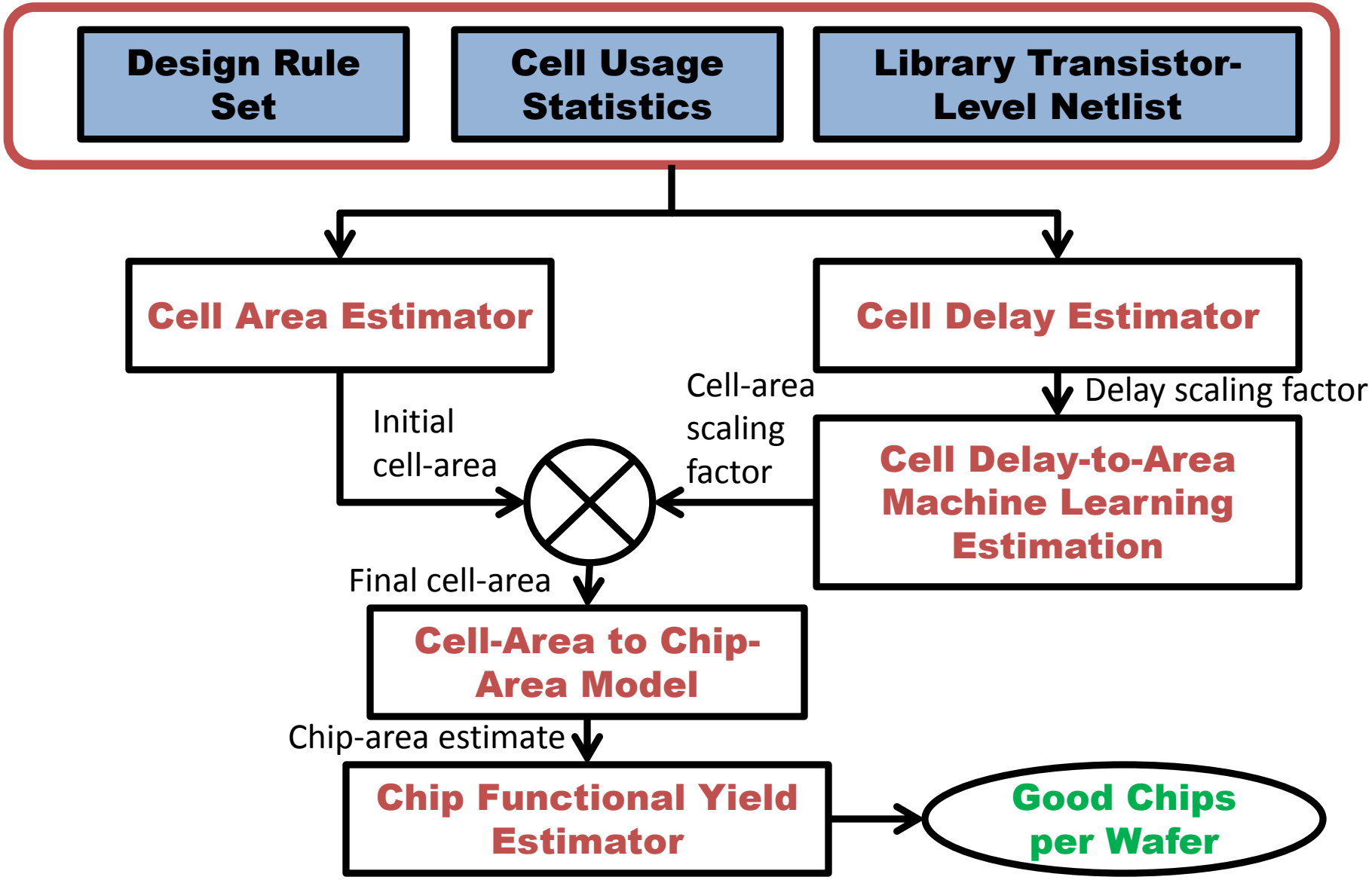
Chip-DRE: Chip level Design Rule Evaluator

- Generates virtual standard-cell library
- Employs semi-empirical and machine-learning-based models
- **Good Chips per Wafer** (**GCPW**)
  - unified metric for area, performance, variability and functional yield metrics

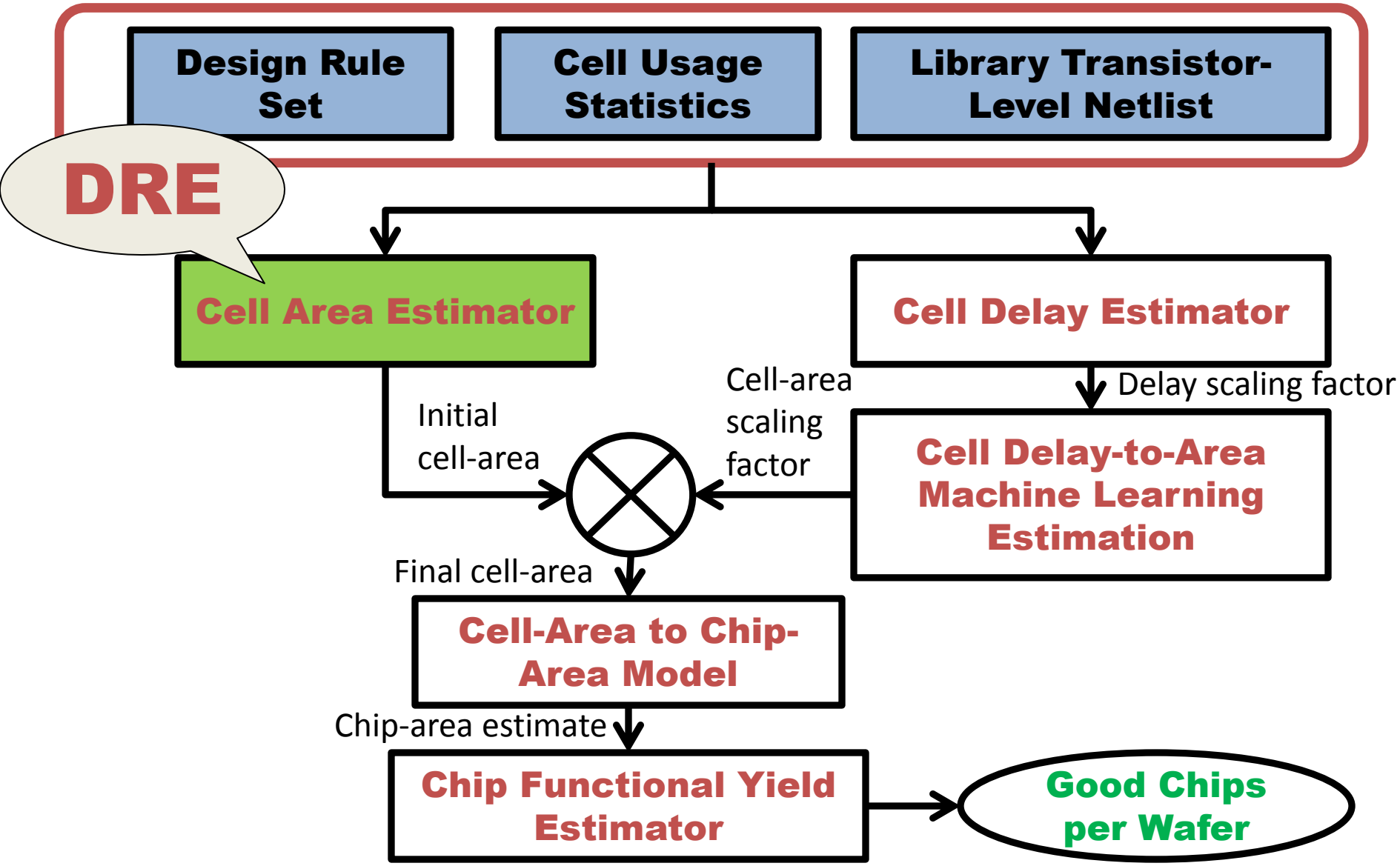
$$\frac{\text{wafer\_area}}{\text{chip\_area}} \times \text{yield}$$

FLOW OF CHIP-DRE

Chip-DRE Flow



Chip-DRE Flow



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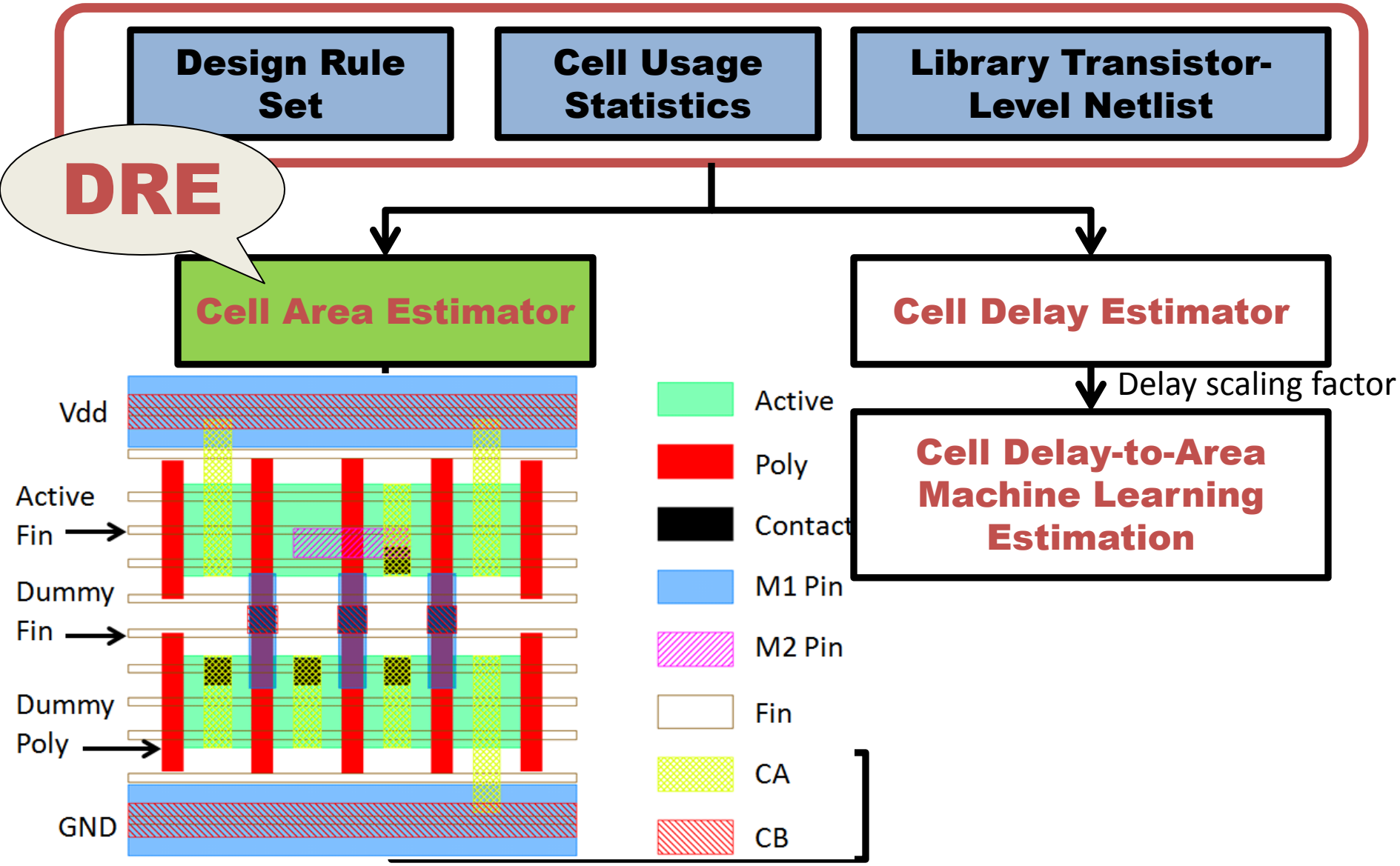

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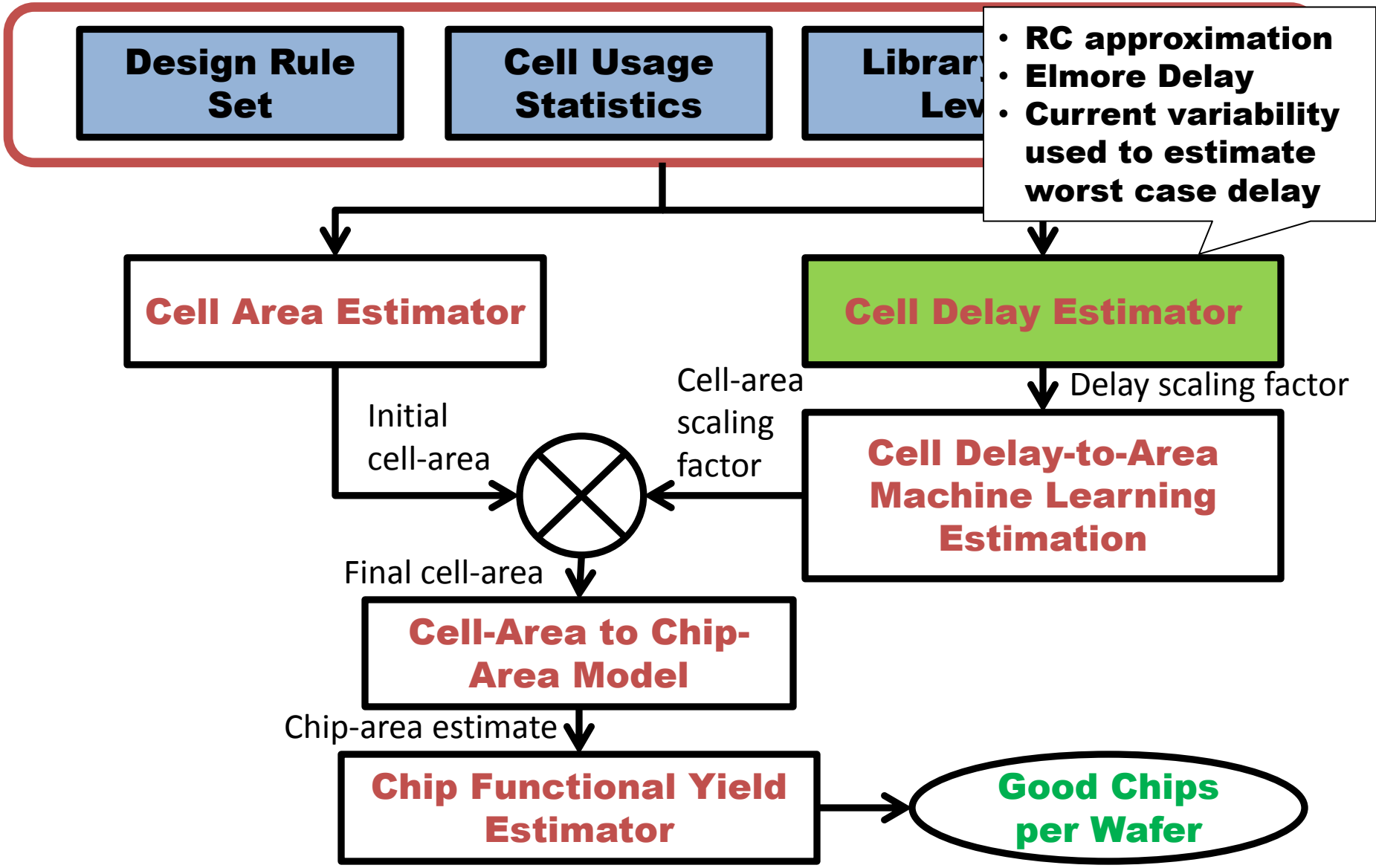

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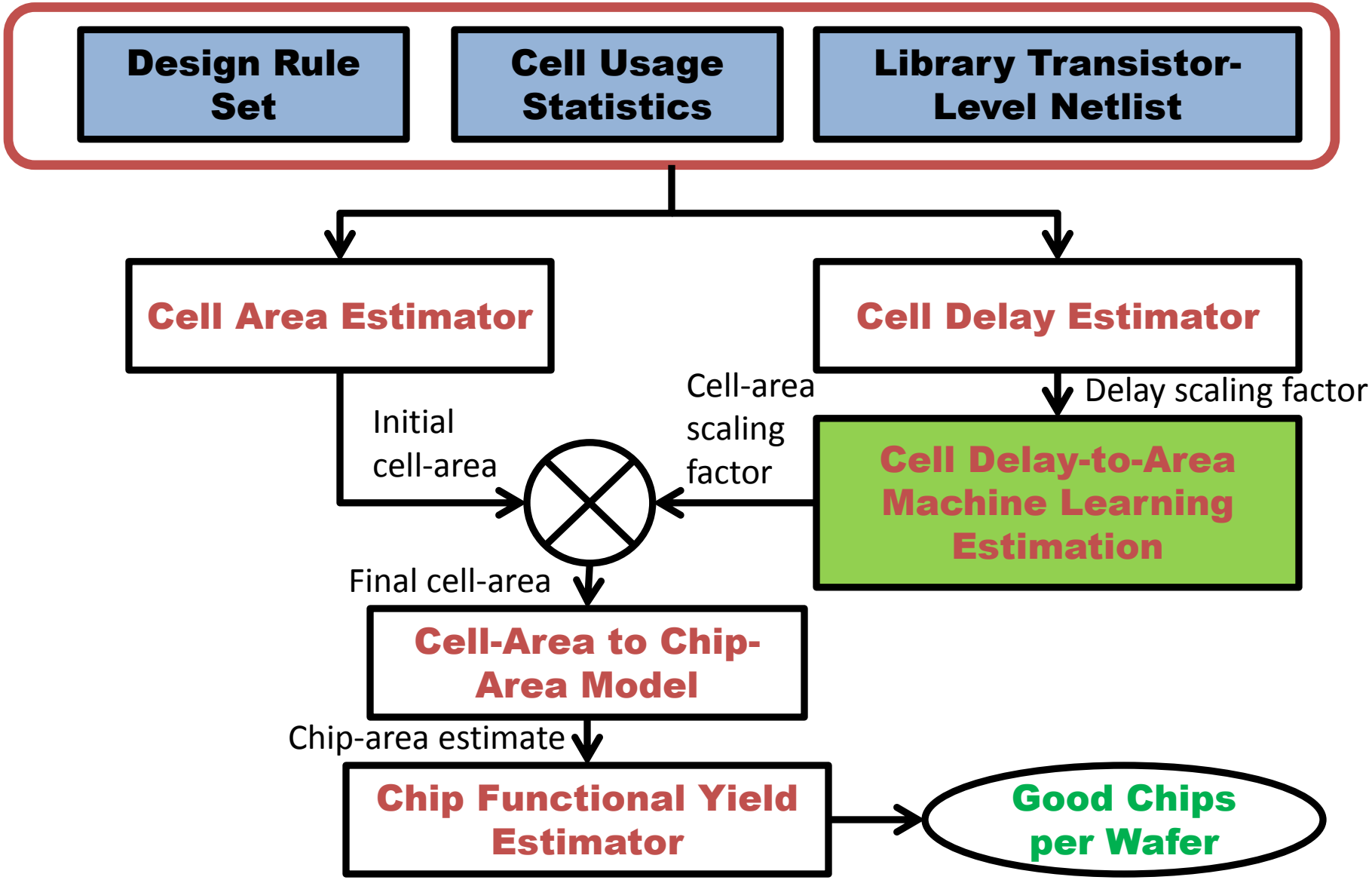

Cell Delay-to-Area Model

- Addresses effect of timing optimization during physical synthesis
- Predicts total **cell-area** scaling factor as **cell-delay** is scaled
- Based on **Machine learning**: Neural Network
- Features:
  - number of instances on critical path,
  - average fanout, average interconnect length,
  - average delay and area of gates on critical path,
  - utilization and timing constraint,
  - ratio between area of critical paths to total cell area and
  - delay scaling factor

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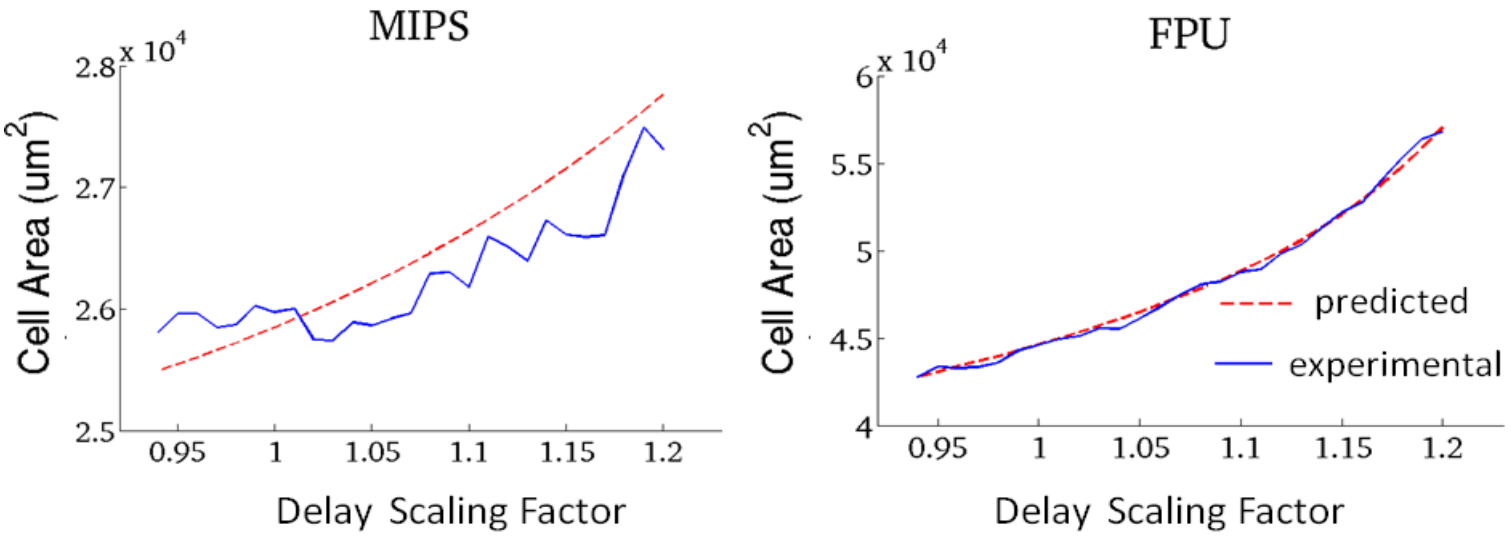

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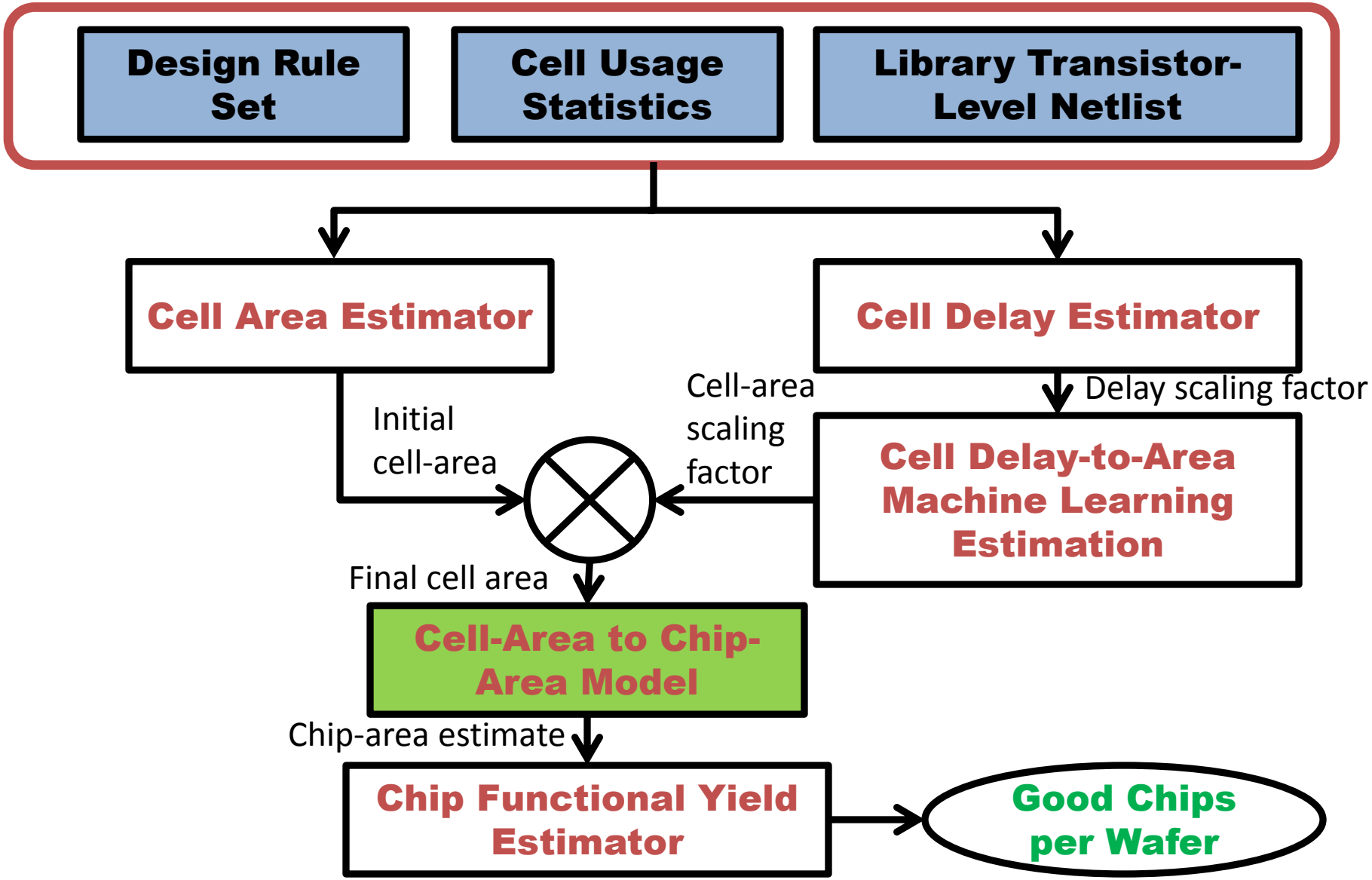

Cell-area to Chip-area Model

- Semi-empirical model to estimate chip-area in terms of cell-area
- Accounts for routing-limited designs
- Coefficients fitted from P&R experiments
  - Use AEGR (Area estimation using Global Routing)
    - Estimate maximum utilization such that design is routable
    - Up to 7x speedup

$$y = x + (y0 - x0) \times \left(\frac{x0}{x}\right)^{\frac{x0}{y0-x0}} \text{ for } x > x0,$$
$$y = y0 \text{ for } x <= x0.$$

x : total cell-area
y : chip-area
x0, y0 : fitting coefficients

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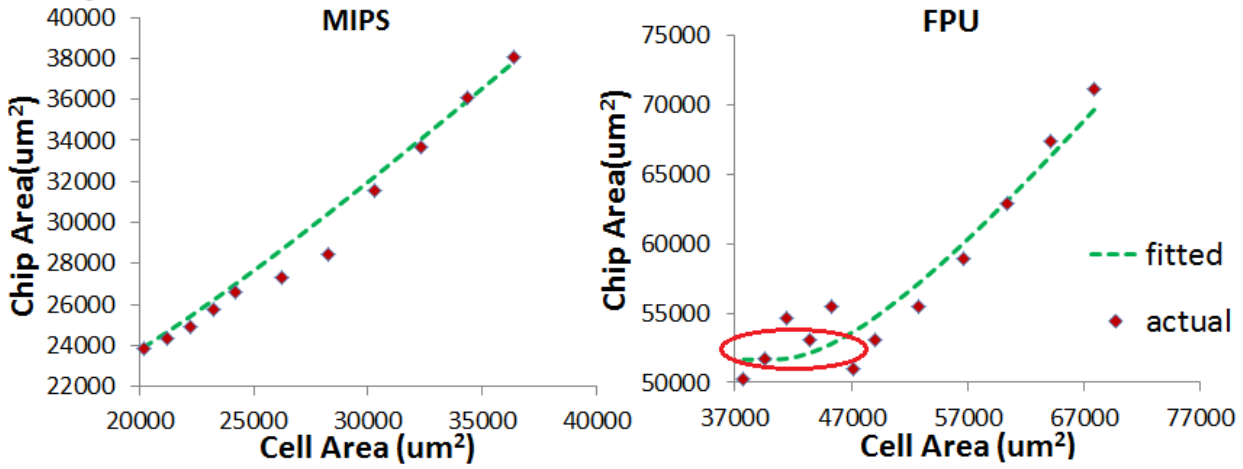

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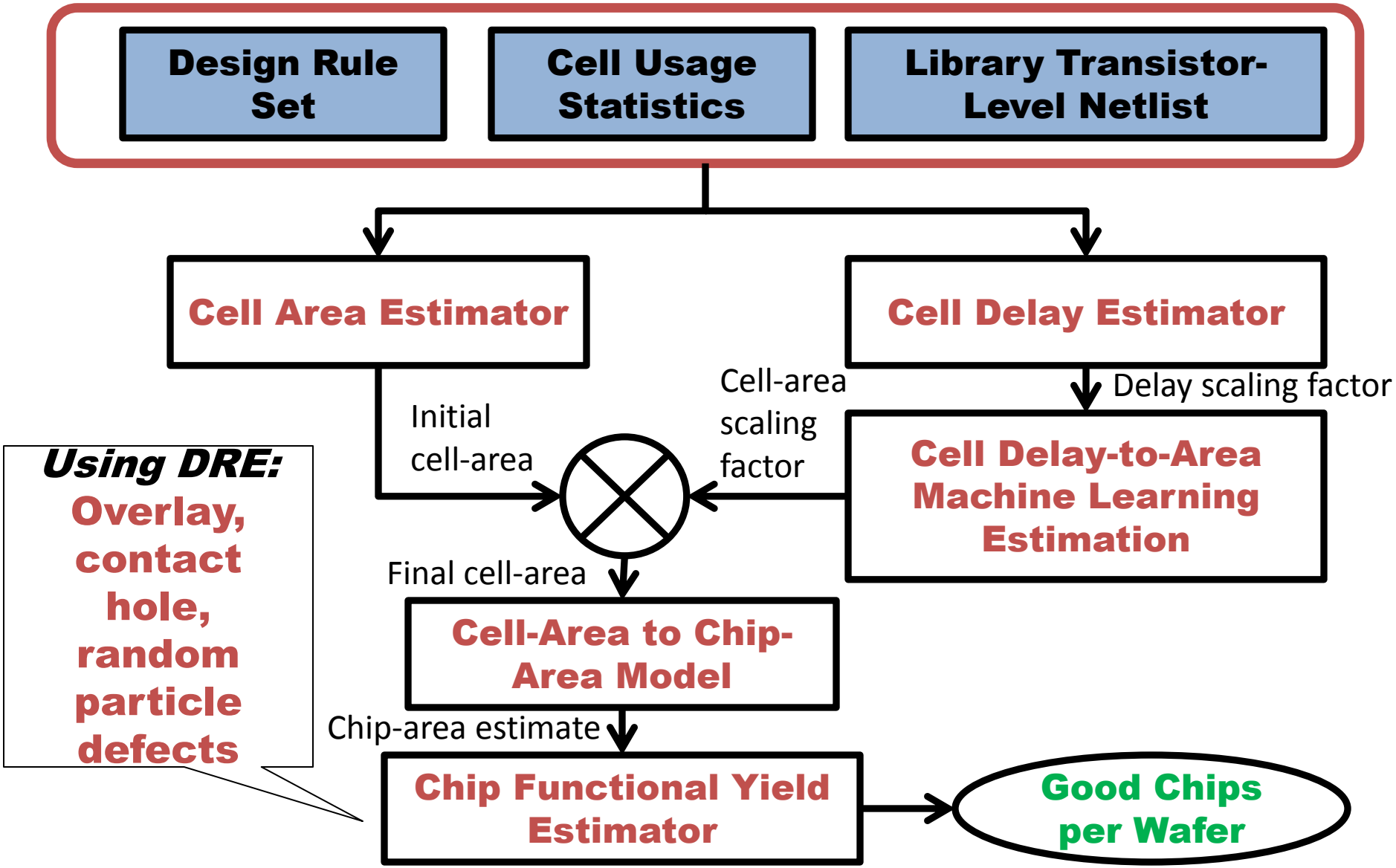
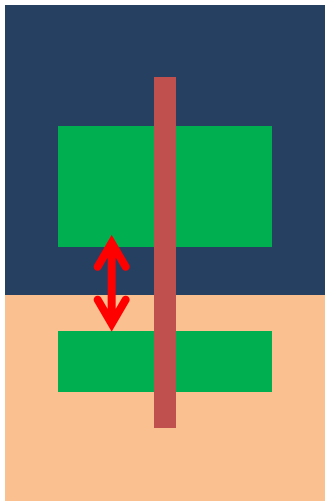
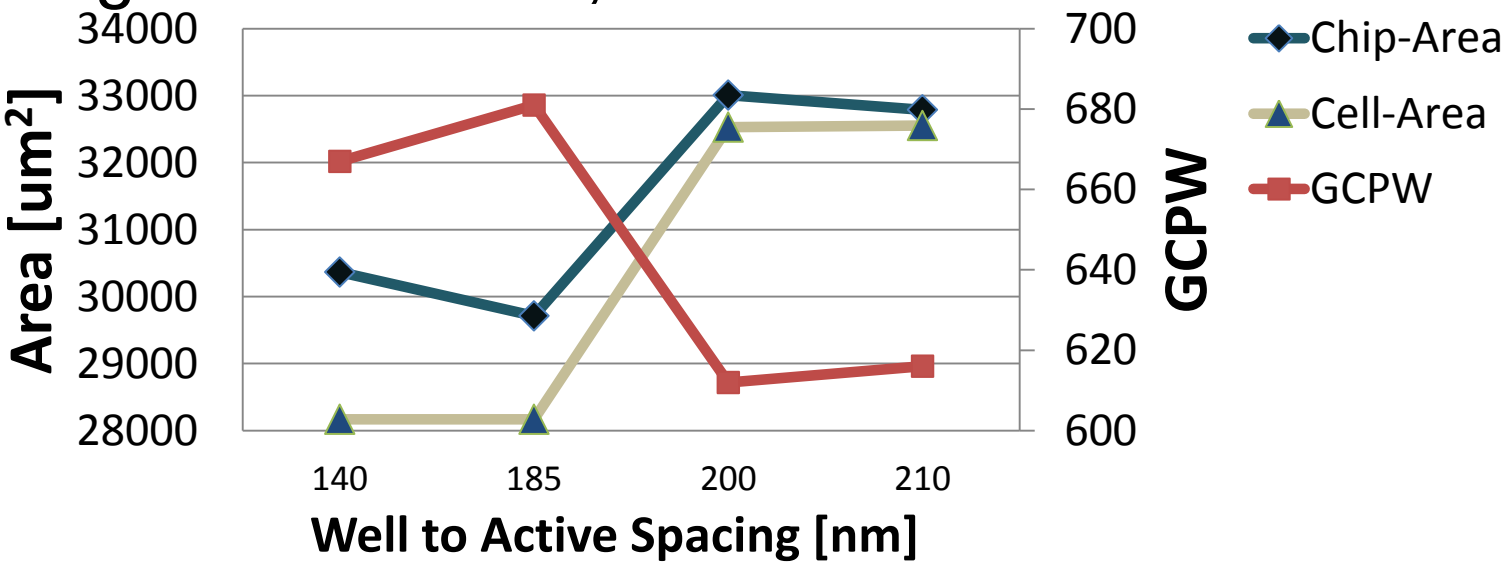


SAMPLE STUDIES USING CHIP-DRE

Well-to-active Spacing Rule Exploration

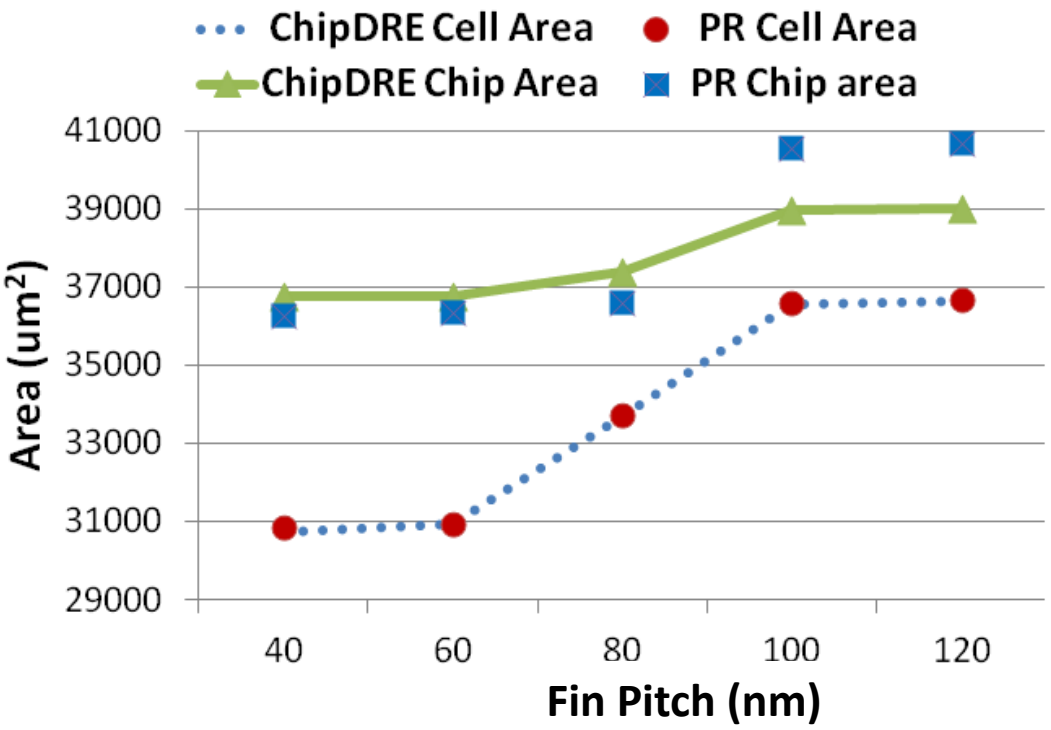
- As Well-to-active spacing rule increases:
  - Cell area increases
  - Cell delay decreases due to well proximity effect
- Dependence of GCPW and chip-area on the rule value is non-monotone!
- Verified against PR runs, with max error of 3%





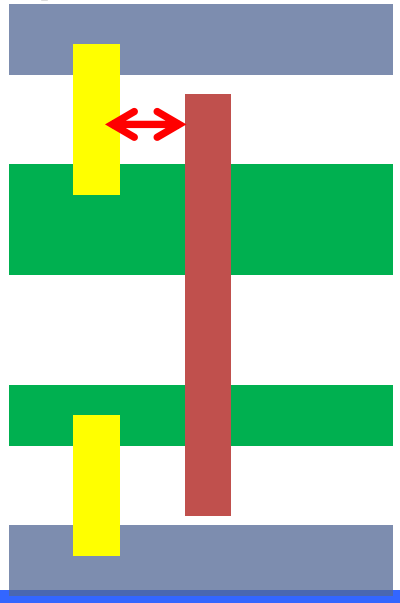
FinFET Fin-Pitch Study

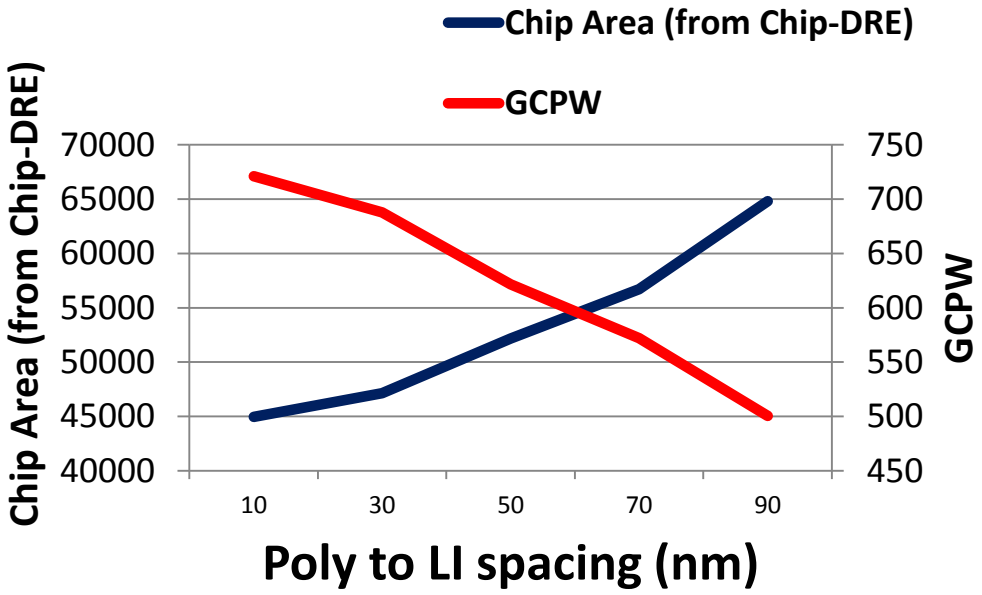
- Fin pitch effect on chip area of FPU
- Fin pitch of 60nm through 100nm, cell area is steeply increasing while chip area is slightly changing
- Error <5%



Local Interconnect-to-poly Spacing Study

- As LI-to-poly space increases
  - Cell area increases
  - Cell delay changes: capacitive coupling decreases but diffusion capacitance may increase
- Study shows cell-area increase dominates over potential chip-area decrease





Conclusion

- Introduced Chip-DRE framework for fast and systematic evaluation of design rules and library architectures at chip-scale

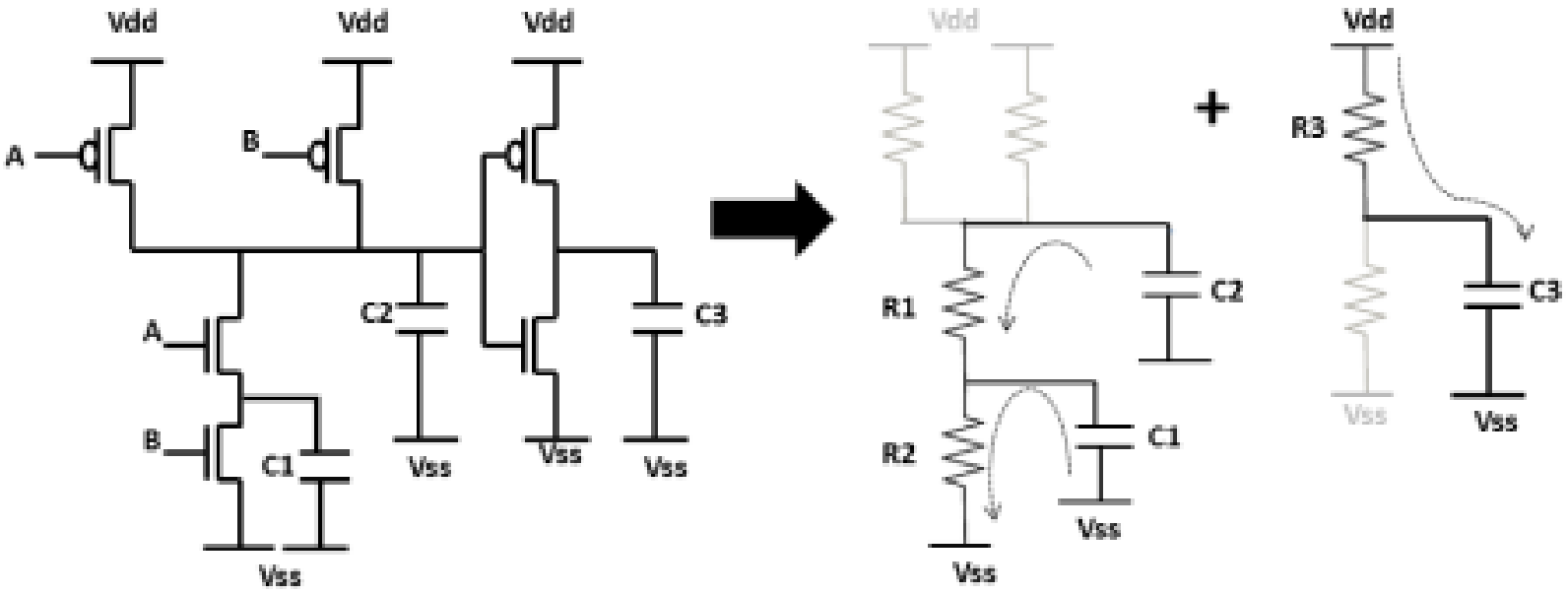
Future Work

- Include Power optimization
- Extend to back-end rules and use Chip-DRE to develop DR and library projections for 5nm node

QUESTIONS ?

BACKUP

Cell Delay Estimation



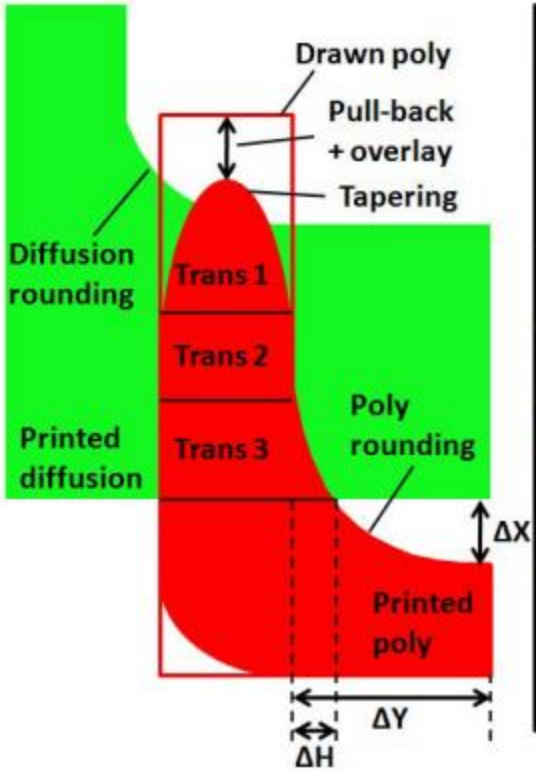
Yield Estimator

- Using **DRE**
- Considers probability of survival from:
  - **Overlay error:** Normal distribution
  - **Random Particle Defects**: Critical area analysis + negative binomial yield model
  - **Contact hole failure**: Poisson distribution

Numeric Results for WPE Experiment

Well-to-active spacing [nm]	Run-time (SPR) [min]	Cell-Area (Chip-DRE)	Chip-Area (Chip-DRE) [um^2]	Chip-Area (SPR) [um^2]	Error [%]	GCPW (Chip-DRE)
140	118	28171	30364	30130	0.8	667
185	356	28171	29709	29460	0.8	681
200	240	32527	33008	33913	-3	612
210	207	32554	32787	33554	-2	616

Variability



Variability

- Current variability index:

$$\Delta\left(\frac{W}{L}\right) = \frac{\sum_{allgates} \left|\Delta\left(\frac{W}{L}\right)_i\right|}{\left(\frac{W_{tot}}{L}\right)_{ideal}}$$

- Modeling delta W/L for each source of variability from literature (tapering, diffusion and poly rounding, CD variability)

Manufacturability

- Manufacturability Index for evaluating DRs is probability of survival (POS) from three major sources of failure
  - contact-defectivity (a.k.a. contact-hole failure);
  - overlay error (i.e. misalignment between layers) coupled with lithographic line-end shortening (a.k.a. pull-back);
  - random particle defects.

Manufacturability (cont'd)

- Contact hole yield follows poisson yield model: Y=Y0*e^(-lambda)
  Lambda is average # failed contacts=# contacts * failure rate.
- Overlay vector components in x and y directions are described by a normal distribution with zero mean & 3σ
- We compute POS from overlay causing: failure to connect between contact and poly/M1/diffusion, gate-to-contact short defect, and always-on device caused by poly-to-diffusion overlay error
- For failure caused by random particles, critical area analysis for open and short defects at M1/poly/contact layers and short defects between gates and diffusion-contacts.
- Yield=yield_contact*yield_overlay*yield3_randomParticles;