

Toward Efficient Programming of Reconfigurable Radio Frequency (RF) Receivers

Jun Tao, Ying-Chih Wang, Minhee Jun,
Xin Li, Rohit Negi, Tamal Mukherjee and
Lawrence T. Pileggi

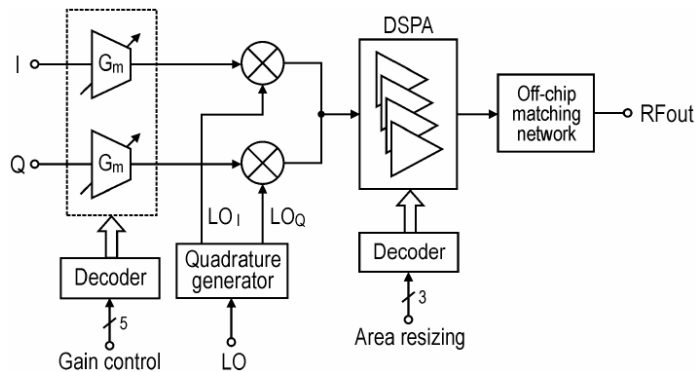


Outline

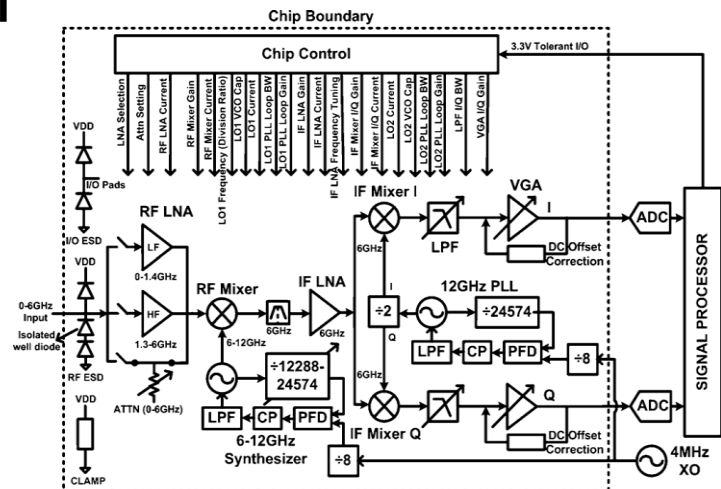
- Background
- Problem formulation
- Proposed method
- Numerical results
- Conclusion

Background

- Remarkable growth of wireless chip design cost
 - New wireless standards
 - Autonomous applications
 - Aggressive miniaturization
- Reconfigurable RF system



Reconfigurable ultra-low power RF transmitter (F. Carrara, et al., *IEEE RFIC Symposium*, 2010)



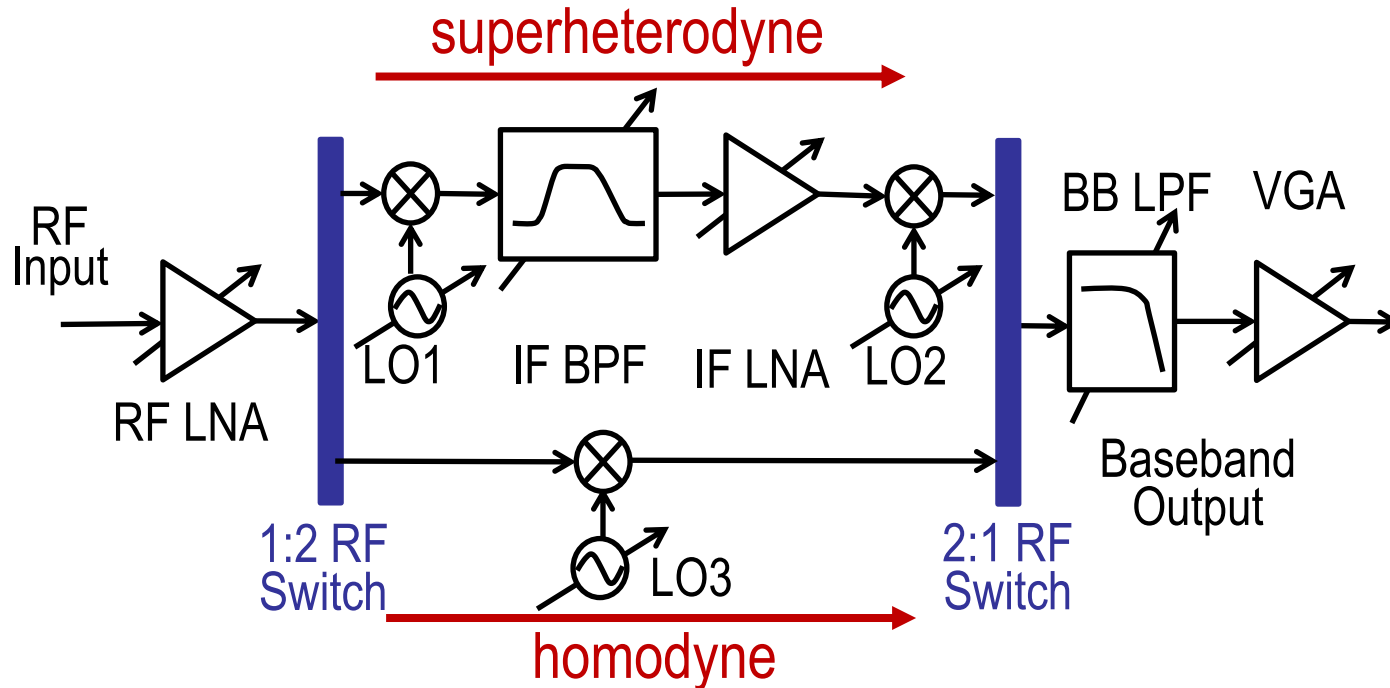
0-6GHz reconfigurable vector signal analyzer and software-defined receiver (A. Goel, et al., *IEEE Trans. on MTT*, 2012)

Background

- Reconfigurable RF system programming
 - Find the optimal configurations for all circuit blocks → meet the given system-level specifications
- Traditional analog optimization methods
 - Equation-based algorithms: equations are difficult to derive and may not be sufficiently accurate
 - Simulation-based algorithms: time-consuming
- A new optimization approach is required
 - **Robustness** → close to global optimum
 - **Efficiency** → low computational cost

Problem Formulation

- Reconfigurable RF system programming



- System-level programming → system architecture
 - System-level programmable knobs: e.g., switch box
- Block-level programming → block performances
 - Block-level programmable knobs: e.g., bias current for LNA

Problem Formulation

- Reconfigurable RF system programming

$$\begin{aligned} \min_{\mathbf{x}, \mathbf{y}} \quad & F(\mathbf{x}, \mathbf{y}) \\ \text{s.t.} \quad & g_j(\mathbf{x}, \mathbf{y}) \geq G_j \quad (j = 1, 2, \dots, J) \end{aligned}$$

↓ Simplify the programming problem

$$\begin{aligned} \min_{\mathbf{x}, \mathbf{y}} \quad & F(\mathbf{x}, \mathbf{y}) \\ \text{s.t.} \quad & S(\mathbf{x}, \mathbf{y}) = \min(g_1(\mathbf{x}, \mathbf{y}) - G_1, \dots, g_J(\mathbf{x}, \mathbf{y}) - G_J) \geq 0 \end{aligned}$$

$F(\bullet)$ and $g_j(\bullet)$ are system level performance metrics

- System-level programming → system architecture
 - System-level programmable knobs: **x**
- Block-level programming → block performances
 - Block-level programmable knobs: **y**

Proposed Method

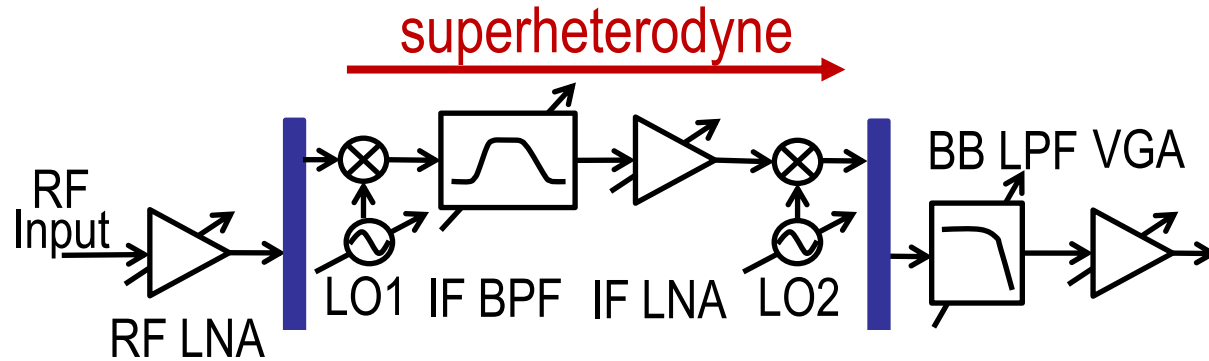
- For different architectures
 - Optimal block-level implementations are different

$$\begin{array}{ll} \min_{\mathbf{x}, \mathbf{y}} & F(\mathbf{x}, \mathbf{y}) \\ \text{s.t.} & S(\mathbf{x}, \mathbf{y}) = \min(g_1(\mathbf{x}, \mathbf{y}) - G_1, \dots, g_J(\mathbf{x}, \mathbf{y}) - G_J) \geq 0 \end{array}$$

- Proposed multi-architecture programming method
 - Step 1: block-level optimization
 - For each possible architecture, find out the optimal configurations of its circuit blocks
 - Step 2: system-level optimization
 - Compare all possible architectures and select the optimal one

Local Relaxation

- Consider local relaxation for block-level optimization



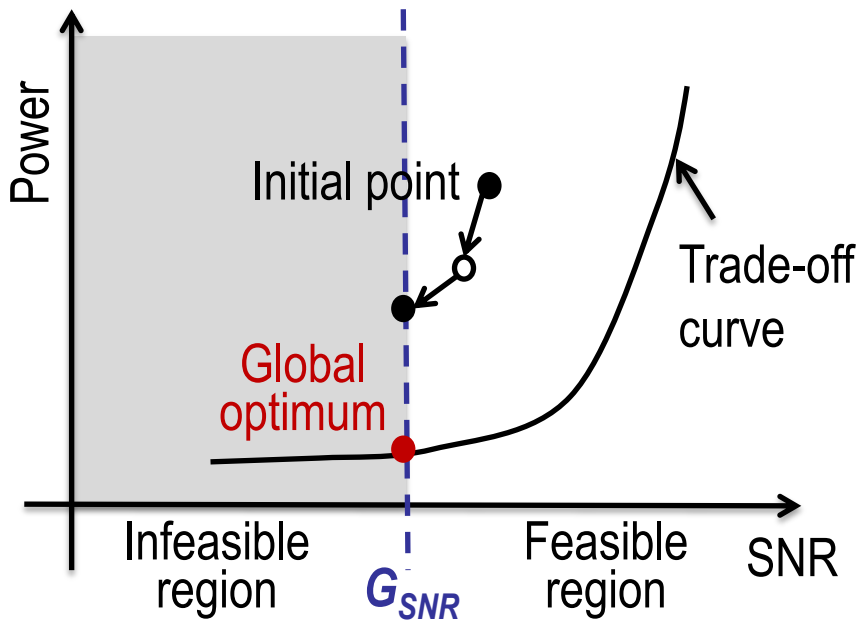
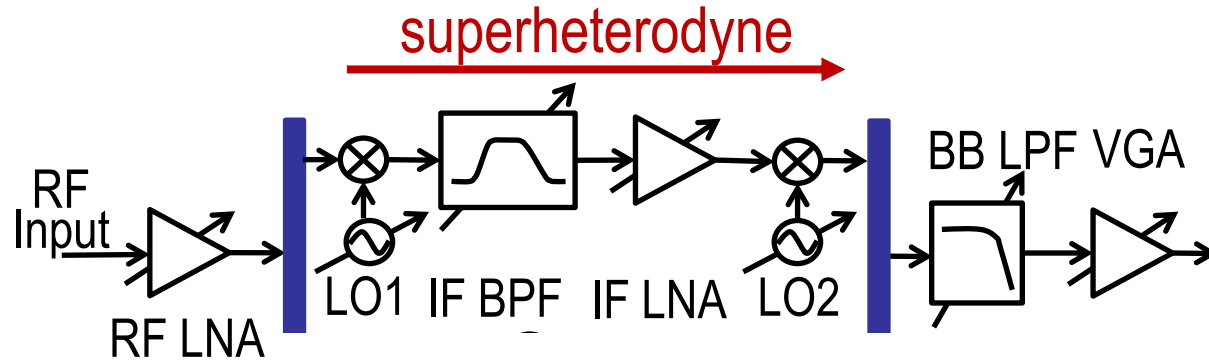
Search for the optimal RF LNA among all possible configurations satisfying the constraints with minimal cost function

Search for the optimal IF BPF among all possible configurations satisfying the constraints with minimal cost function

⋮

Search for the optimal VGA among all possible configurations satisfying the constraints with minimal cost function

Local Relaxation



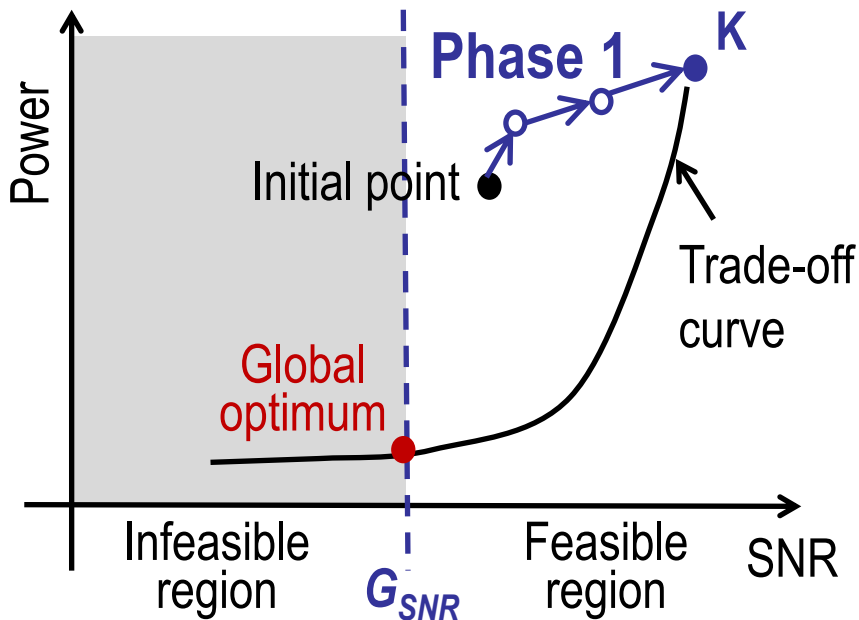
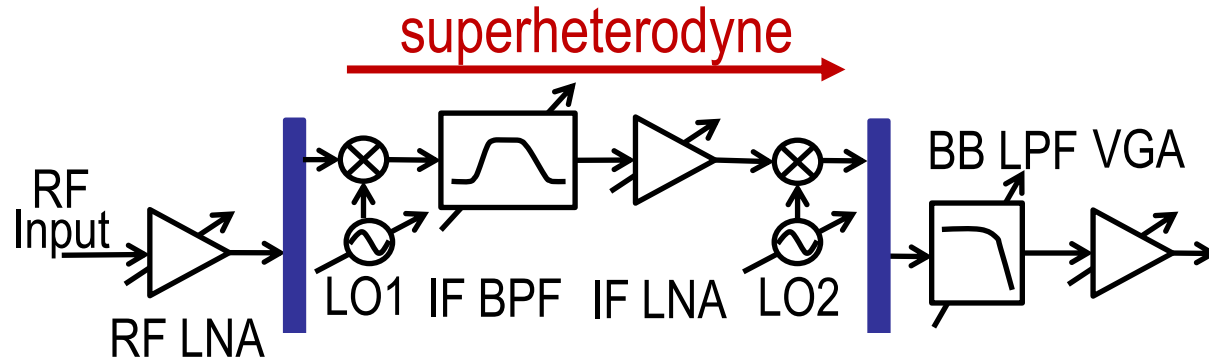
Cost function $F(\bullet)$: Power

Constraint function $g(\bullet)$: SNR

Local relaxation

- Initial point is close to G_{SNR} → a lot of configurations of a GIVEN block are considered to be 'infeasible'.
- It fails to converge to global optimum

Two-phase Relaxation Search



- Phase 1: maximize constraint function (SNR) w/o considering the cost function

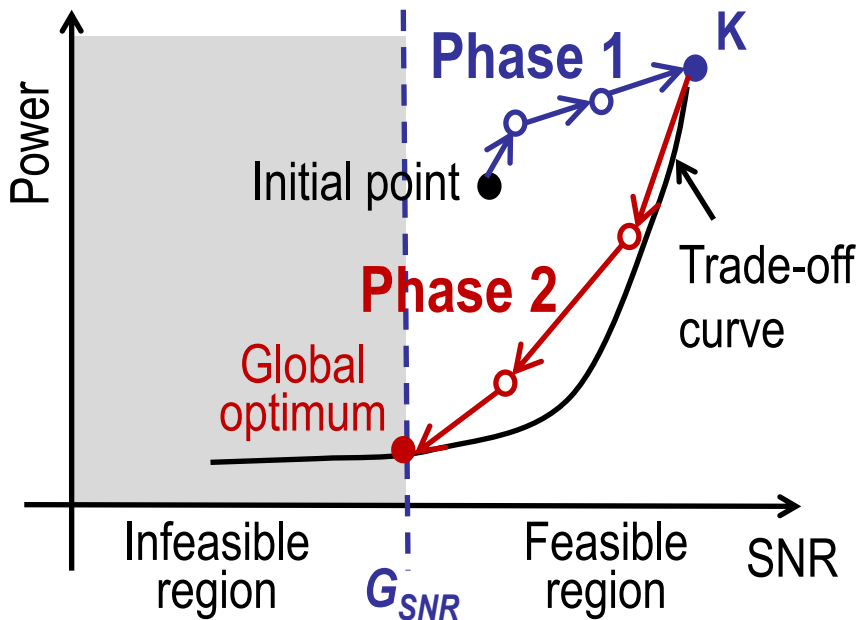
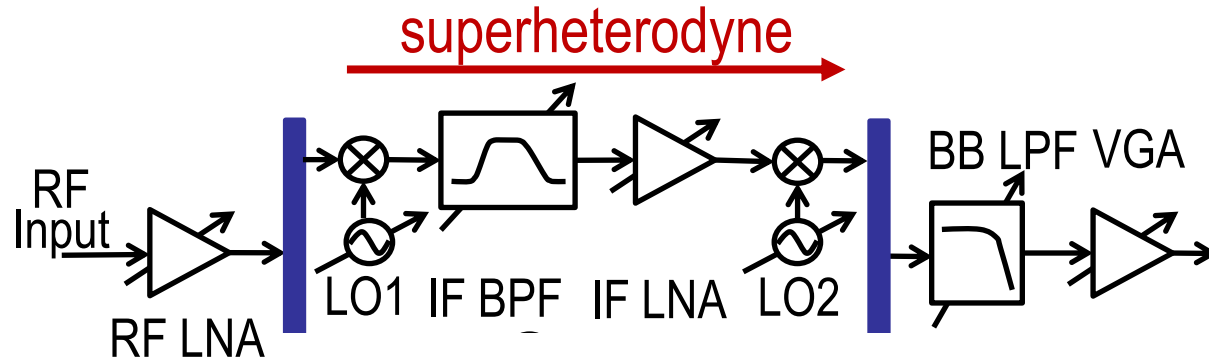
Optimize RF LNA to maximize SNR

Optimize IF BPF to maximize SNR

⋮

Optimize VGA to maximize SNR

Two-phase Relaxation Search

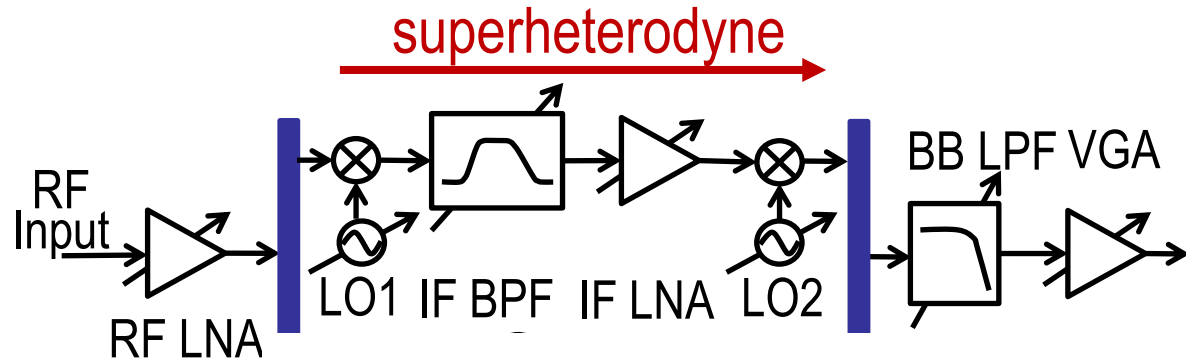
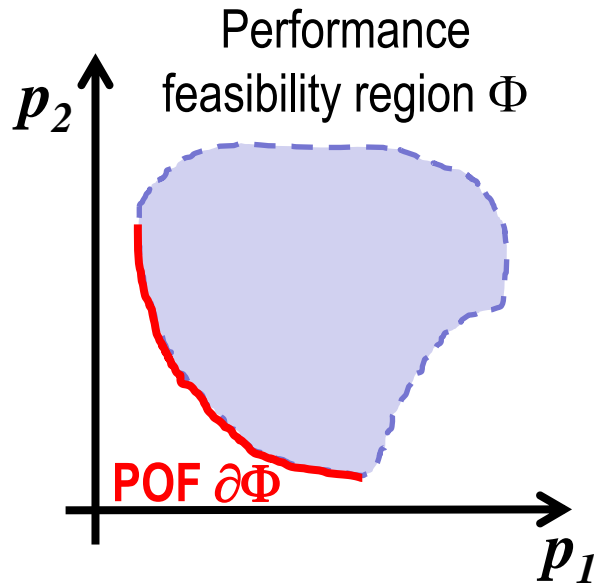


- **Phase 2:** minimize cost function subject to the given constraints
 - Similar as local relaxation
 - Use **K** as the initial point \rightarrow far from $G_{SNR} \rightarrow$ a lot of configurations of a GIVEN block now become 'feasible'
 - Avoid a lot of local optima

Search Space Reduction

- Computational cost of the proposed two-phase relaxation is dominated by system simulation time
 - More than 10 minutes are required for each simulation
- Search space reduction
 - Remove the block configurations that cannot be the optimal choice in Phase 1 and Phase 2
- Pareto optimal front (POF)
 - Boundary of feasible performance region
 - Previously developed for analog system-level optimization

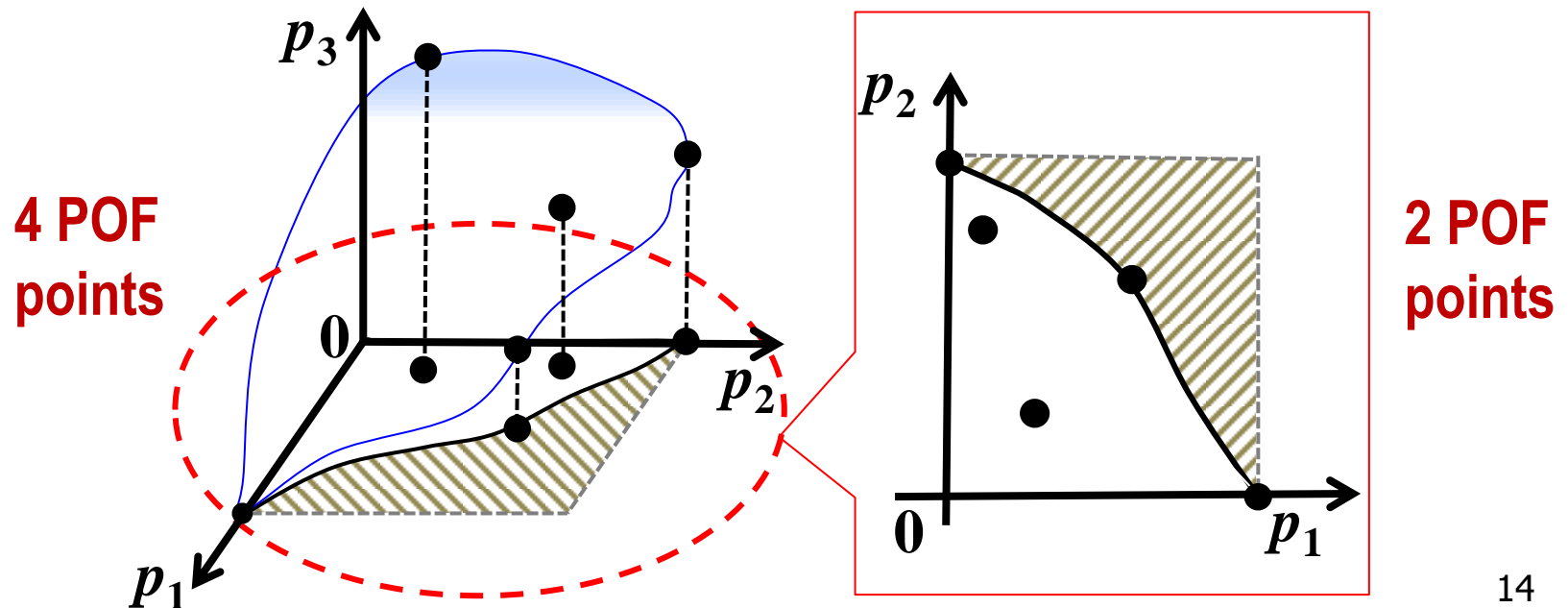
Pareto Optimal Front



- Only the configurations on POF of circuit blocks could result in the optimal performance of RF receiver
 - Maximize SNR \rightarrow RF LNA with large **gain**, low **NF** and large **IIP3** \rightarrow only consider the configurations on the POF with respect to **gain**, **NF** and **IIP3**

Pareto-driven Search Space Reduction

- Two-phase relaxation search
 - Phase 1: maximize constraint function w/o considering the cost function
 - Ignore the block-level performance metrics which only affect the cost function → reduce the number of configuration candidates

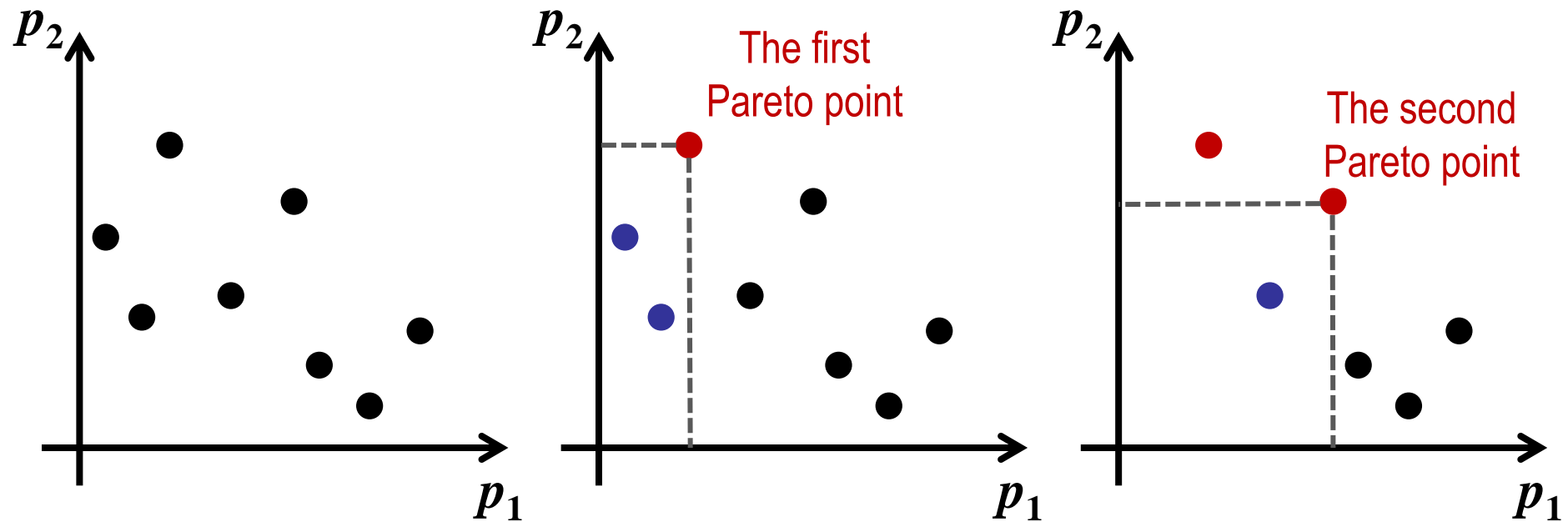


Pareto Points Selection

All configuration points for one block

1. Choose the performance point that has the greatest value for p_2
2. Remove all other points that are dominated by this selected one

1. Choose the performance point that has the greatest value for p_2 from the remaining candidates
2. Remove all other points that are dominated by this selected one



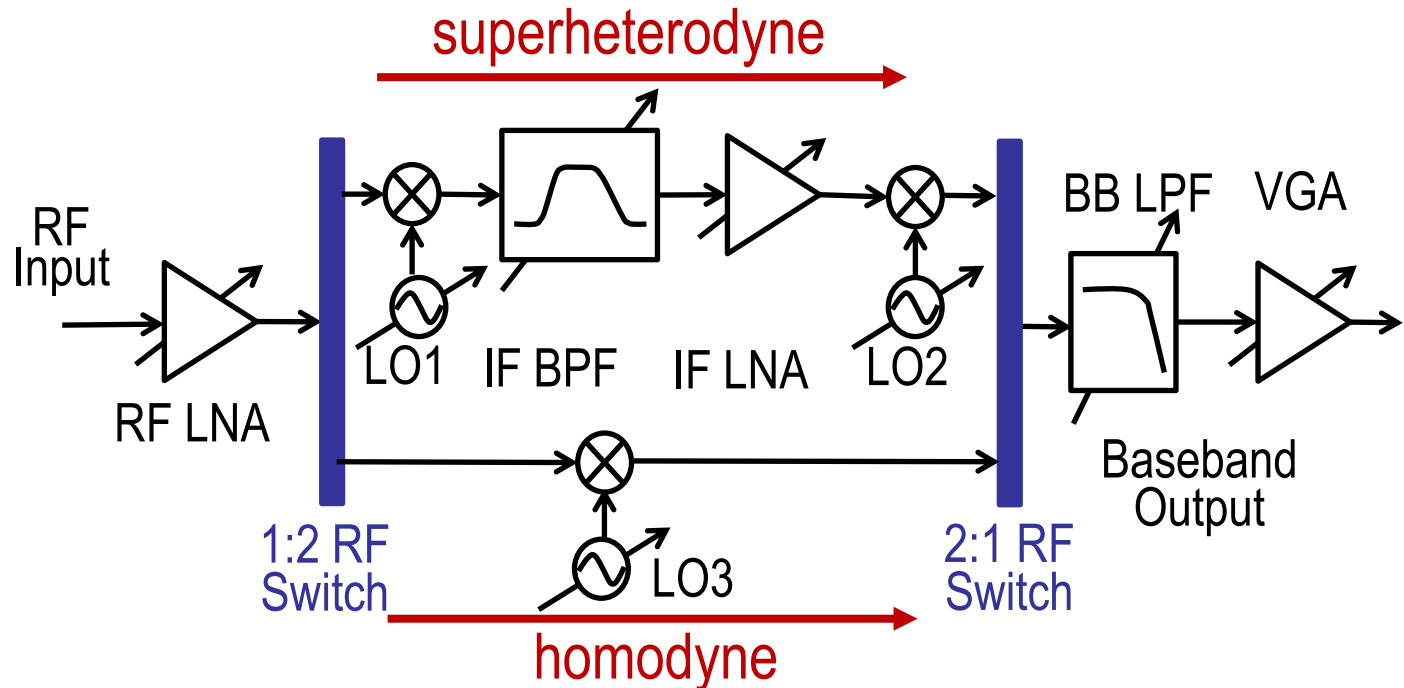
Continue the iterations until only Pareto points remain

Summary

$$\begin{aligned} \min_{\mathbf{x}, \mathbf{y}} \quad & F(\mathbf{x}, \mathbf{y}) \\ \text{s.t.} \quad & S(\mathbf{x}, \mathbf{y}) = \min(g_1(\mathbf{x}, \mathbf{y}) - G_1, \dots, g_J(\mathbf{x}, \mathbf{y}) - G_J) \geq 0 \end{aligned}$$

- For each architecture
 - Select the Pareto points for each block without considering the cost function
 - **Phase 1:** maximize the constraint function based on these selected Pareto points
 - **Phase 2:** minimize the cost function subject to the given constraints
- Determine the optimal receiver architecture that can achieve the minimal cost subject to the given constraints

Numerical Results



- IEEE 802.11a WLAN standard where the channel bandwidth is 20MHz
- Minimize power (cost function) subject to a given SNR specification (constraint function)
- RF LNA and IF LNA: 11 configurations (gain, NF, IIP3 and power)
- IF BPF: 9 configurations (bandwidth and unloaded quality factor)
- 1100 possible configurations in total for this RF receiver example

Numerical Results

| SNR Spec (dB) | Algorithm | SNR (dB) | Power (mW) | Selected Arch |
|---------------|-----------------|--------------|-------------|---------------|
| 6 | Exhaustive | 7.36 | 1.32 | HD |
| | Relaxation | 7.36 | 1.32 | HD |
| | Annealing | 7.36 | 1.32 | HD |
| | Proposed | 7.36 | 1.32 | HD |
| 8 | Exhaustive | 8.61 | 1.44 | SH |
| | Relaxation | 8.61 | 1.44 | SH |
| | Annealing | 8.61 | 1.44 | SH |
| | Proposed | 8.61 | 1.44 | SH |
| 9 | Exhaustive | 9.53 | 2.04 | SH |
| | Relaxation | 9.66 | 2.60 | HD |
| | Annealing | 9.53 | 2.04 | SH |
| | Proposed | 9.53 | 2.04 | SH |
| 10 | Exhaustive | 10.51 | 3.32 | SH |
| | Relaxation | failed | failed | failed |
| | Annealing | 10.51 | 3.32 | SH |
| | Proposed | 10.51 | 3.32 | SH |

Programming results with different SNR specifications

- Exhaustive: exhaustive search
 - Relaxation: local relaxation
 - Annealing: simulated annealing
 - Proposed: proposed method
-
- HD: homodyne
 - SH: superheterodyne

The proposed algorithm converges to the global optima in all test cases

Numerical Results

| SNR Spec (dB) | Exhaustive | Relaxation | Annealing | Proposed |
|---------------|------------|------------|-----------|----------|
| 6 | 1100 | 32 | 170 | 35 |
| 8 | 1100 | 32 | 179 | 34 |
| 9 | 1100 | 36 | 331 | 34 |
| 10 | 1100 | 36 | 259 | 40 |

The number of required simulations with different SNR specifications

- Exhaustive search and simulated annealing: a large number of simulations are required to reach convergence
- Proposed method and local relaxation: 5× speed-up over exhaustive search
- Pareto-based search space reduction: further reduce the number of required simulations by more than 80

Conclusion

- Reconfigurable RF receiver programming
 - Minimize cost function
 - Subject to a set of given constraints
- Two-phase relaxation search & Pareto-based search space reduction
 - Robustness → close to global optimum
 - Efficiency → low computational cost
- Future work: further apply the proposed CAD algorithm to large reconfigurable RF systems with more than two system performance specifications

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Thank you