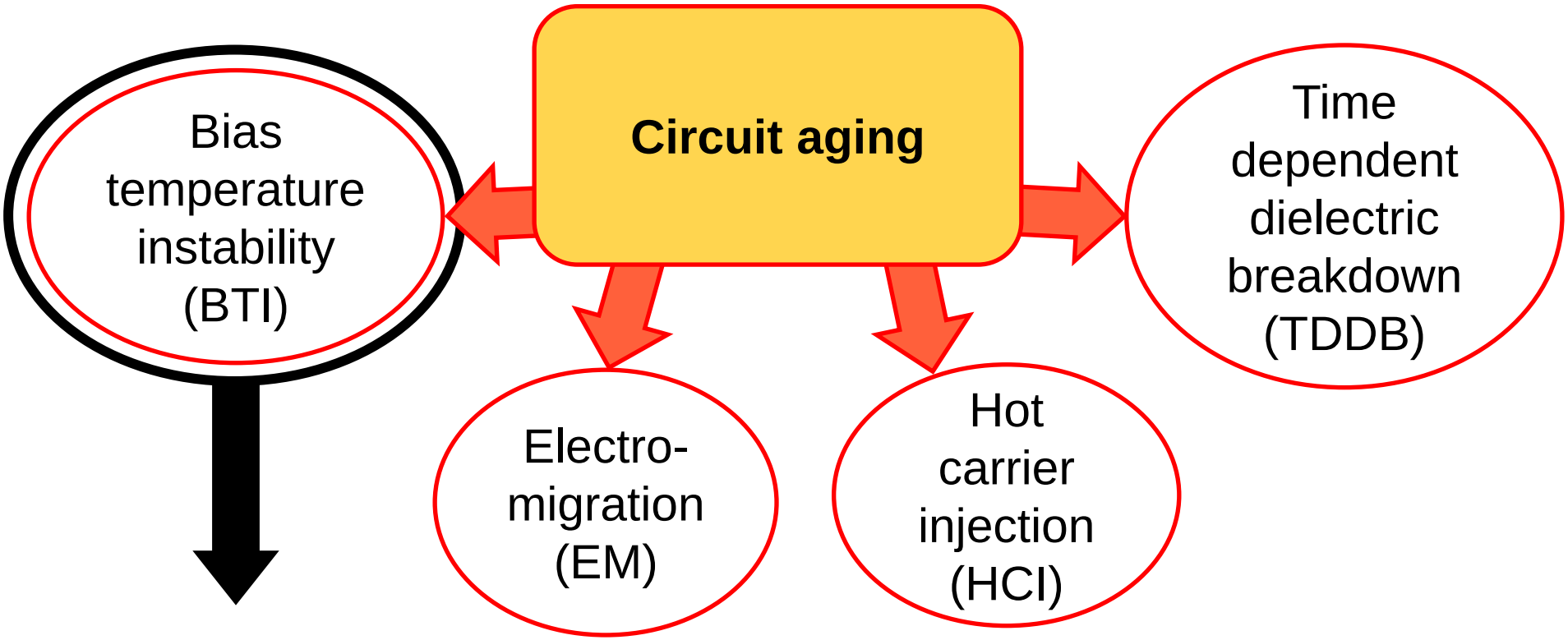
Predicting Circuit Aging Using Ring Oscillators

Deepashree Sengupta
Sachin S. Sapatnekar
Department of Electrical and Computer Engineering
University of Minnesota

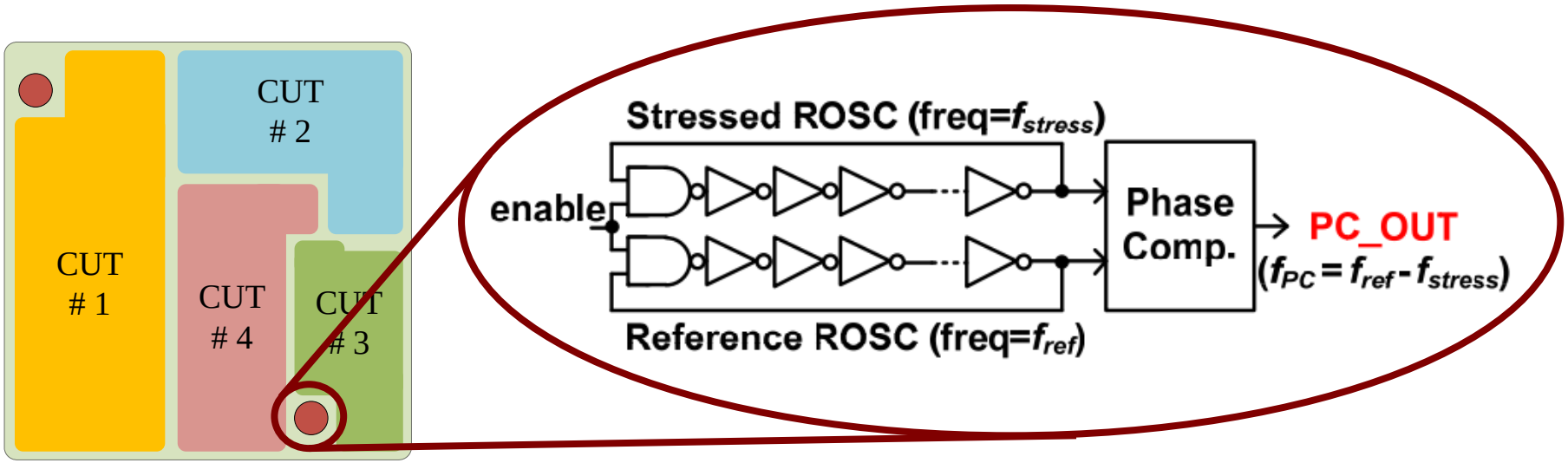
Introduction



- Predominant.
- Increases V_{th}, thus decreasing maximum frequency, f_{Max} of circuits.
- Aging in PMOS by negative BTI, in NMOS by Positive BTI.

Contribution

- Predict circuit aging using delay degradation data of on-chip ring oscillators (ROSC).



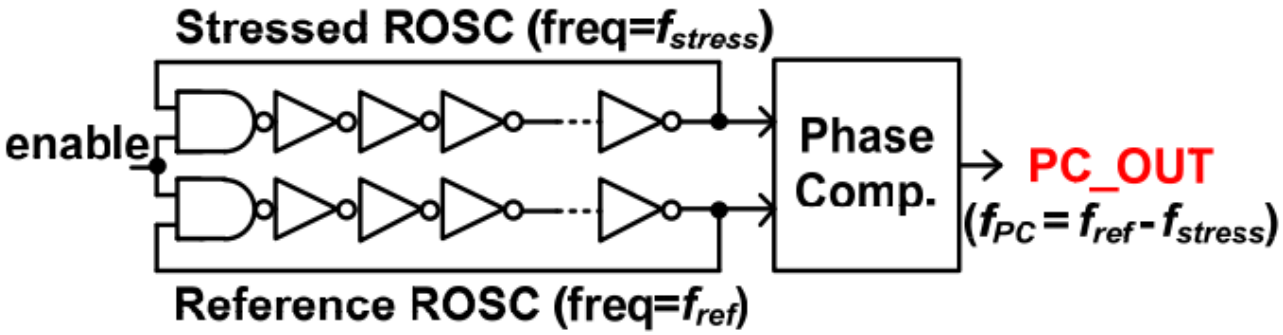
[Kim, ISVLSI07]

- ROSC degradation measured by beat frequencies with respect to a reference ROSC [Lu (IBM), IRPS13].

- Infer delay degradation of circuit under test (CUT) from ROSC.

Why ROSC ?

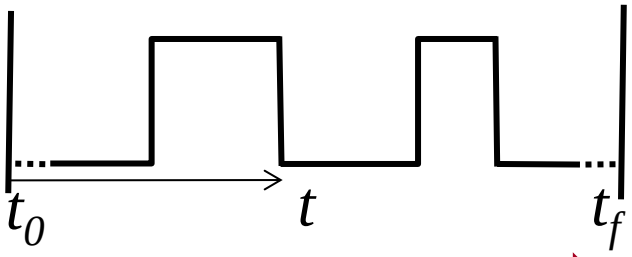
- Pros
  - Small and easily repeatable.
  - Easy to lay out.
  - Easy to measure $\Delta D_{ROSC}(t)$ using phase comparator as shown:



[Kim, ISVLSI07]

- Cons
  - Measuring ROSC is not equivalent to measuring CUT.
  - Needs calibration to be used as aging sensor.

BTI aging



Fresh Device
$D(t_0) = g(V_{th}(t_0))$

Degraded Device
$D(t) = g(V_{th}(t))$

$\Delta V_{th,n}(t) = K_1\, h(\xi_1)\, f(t)$: Positive BTI

$\Delta V_{th,p}(t) = K_2\, h(\xi_2)\, f(t)$: Negative BTI

ξ_1 and ξ_2 are probabilities that the signal is high and low, respectively.

Thus, $D(t) = D(t_0) + \left.\frac{\partial g}{\partial V_{th}}\right|_{V_{th}(t_0)} \underbrace{Kh(\xi)\left(f(t) - f(t_0)\right)}_{\Delta V_{th}(t)}$

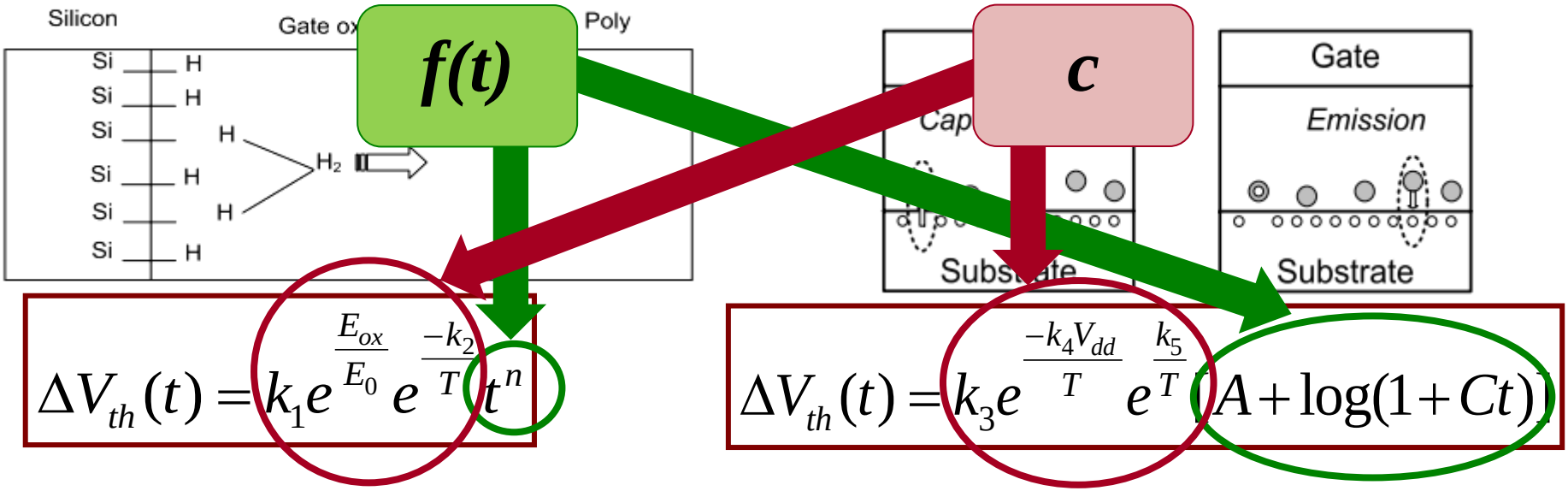
S c

What is $f(t)$, c?

- $f(t)$, c depend on aging mechanism:

Reaction-Diffusion (RD) model

Charge-Trapping (CT) model



$$\Delta V_{th}(t) = k_1 e^{\frac{E_{ox}}{E_0}} e^{\frac{-k_2}{T}} t^n$$

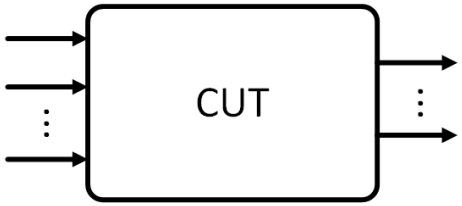
$$\Delta V_{th}(t) = k_3 e^{\frac{-k_4 V_{dd}}{T}} e^{\frac{k_5}{T}} [A + \log(1+Ct)]$$

- Delay degradation from t_0 to t:

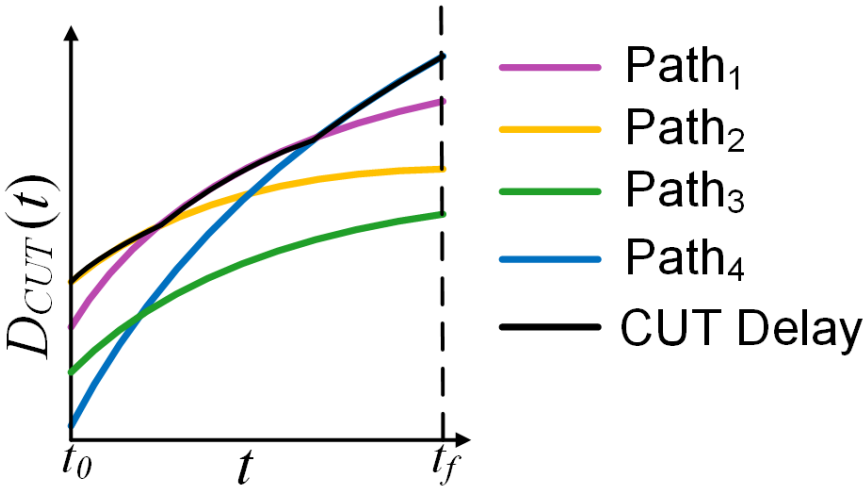
$$\Delta D(t) = k\left(f(t) - f(t_0)\right); \quad k = c\left.\frac{\partial g}{\partial V_{th}}\right|_{V_{th}(t_0)}$$

k: aging sensitivity, depends on T, V_{dd} and ξ.

BTI aging of critical paths



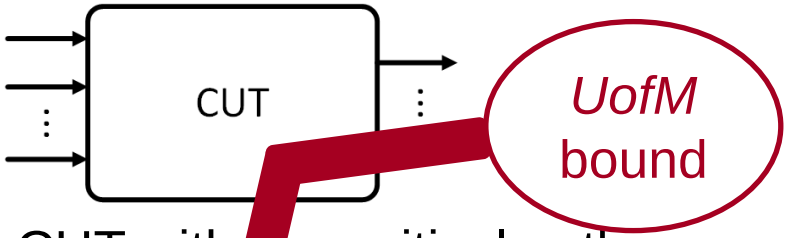
For CUT with four critical paths



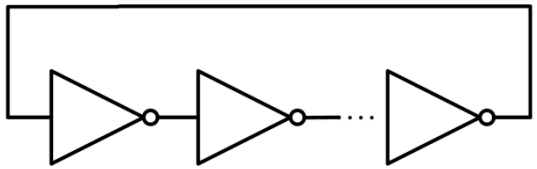
- Critical paths may change during lifetime.
- CUT delay: piecewise smooth curve.

Multiple critical paths crossover

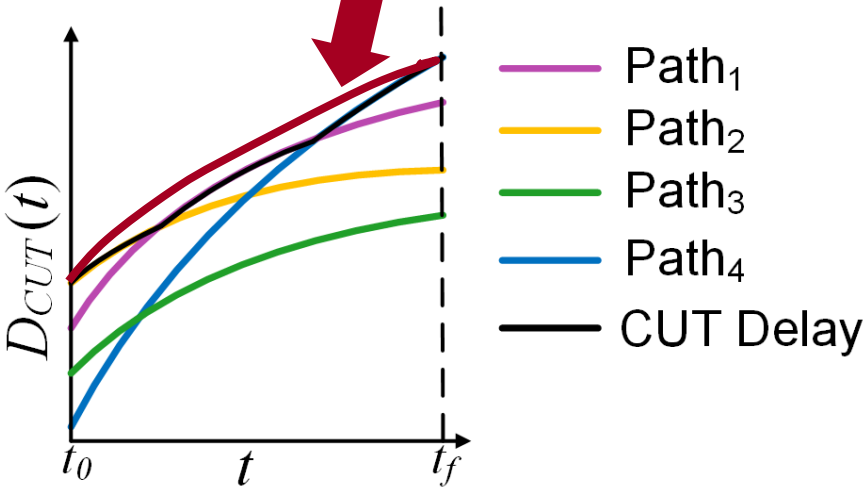
Issues with ROSC based aging estimation

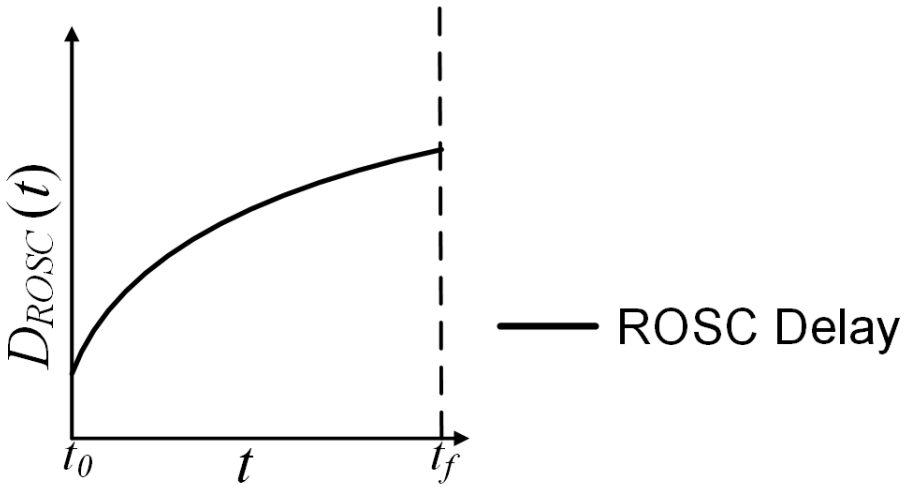


For CUT with four critical paths



For ROSC with one path



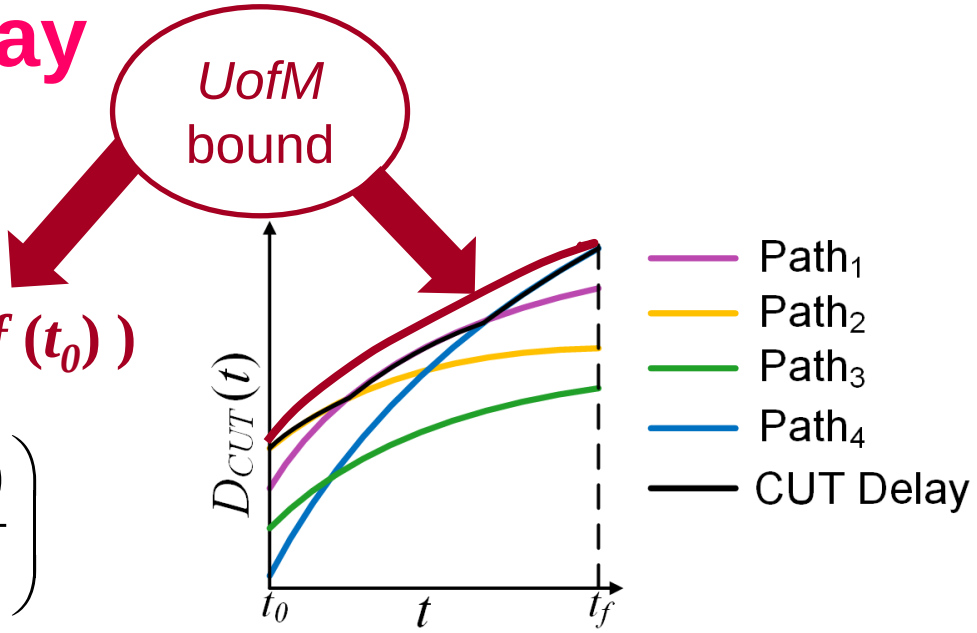


Variable aging sensitivities

Constant aging sensitivity

CUT delay approximated by analytical bound, called the *Upperbound on* f_{Max} (*UofM*) bound of delay.

UofM bound of delay



$$D_{CUT}(t)=D_{CUT}(t_0)+k_{CUT}(f(t)-f(t_0))$$

$$k_{CUT}=\frac{D_{CUT}(t_f)-D_{CUT}(t_0)}{f(t_f)-f(t_0)}$$

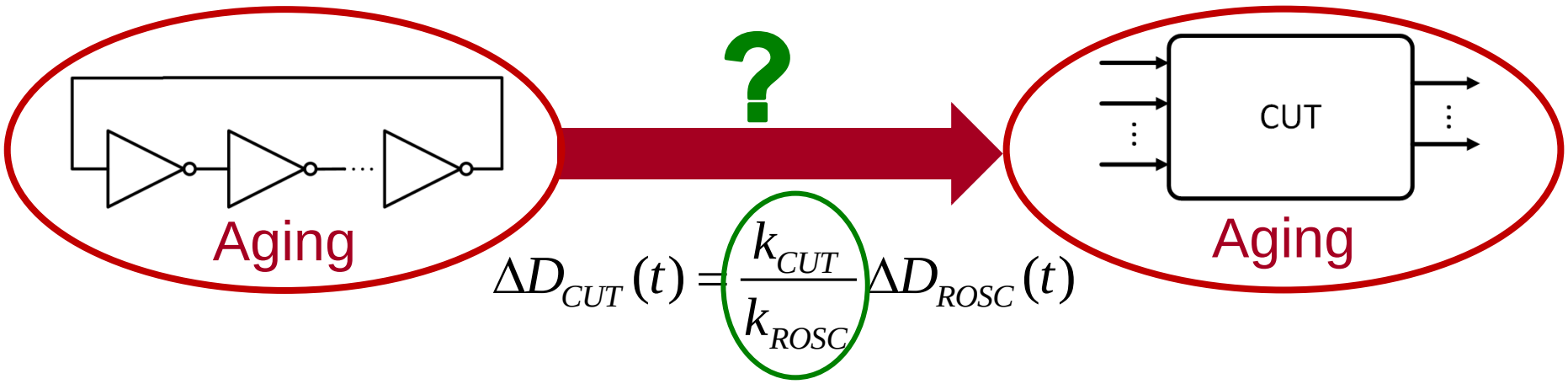
$D_{CUT}(t_0)$, $D_{CUT}(t_f)$: by performing STA on CUT at t_0 and t_f.

$f(t_0)$, $f(t_f)$: computed analytically; ξ= 0.95 for both NBTI and PBTI.

ROSC: $D_{ROSC}(t)=D_{ROSC}(t_0)+k_{ROSC}(f(t)-f(t_0))$

CUT delay degradation from ROSC

$$\Delta D_{CUT}(t) = k_{CUT}\,(f(t) - f(t_0)); \quad \Delta D_{ROSC}(t) = k_{ROSC}\,(f(t) - f(t_0))$$



$$\Delta D_{CUT}(t) = \frac{k_{CUT}}{k_{ROSC}} \Delta D_{ROSC}(t)$$

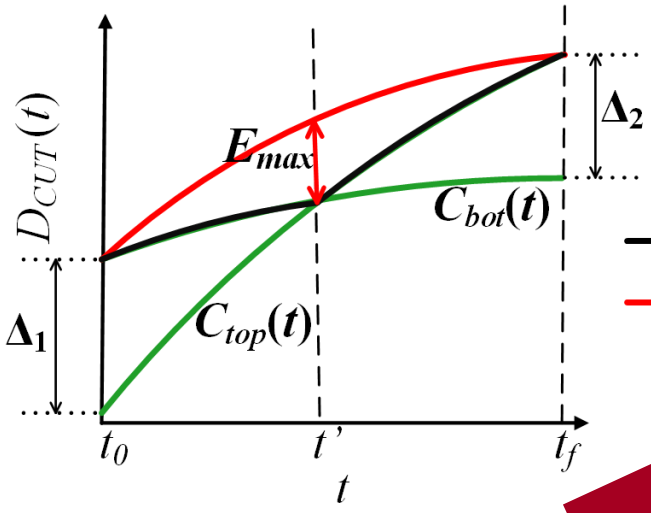
Degradation Ratio, $\mathcal{D}$

Features of $\mathcal{D}$:

- Independent of t, T and V_{dd}.
- CUT with one dominant critical path: true $\Delta D_{CUT}(t)$.
- CUT with multiple critical paths: pessimistic $\Delta D_{CUT}(t)$.

Maximum pessimism in *UofM* bound

- Generate CUT with two paths:
  - Path$_1$ ($C_{bot}(t)$): gates with minimum aging sensitivity, k_1
  - Path$_2$ ($C_{top}(t)$): gates with maximum aging sensitivity, k_2
- Adjust number of stages so that $\Delta_1 = \Delta_2$ (see figure).



True delay

UofM bound

$$E_{\max} = \frac{(k_2 - k_1)\left(f(t_f) - f(t_0)\right)}{4}$$

Maximum fractional error, depends on gate library

$$E_{frac} = \frac{E_{\max}}{C_{top}(t')} = \frac{4E_{\max}^2}{d_1 d_2 \left(\frac{k_2}{d_2} - \frac{k_1}{d_1}\right)\left(f(t_f) - f(t_0)\right)}$$

Experimental setup

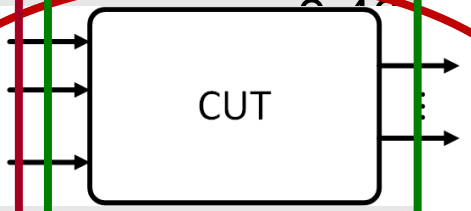
Gate functionalities	• INV, BUF, 2 & 3-input NAND, NOR, 3 & 4-input AOI: each X1, X2 and X4
Gate library	• NanGate 45nm Open Cell Library
Transistor model	• 45nm Predictive Technology Model
Benchmark circuits	• ISCAS'89, ITC'99 synthesized in Synopsys Design Compiler
Machine used	• 64-bit Ubuntu server (Intel® Core™2 Duo CPU E8400 3GHz)

- RD Model of BTI aging: $f(t) = ct^{1/6}$
- Bound on maximum pessimism by *UofM* bound (E_{frac}): 3.59%
- Lifespan of CUT: 10 years (beyond 3 months of burn-in)

Degradation ratio for various CUTs

CUT	No. of gates	$\mathcal{D}$	Error (%)	Runtime (s)
s5378	690	1.51	0.17	0.50
s13207	590	1.68	0.00	
	336	1.95	0.00	
S_{mult}			0.00	
			0.09	1.75
			0.00	1.69
			0.00	1.99
			0.00	5.18
			0.00	16.95
b	128494	11.89	0.00	31.64
b21	24080	12.25	0.00	6.09
b22	36149	12.23	0.00	8.38

$\mathcal{D}$



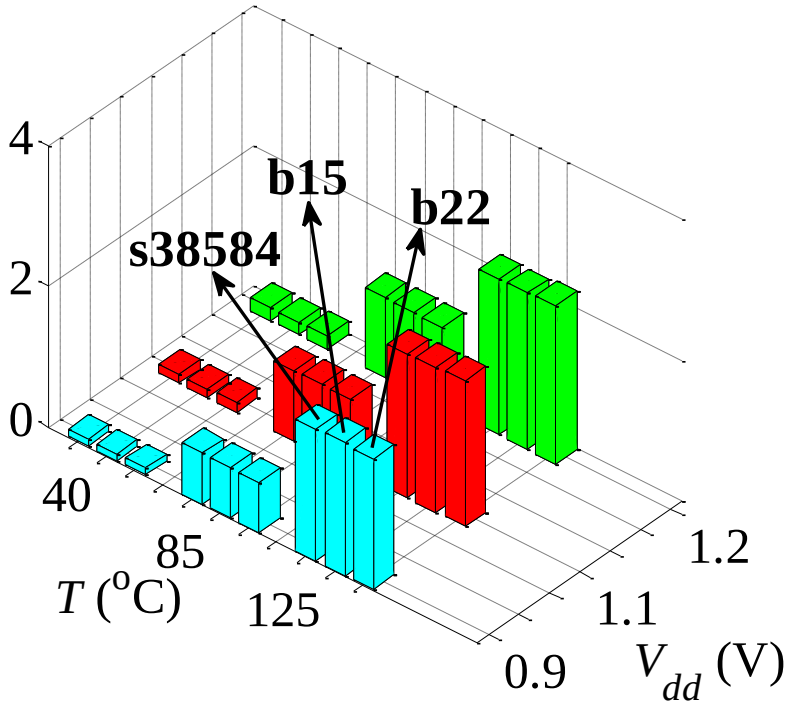
Aging

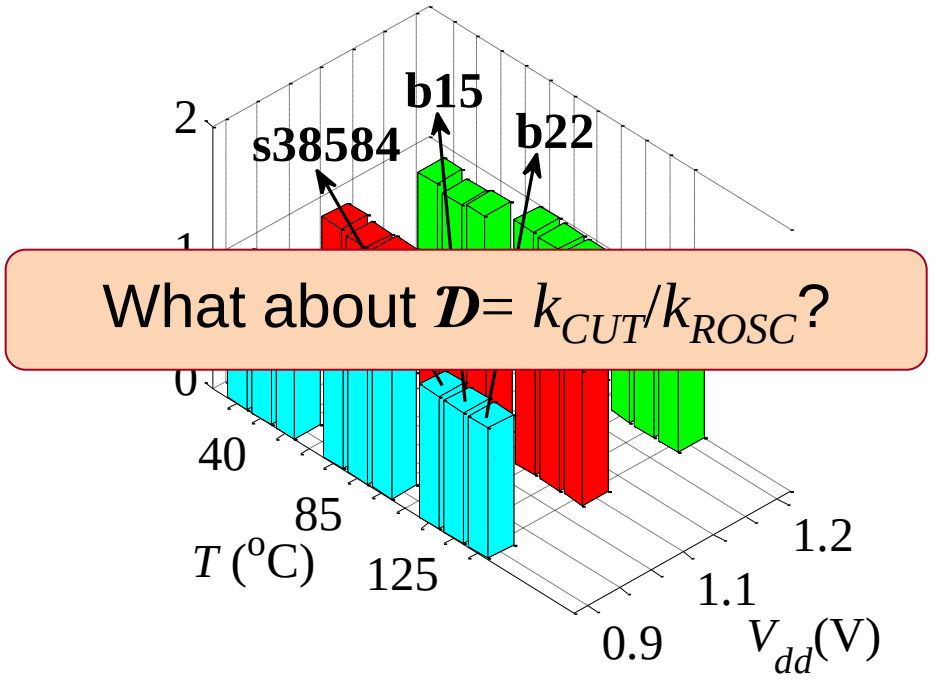
- Practically, observed pessimism is negligible.
- Modest runtime: scalable to large CUTs.

Temperature and V_{dd} independence

k_{CUT}: dependent on T and V_{dd}

$\mathcal{D}$: independent of T and V_{dd}



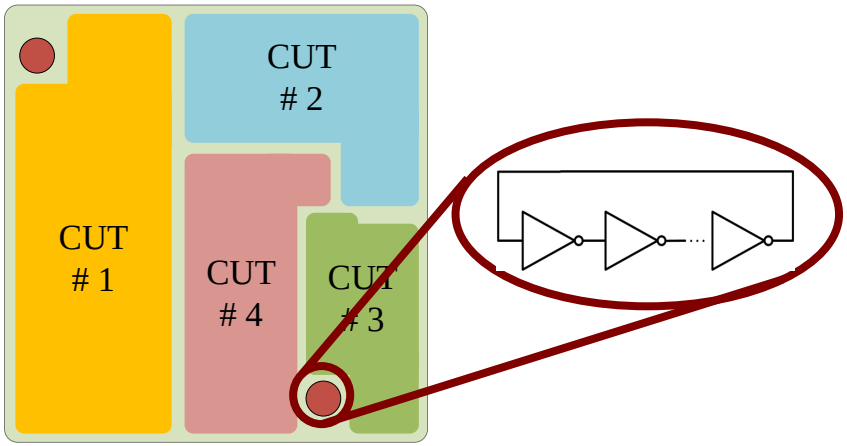


What about $\mathcal{D} = k_{CUT}/k_{ROSC}$?

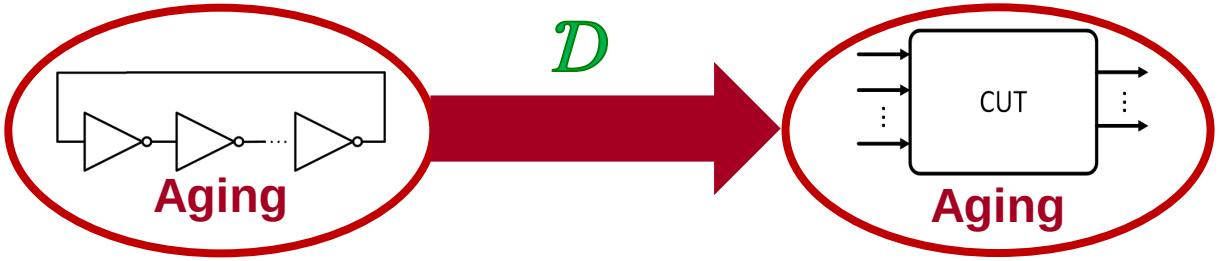
- Single $\mathcal{D}$ for a CUT irrespective of operating conditions.

Conclusion

- BTI induced aging: signal probability dependent, captured by *UofM* bound.
- On-chip ROSC as aging sensor:



- Degradation ratio, $\mathcal{D}$ transforms ROSC aging to CUT aging.



- Single constant predicts aging at all operating conditions.

THANK YOU