Efficient Simulation-Based Optimization of Power Grid with On-Chip Voltage Regulator

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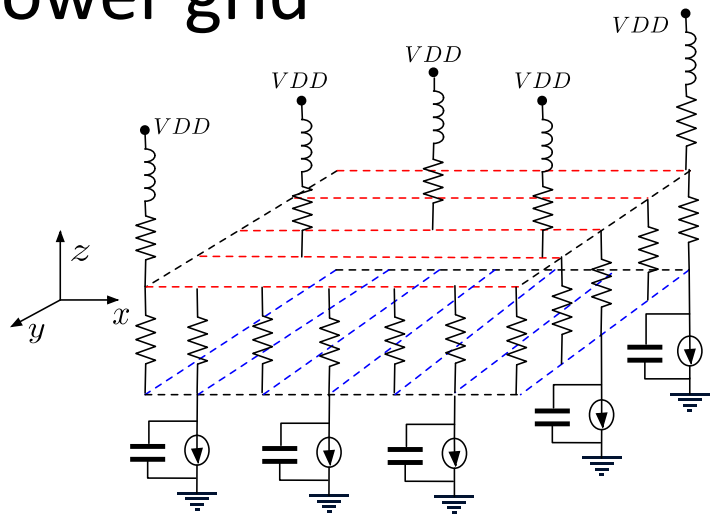
Power Grid and IR-drop

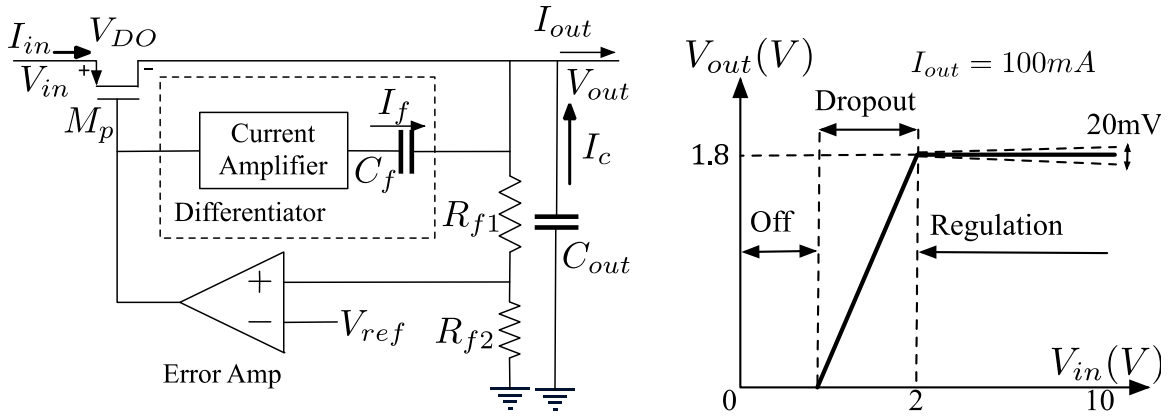
- An example power grid



- IR-drop
  - Due to impedance of power grid, devices' nodes get less voltage values than that of power supply
  - Increase circuit delay and deteriorate timing
  - To generate reliable circuit, maximum IR-drop value should be less than 10% of power supply
- It is important to optimize power grid to meet the IR-drop constraint.

On-Chip Low-Dropout Voltage Regulator(LDO)

- LDO is a nonlinear and active device
- It is proven that the LDO improves load regulation and eliminates load-transient spikes

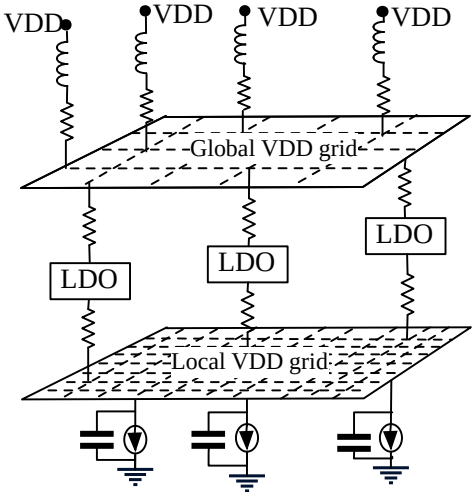


On-chip LDO structure and characteristic curve

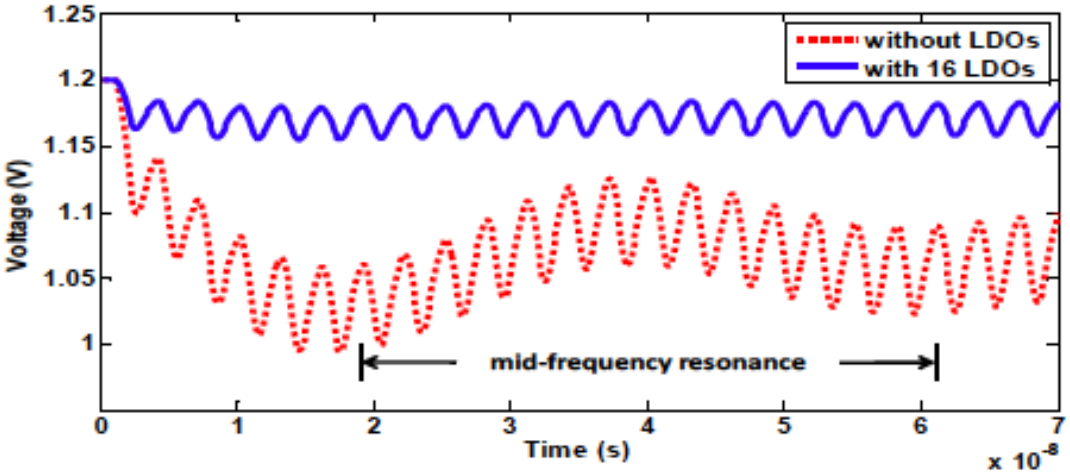
- It is promising to integrate the LDOs into power grid to reduce IR-drop values

Integrate LDOs into Power Grid (1)

- Power grid with LDO integration



Power grid with LDOs



Voltage values of a node with/without LDOs

- Previous work
  - Based on even distribution, it is demonstrated that integrating on-chip LDOs reduces both high and mid-frequency switching noises caused by resonance

Integrate LDOs into Power Grid(2)

- Limited by available white space, the most effective locations of the LDOs depends on the devices' switching activities

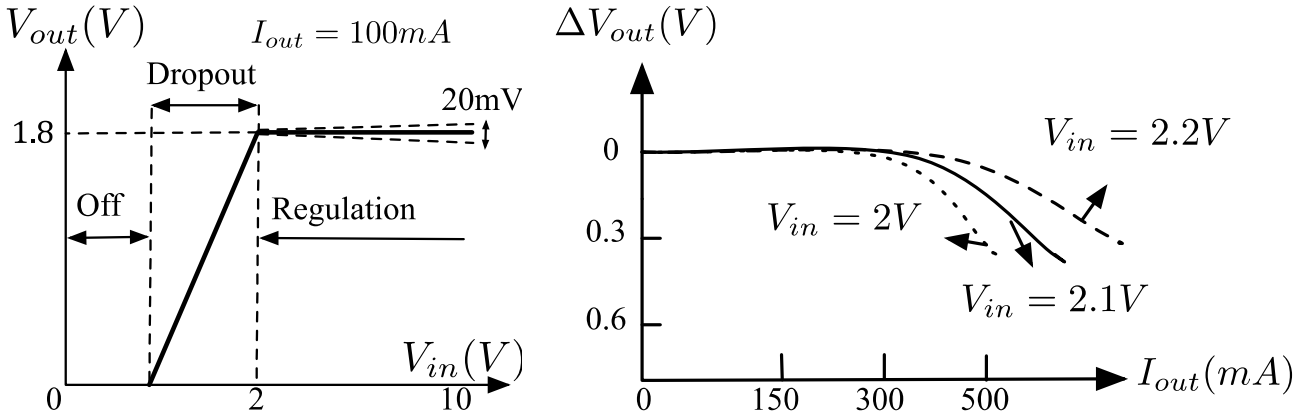
- It is necessary to optimize the IR-drop values considering uneven distribution of the LDOs
- It is very challenging to meet the IR-drop constraint by adding a set of on-chip LDOs
  - Simulation of power grid with LDO is difficult
    - No effective numerical computational model for LDO
  - Find the effective location for the LDOs
  - Effective flow is required to reduce the runtime of the optimization

Our Simulation-Based Approach

- Considering the chip white space and devices' switching, we develop an efficient method to integrate on-chip LDOs into power grid to meet the IR-drop constraint
  - We propose a hybrid simulation flow to address the simulation difficulty of power grid and LDOs
  - We propose an effective simulation flow to add LDOs to meet the IR-drop constraint
  - The LDOs are set at the locations that can effectively reduce the IR-drop values of power grid

Supply Voltage of Power Grid

- LDO has a voltage drop
- Larger input voltage is more resistive to the output current change, but results in less efficiency of LDO

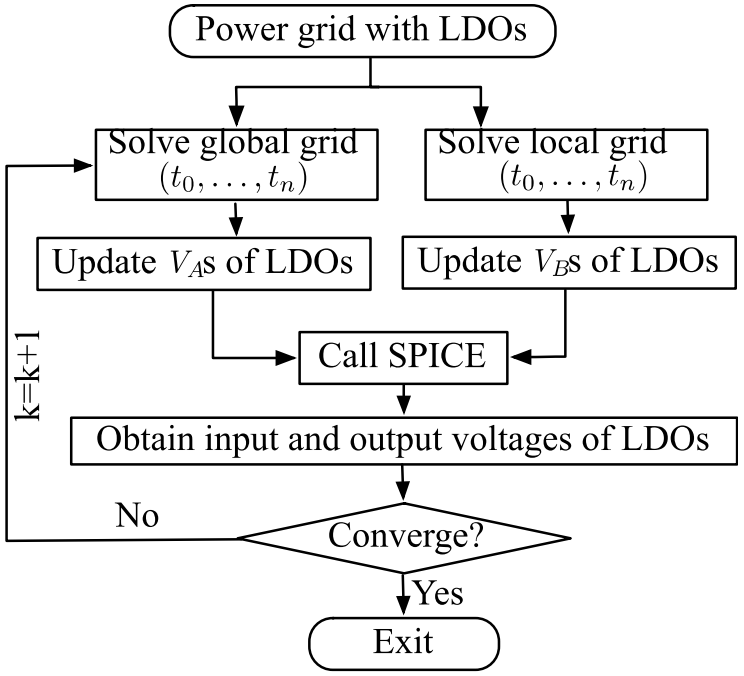


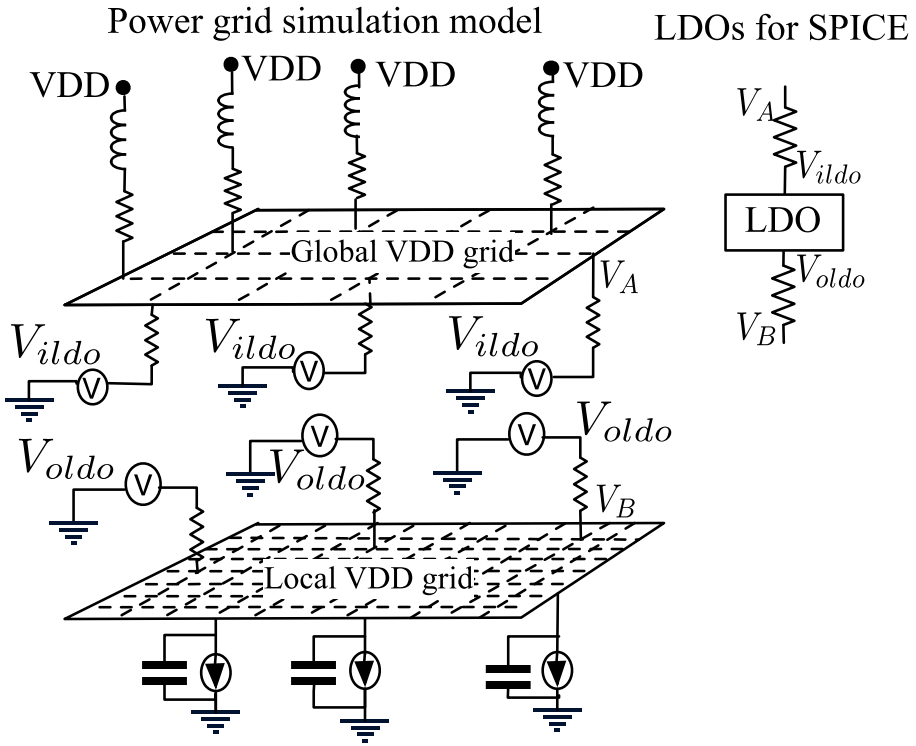
Voltage drop of LDO varies with the output current

- Use 2.2V power supply for global power grid. Ideally, local power grid gets 1.8V as the power supply

Simulating Power Grid with LDO

- Hybrid simulation model
  - Divide power grid into global grid and local grid
  - Treat LDOs as voltage sources for global and local power grids
- Simulation flow

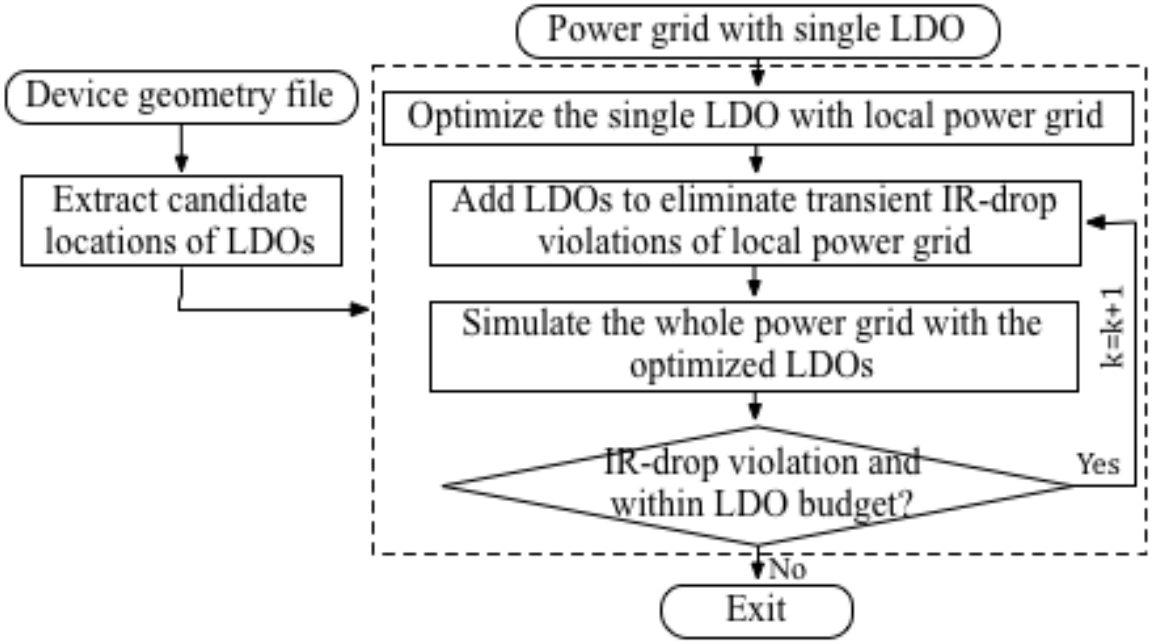




Hybrid simulation model

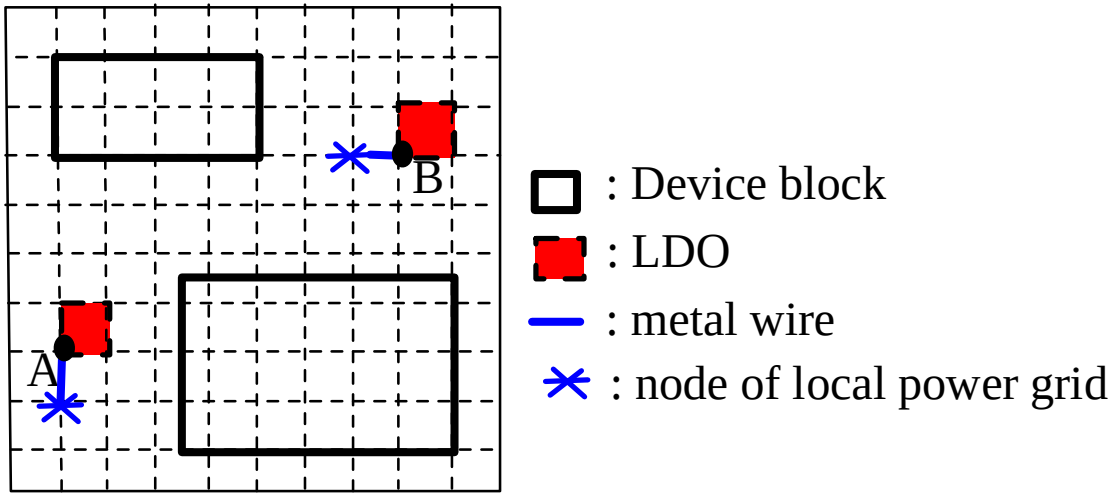
Optimize LDOs to Meet IR-drop Constraint

- Optimization flow
  - Extract candidate locations of the LDOs
  - Optimize the location of the initial single LDO
  - Utilize local power grid to add LDOs
  - Simulate both local and global power grids with LDOs to verify the solutions



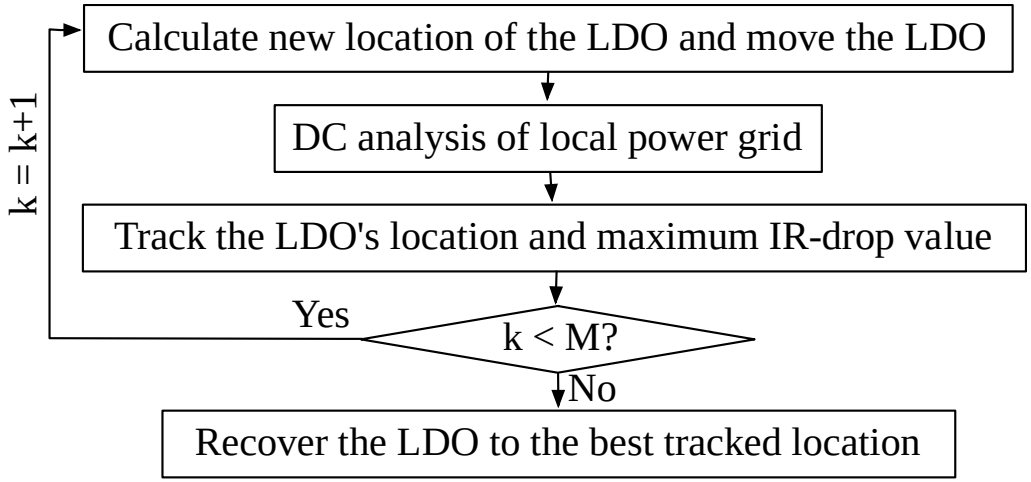
Candidate Locations of LDOs

- Divide the chip into a grid with LDO's width and height
- Candidate locations of the LDOs are the grid nodes that are located in white space area
- LDOs are connected to local and global power grids through metal wires



Optimize The Location of The Single LDO

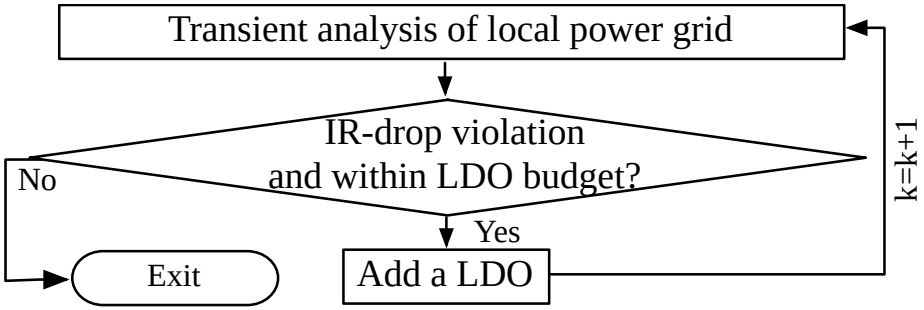
- Optimization flow of the single LDO



  - Perform DC analysis of local power grid
  - Assign each node a weight, which is proportional to its IR-drop
  - Move the LDO to the candidate location that is closest to weighted geometrical center of power grid
  - Repeat the process for a few times and set the LDO at the location with lowest max IR-drop values of the times tried

Add LDOs to Eliminate IR-drop Violation

- Flow of LDO insertion



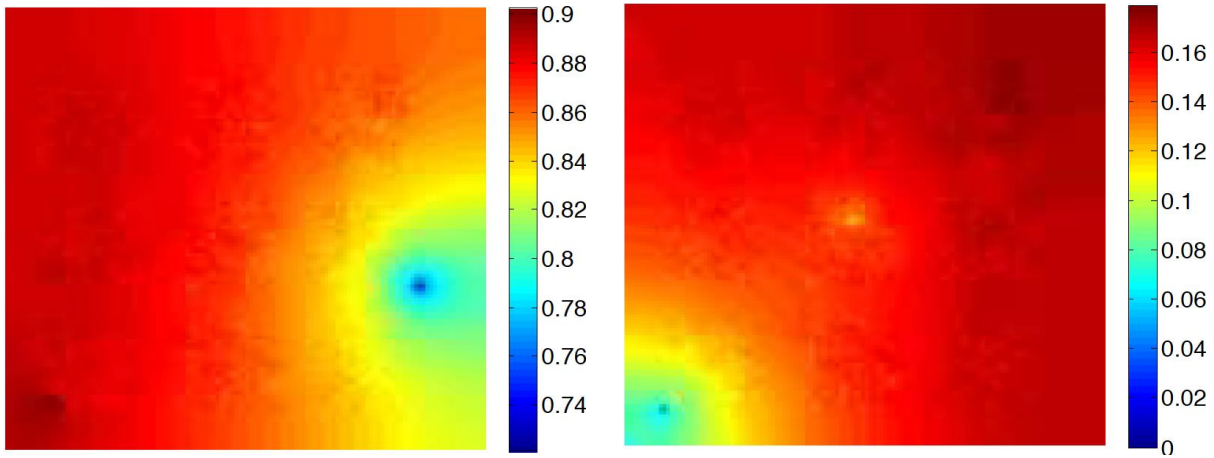
  - Utilize local power grid to insert the LDOs
  - Accumulate the IR-drop values of each node of local grid along the time steps
  - Insert LDOs at the closest candidate location to the node with maximum accumulated IR-drop value

Configurations of Experiments

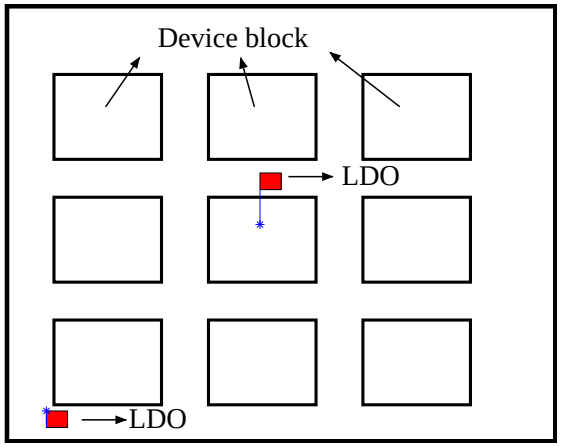
- The program is developed with C++ and SPICE
- It is executed on a CPU with 2.13 GHz frequency and 32 GB of RAM
- We generate a set of benchmarks to test the program
  - Each benchmark includes a power grid netlist and a device geometry file
  - There are 1000 time steps in each benchmark
- IR-drop constraint: $\Delta V_{max} \leq 0.1 * 1.8V = 0.18V$

Effect of The Proposed Method

- Test the proposed method on a power grid of 17K nodes



IR-drop values before and after optimizing the LDOs

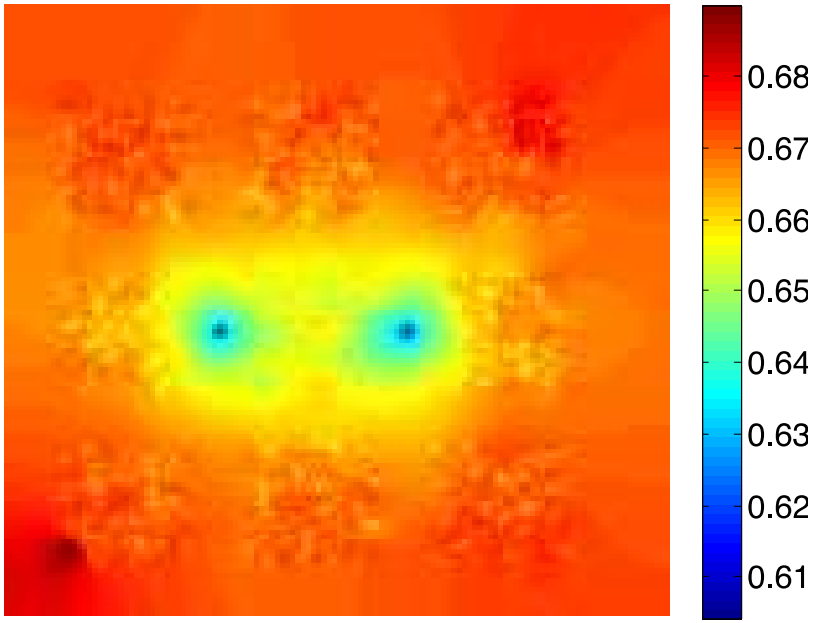


Locations of the LDOs

- With initial LDO, maximum DC and transient IR-drop values are 0.2V and 0.9V
- Moving the single LDO to center reduces the maximum DC IR-drop value to 0.16 V (max transient IR-drop value is still 0.42V)
- Adding another LDO reduces the max transient IR-drop value to 0.17 V

The Proposed Method and Others (1)

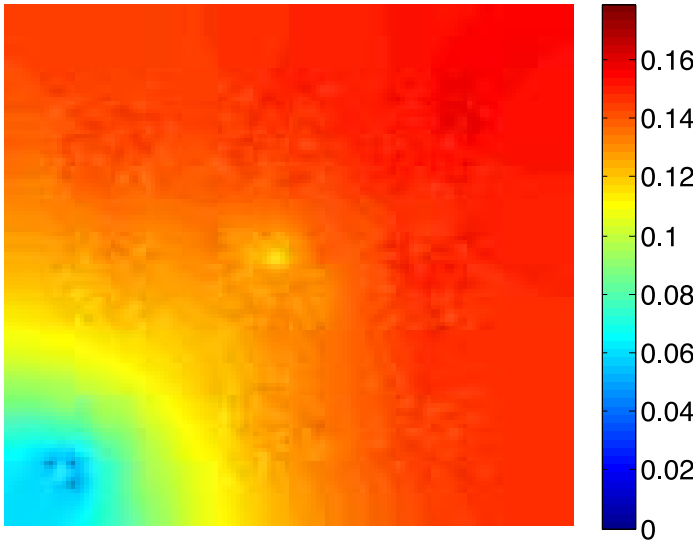
- Compare the proposed method with two other methods in optimizing the LDOs
  - Evenly distribute the two LDOs on the chip
    - Maximum transient IR-drop is at 0.62V, which violates the IR-drop constraint



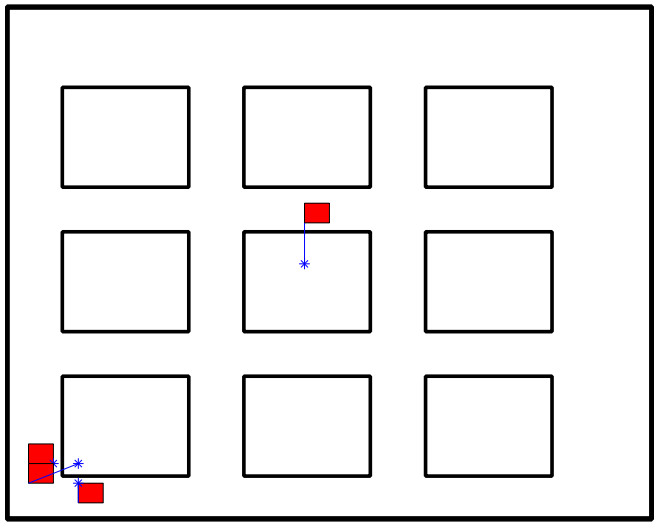
IR-drop values with even distribution of the two LDOs

The Proposed Method and Others (2)

- Insert LDO at any time step when there is a IR-drop constraint violation
  - Requires four LDOs to meet the IR-drop constraint, which is more than two LDOs of the proposed method
  - This method cannot see the improvement of DC operation point after adding each LDO at some time step



IR-drop values with the four LDOs



Locations of the four LDOs

Test The Proposed Method on More Cases

- Simulation results

$Case$	N_{LDO}	N_B	ΔV_{imax}	ΔV_{omax}	$T(h:m:s)$	K
C17K	2	301	0.913	0.179	00:49:20	98
C525K	3	580	0.935	0.155	08:54:50	53
C1M	13	139	1.534	0.167	34:38:24	92
C2M	21	621	1.192	0.173	62:30:12	103

1.N_{LDO} : number of LDOs after optimization; 2.N_B : number of LDO candidates; 3.ΔV_{imax} and ΔV_{omax} : maximum IR-drop value before and after optimization; 4.$T(h:m:s)$:runtime (hour:minute:second); 5.K : total number of transient analysis of global and local power grid

- By integrating a set of LDOs into power grid, the maximum IR-drop values are effectively reduced to meet the IR-drop constraint

Conclusions

- We propose an efficient method to integrate a set of on-chip low-dropout voltage regulators (LDOs) into power grid, so that the maximum IR-drop value is less than 10% of power supply
- Hybrid simulation of power grid and LDOs is performed to obtain the voltage values of LDOs and nodes in power grid
- With an efficient optimization flow, a set of LDOs are set at the most effective locations to reduce the IR-drop values
- Experimental results verify the effectiveness of the proposed method