

Scattered Refresh: An Alternative Refresh Mechanism to Reduce Refresh Cycle Time

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Outline

- Refresh Basics
- Refresh Overhead
- Literature Survey
- Logical Organization of a DRAM bank
- DRAM Bank - closer look
- Scattered Refresh - Concept
- Experimental Setup
- Results
- Conclusions

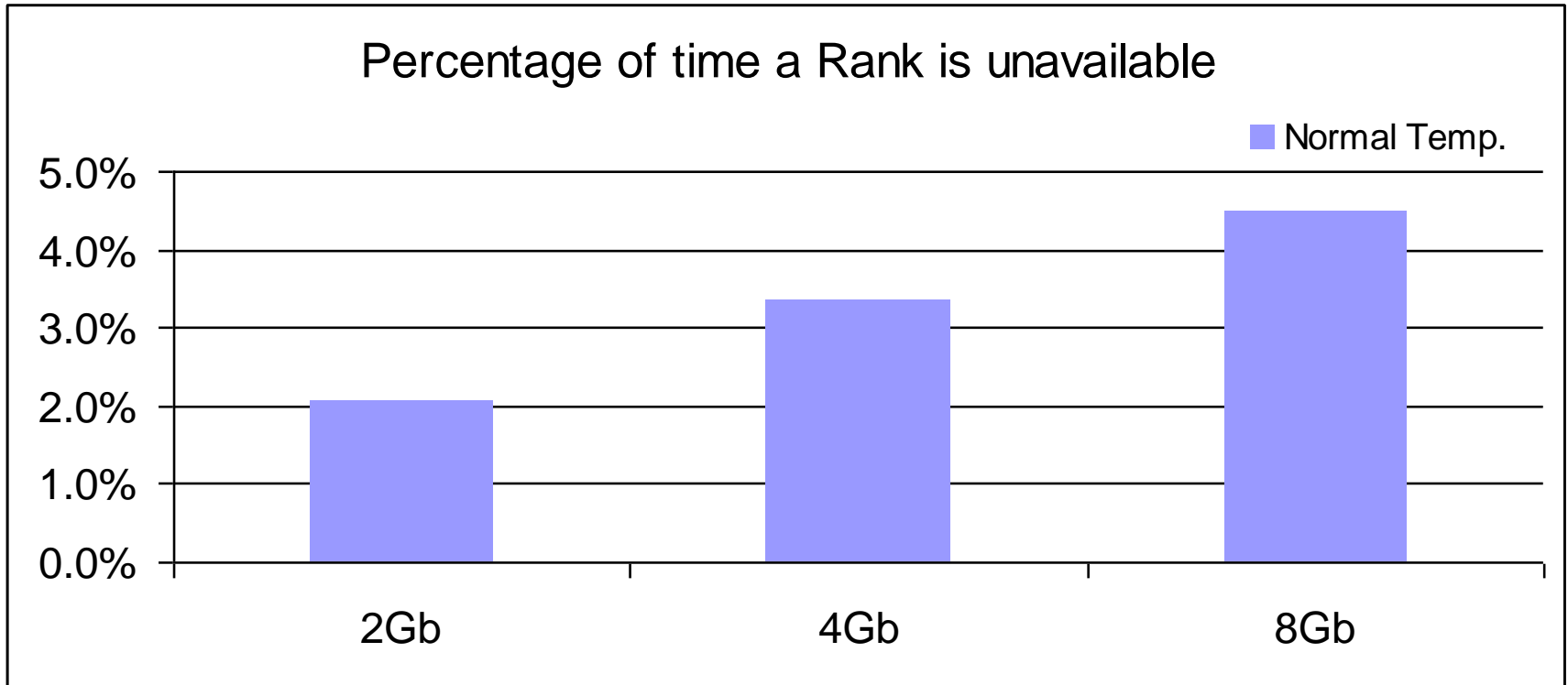
Refresh Basics

- DRAM cells lose charge due to leakage.
 - Periodic charge/data refill is needed.
- Refresh Types –
 - RAS-only refresh
 - CAS-before-RAS refresh
- Distributed Refresh
 - Divide rows into small groups, send refresh command to each.
 - 8K refresh commands spaced t_{REFI} time apart.
 - Refresh Cycle Time (t_{RFC}) per refresh command.

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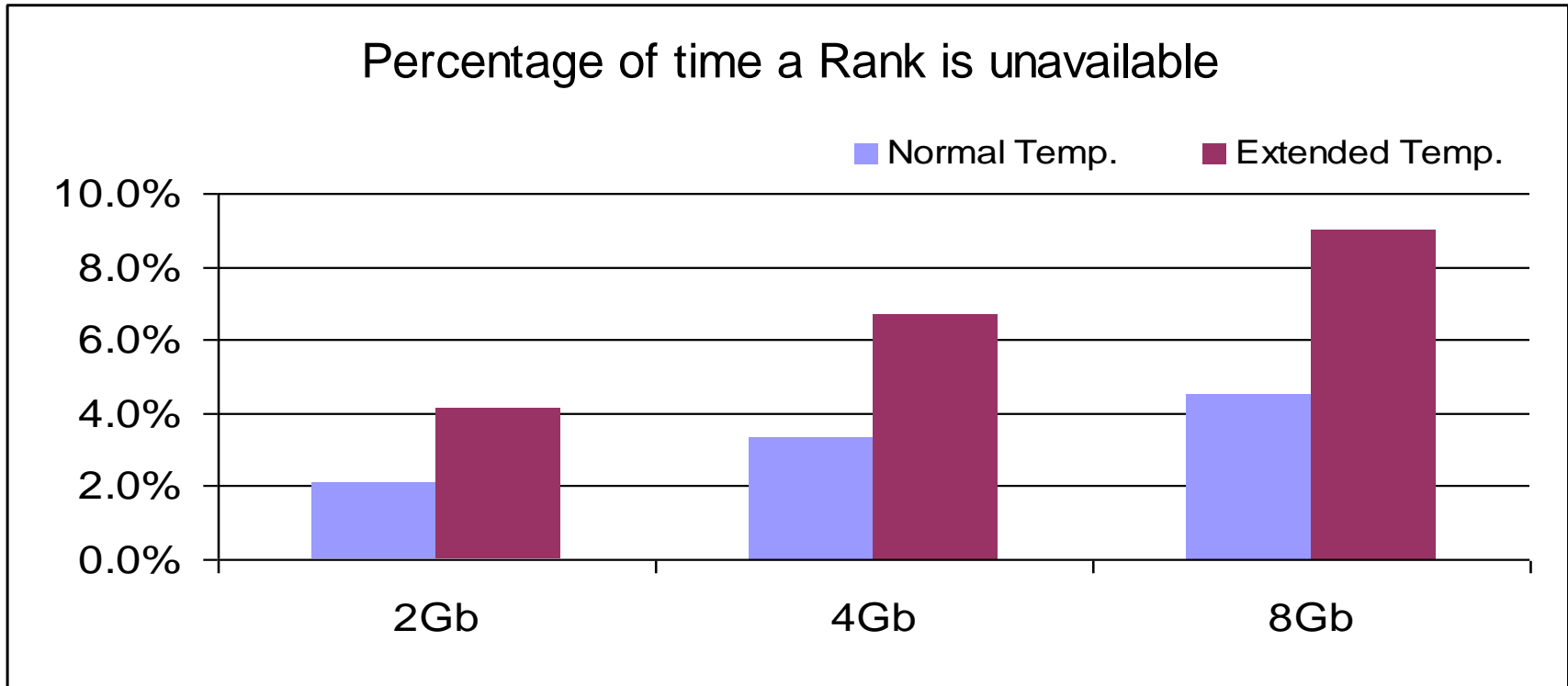
Refresh Overhead



Retention time is 64ms, $t_{REFI} = 7.8\mu s$

Refresh Overhead

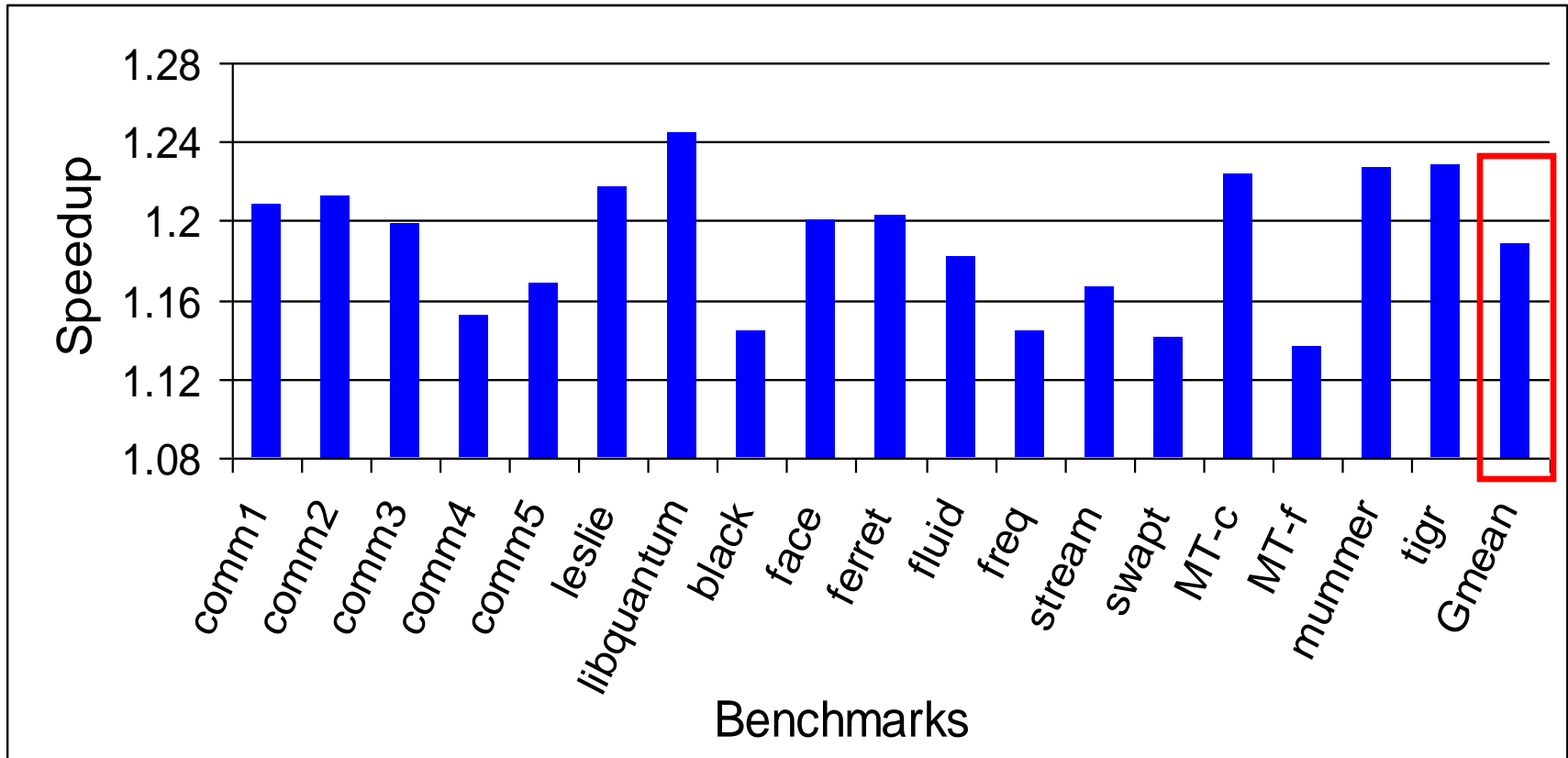
Cont ...



Retention time is 64ms (temp < 85°C), tREFI_normal = 7.8us

Retention time is 32ms (temp > 85°C), tREFI_extended = 3.9us

Scope of Improvement



8Gb device @ 800MHz in Ext. Temp. mode

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Literature Survey

- Refresh Pausing [Prashant et. al, HPCA, 2013]
- Concurrent Refresh [Kiriata et. al, JSSC, 2005]
- Adaptive Refresh [Mukundan et. al, ISCA, 2013]
- Coordinated Refresh [Ishwar et. al, ISLPED 2013]
- Smart Refresh [Mrinmoy et. al, MICRO, 2007]
- Elastic Refresh [Stuecheli et. al, MICRO, 2010]
- Retention-aware placement in DRAM (RAPID) [Venkatesan et. al, HPCA, 2006]
- Flicker [Song et. al, Comp. Arch. News, 2011]
- Retention-aware intelligent DRAM refresh (RAIDr) [Jamie et. al, ISCA, 2012]

Outline

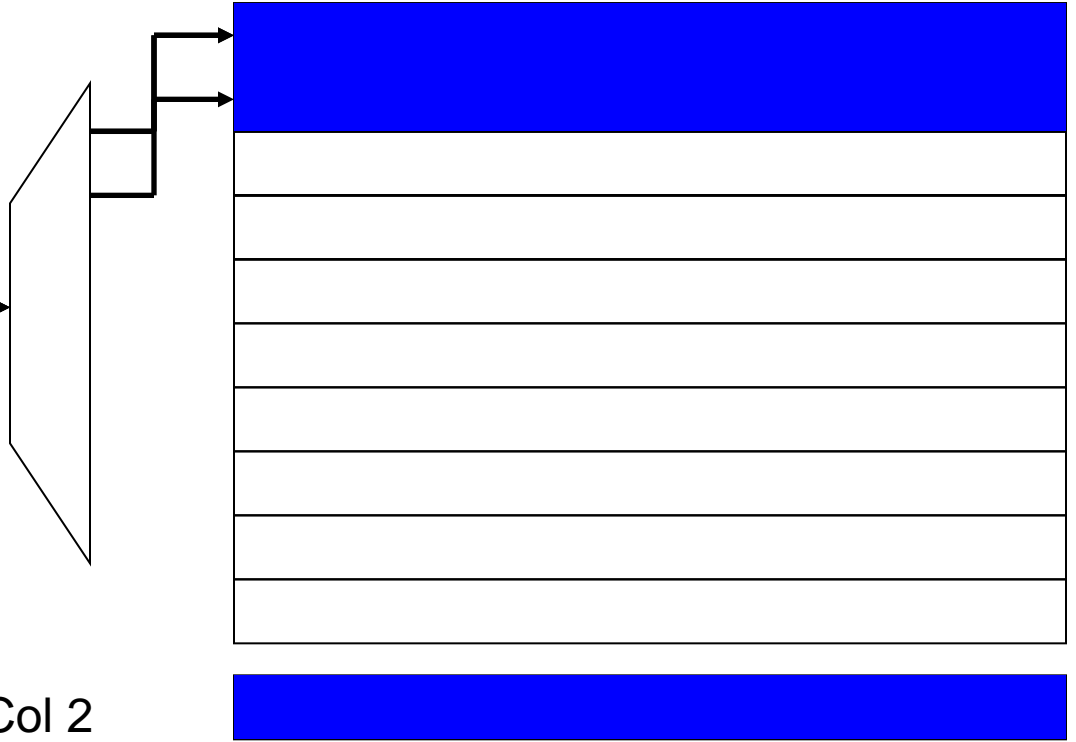
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Logical Organization of a DRAM Bank

Refresh Controller

ACTIVATE
CAS
PRECHARGE

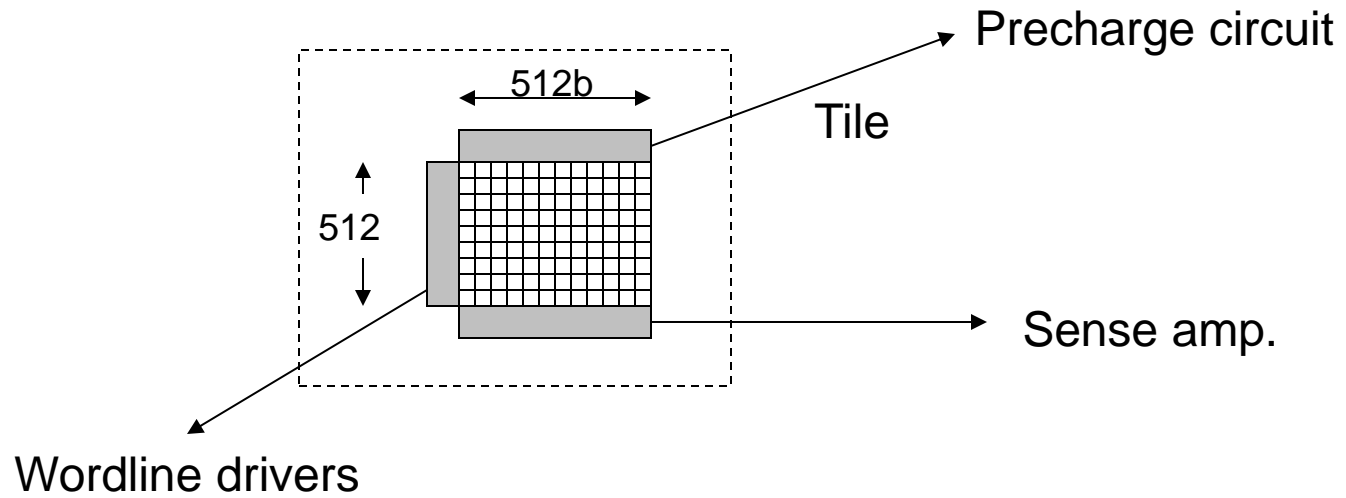
Row 0



Col 2

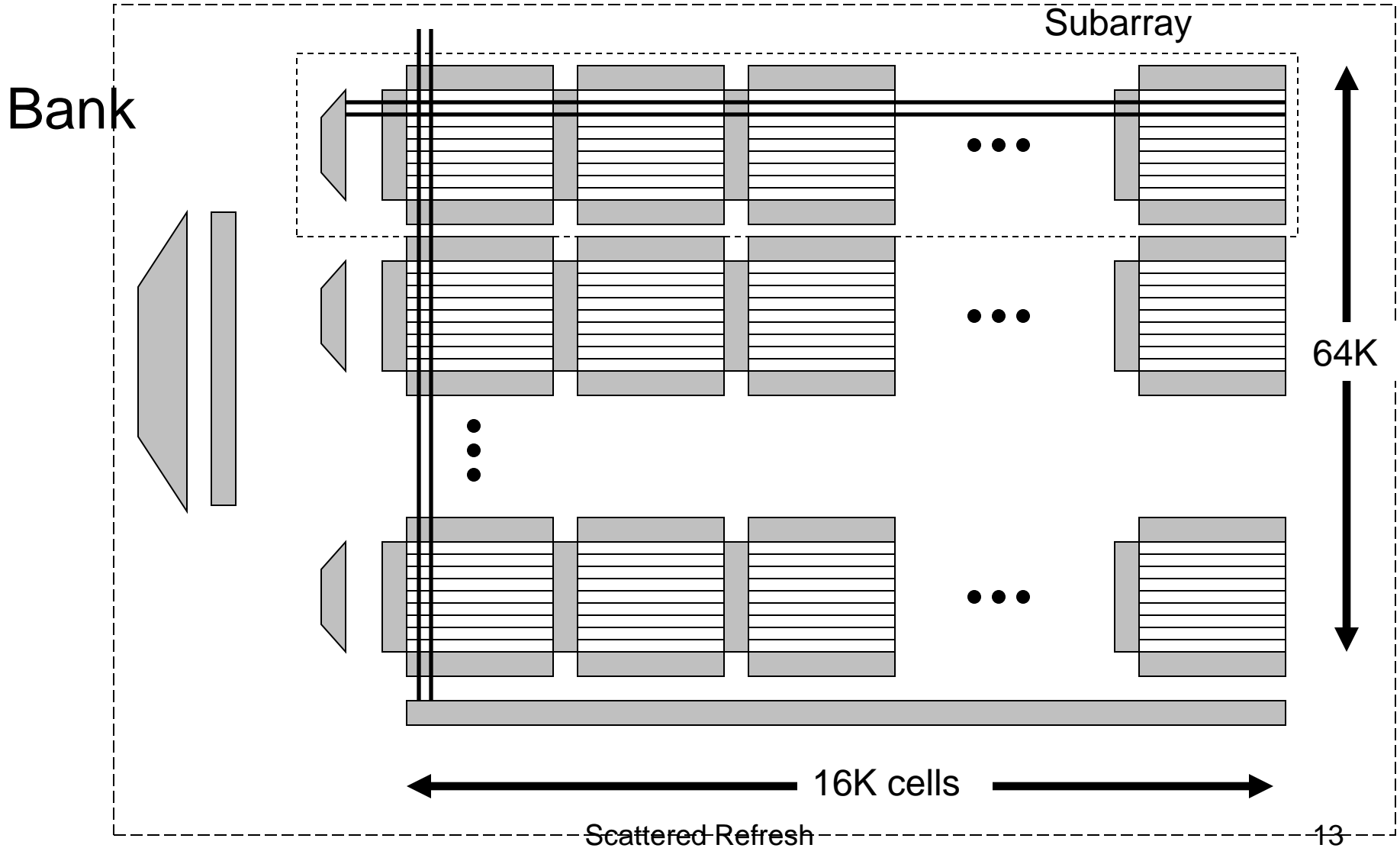


DRAM Bank – Closer look



DRAM Bank – Closer look

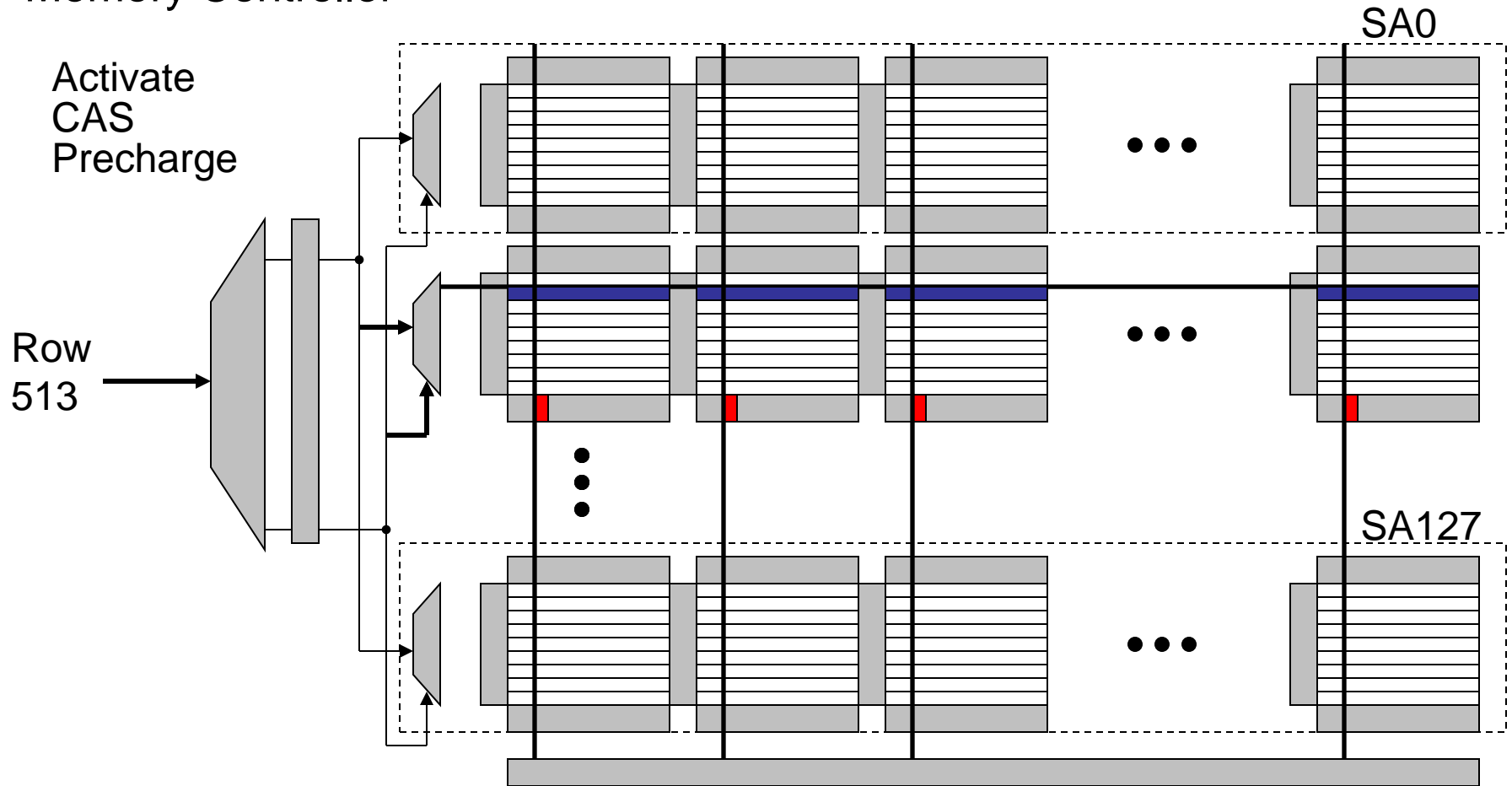
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DRAM Bank – Closer look

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Memory Controller



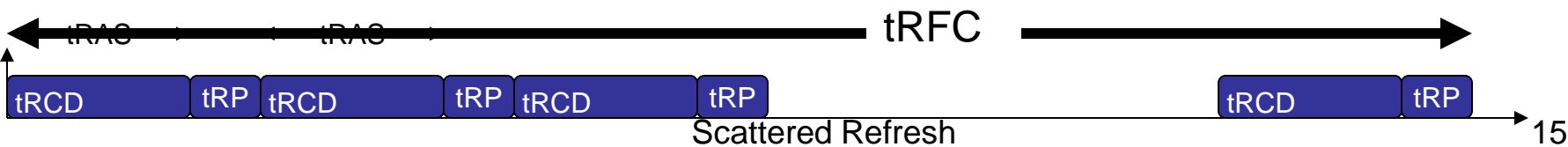
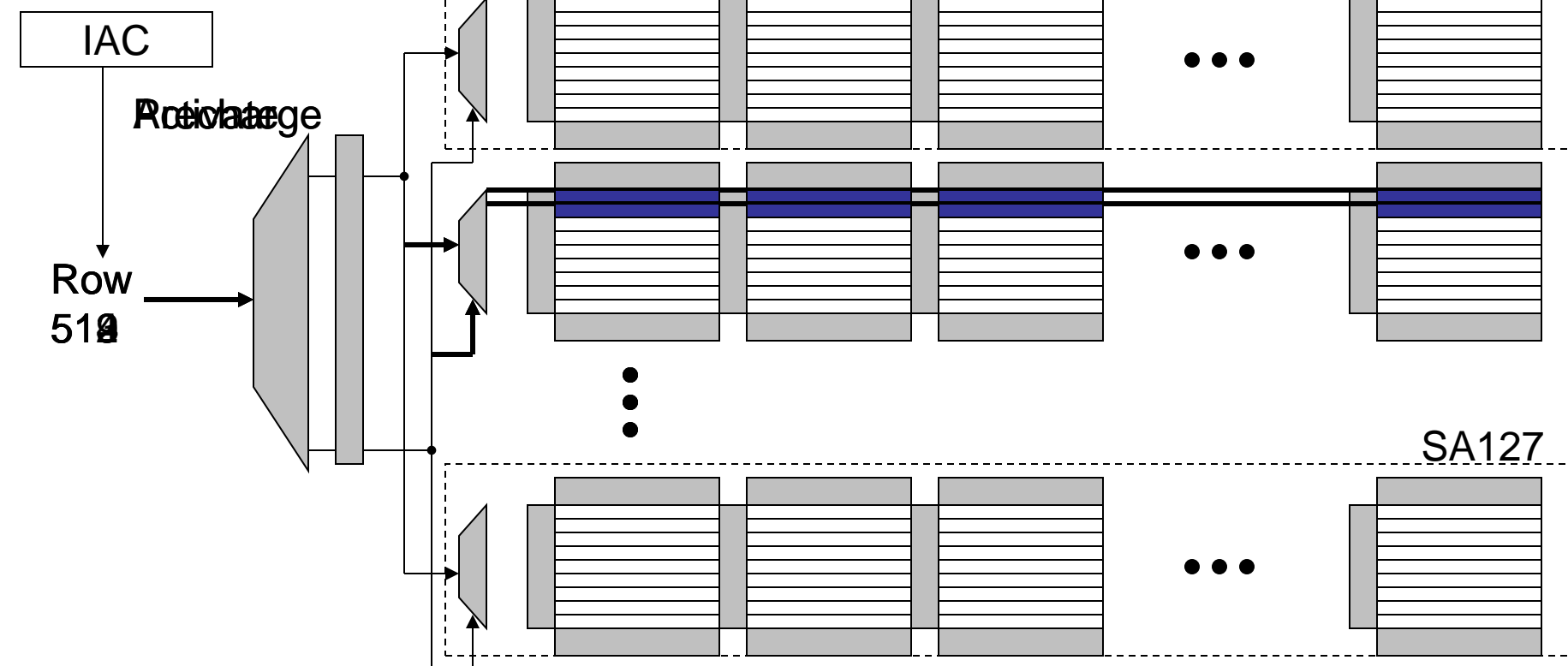
Scattered Refresh

DRAM Bank – Closer look at Refresh

Memory Controller

REF 64th => Rows 512 – 519 are to be refreshed

Refresh Controller



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Scattered Refresh - Concept

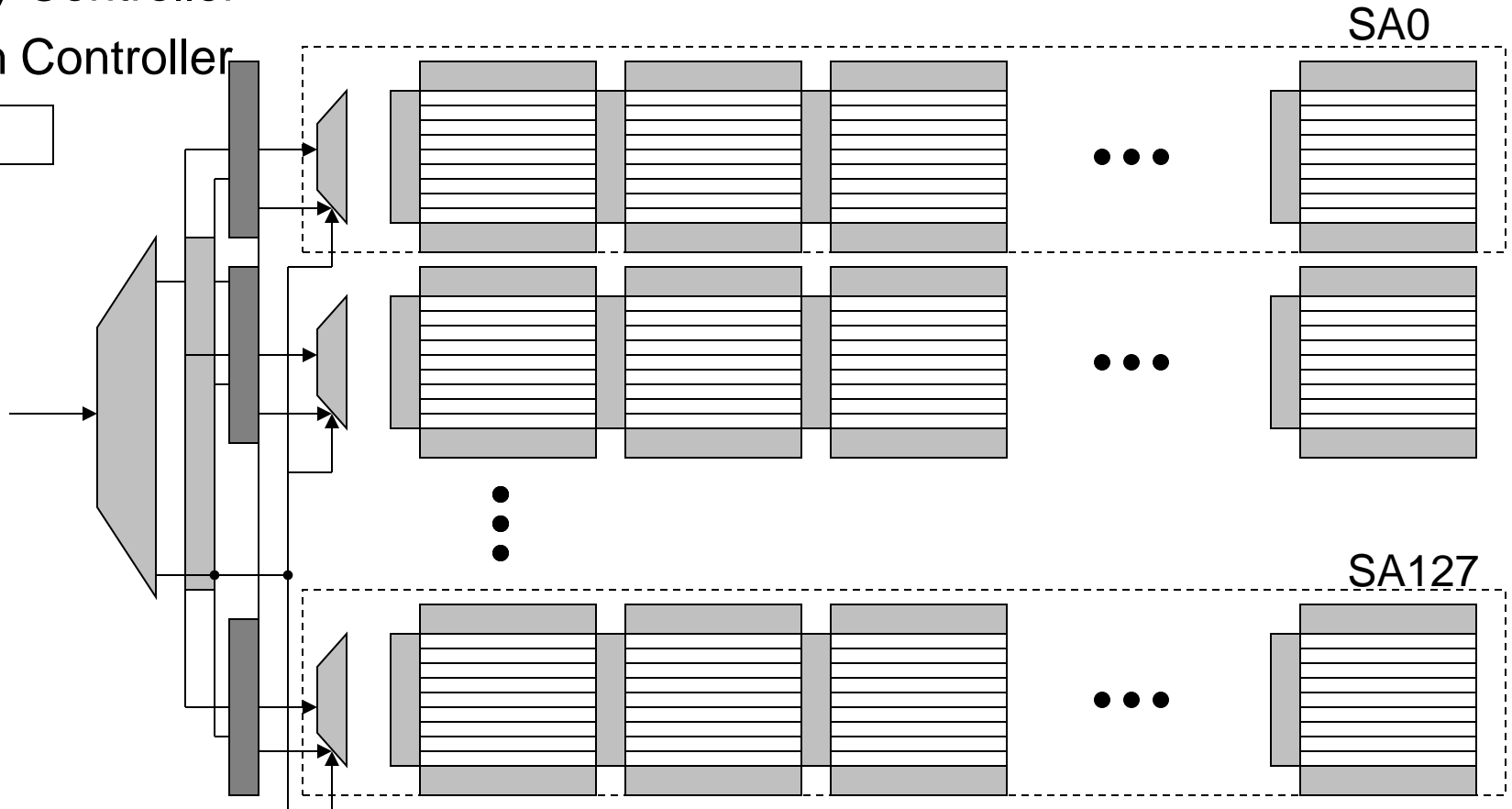
- Exploit possible overlap in subarray accesses.
- Involve more than one subarray during Refresh.
 - Activate rows from different subarrays.
 - Remove Precharge from critical path of next Activate.
- Stride to IAC can be anything greater than tile size.
 - We choose 8K keeping in-view implementation ease.

Scattered Refresh

Memory Controller

Refresh Controller

IAC



DDR DRAM model by Thomas Vogelsang, RAMBUS, MICRO 2010.

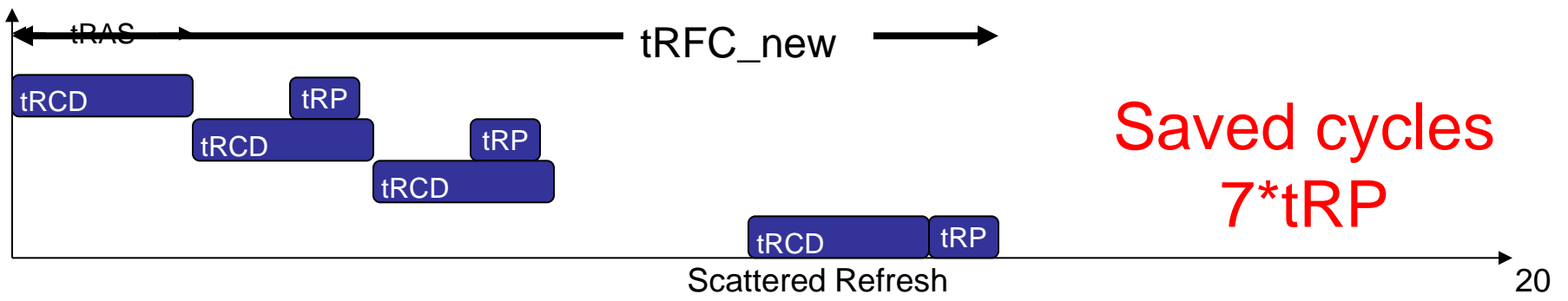
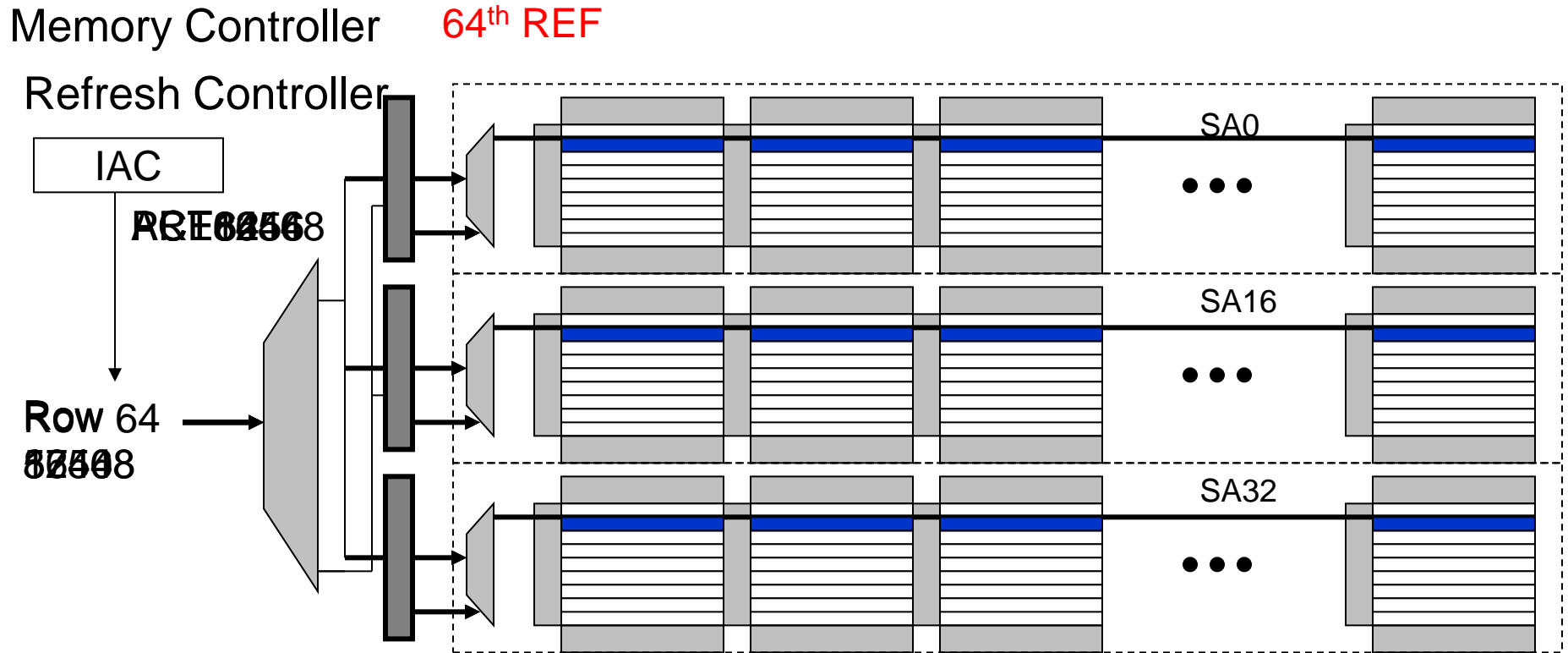
Scattered Refresh

Scattered Refresh - working

During the 64th Refresh the rows to be refreshed are

Row no.	Subarray (SA)
64	SA 0
8256	(64 SA 192)
16448	(8256 SA 384)
24640	(16448 SA 576)
32882	(24640 SA 768)
41024	(32882 SA 960)
49216	(41024 SA 1152)
57408	(49216 SA 1344)

Scattered Refresh - working



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Experimental Setup

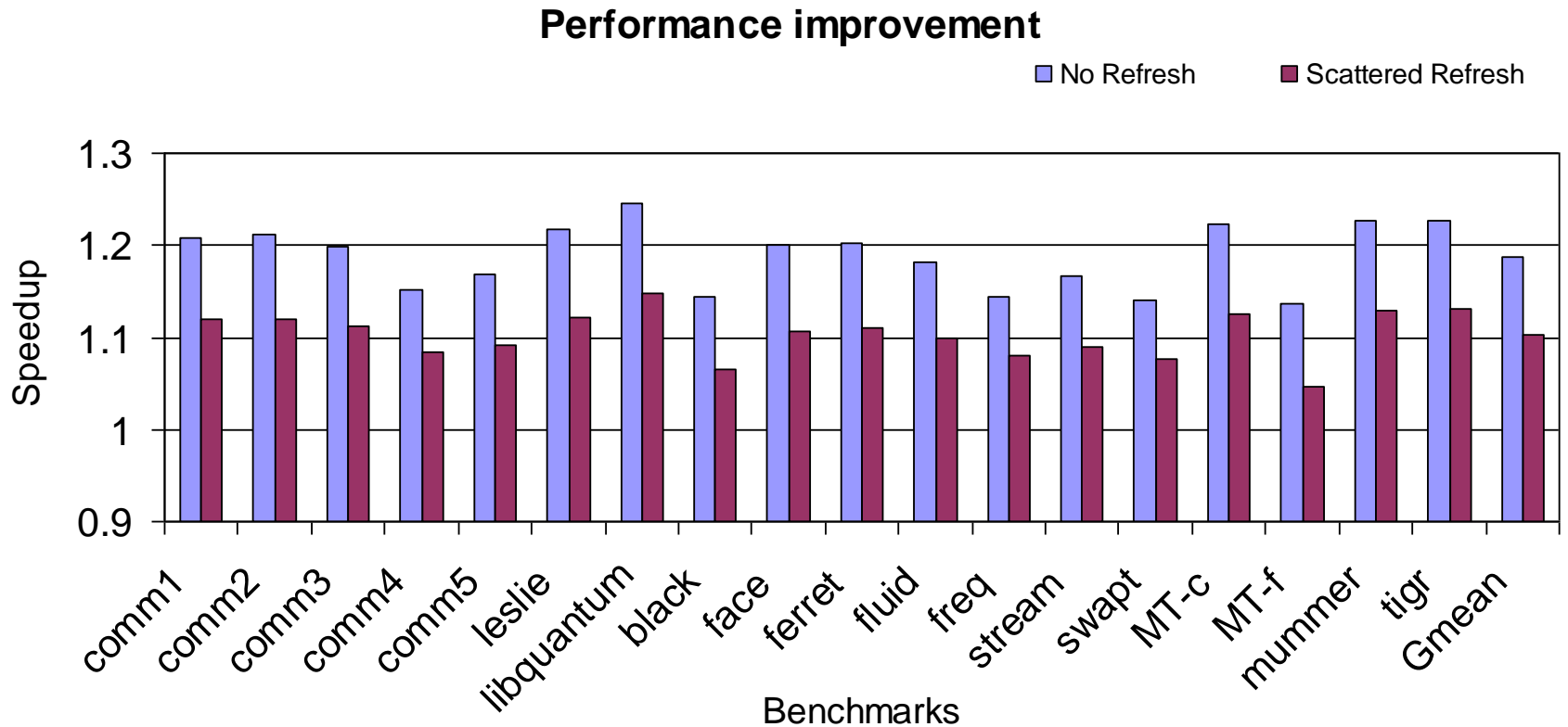
- Processor Configuration –
 - 4 width, 10 stage pipeline
 - Quad core, 3.2GHz
 - 3 levels of cache, 512KB LLC per core

Experimental Setup

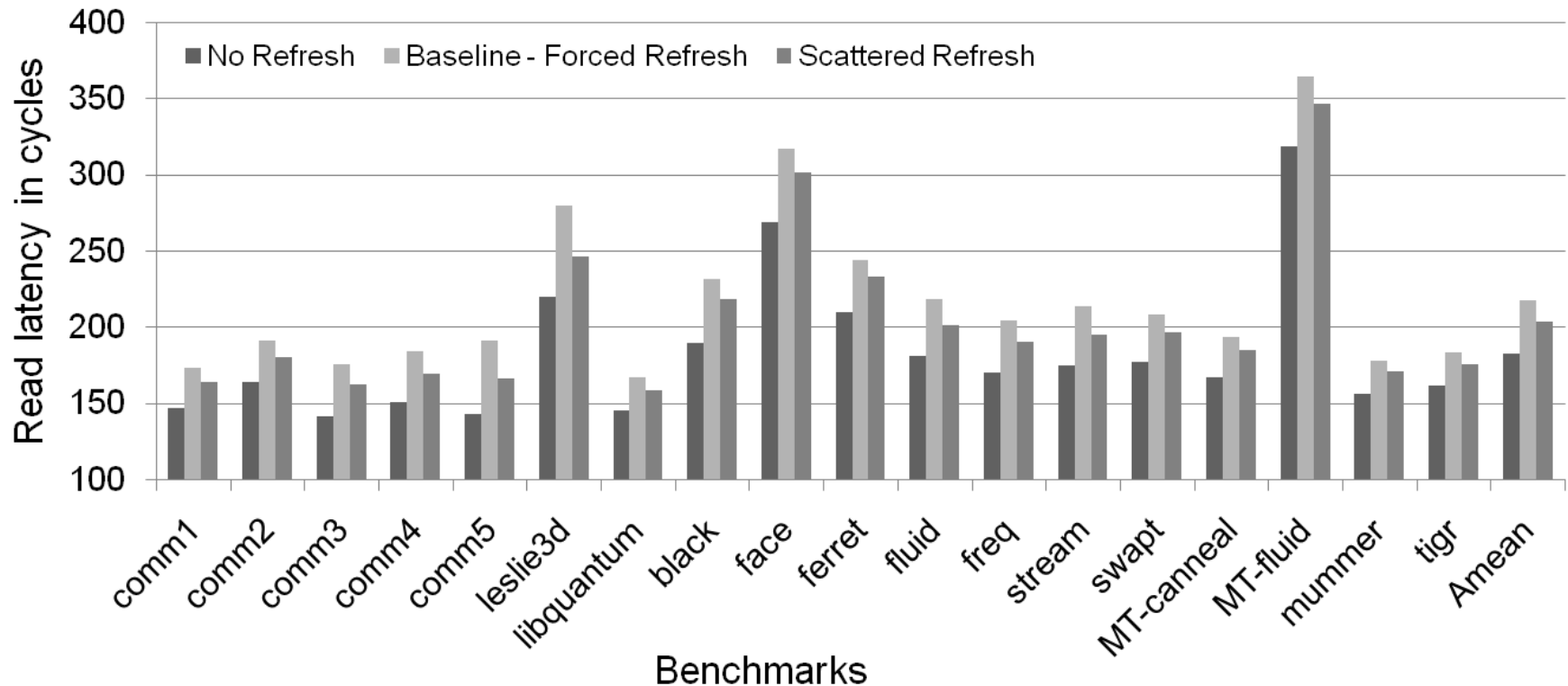
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- Memory Configuration –
 - Request scheduling: FR-FCFS
 - Page management: Close-page policy
 - Refresh scheduling: Forced-refresh
 - 4 channel, 2 ranks/channel, 8 banks/ rank
- DRAM device Configuration –
 - 8Gb 11-11-11 DDR4 DRAM @ 800MHz
 - 64K row per bank
 - 8Kb page size

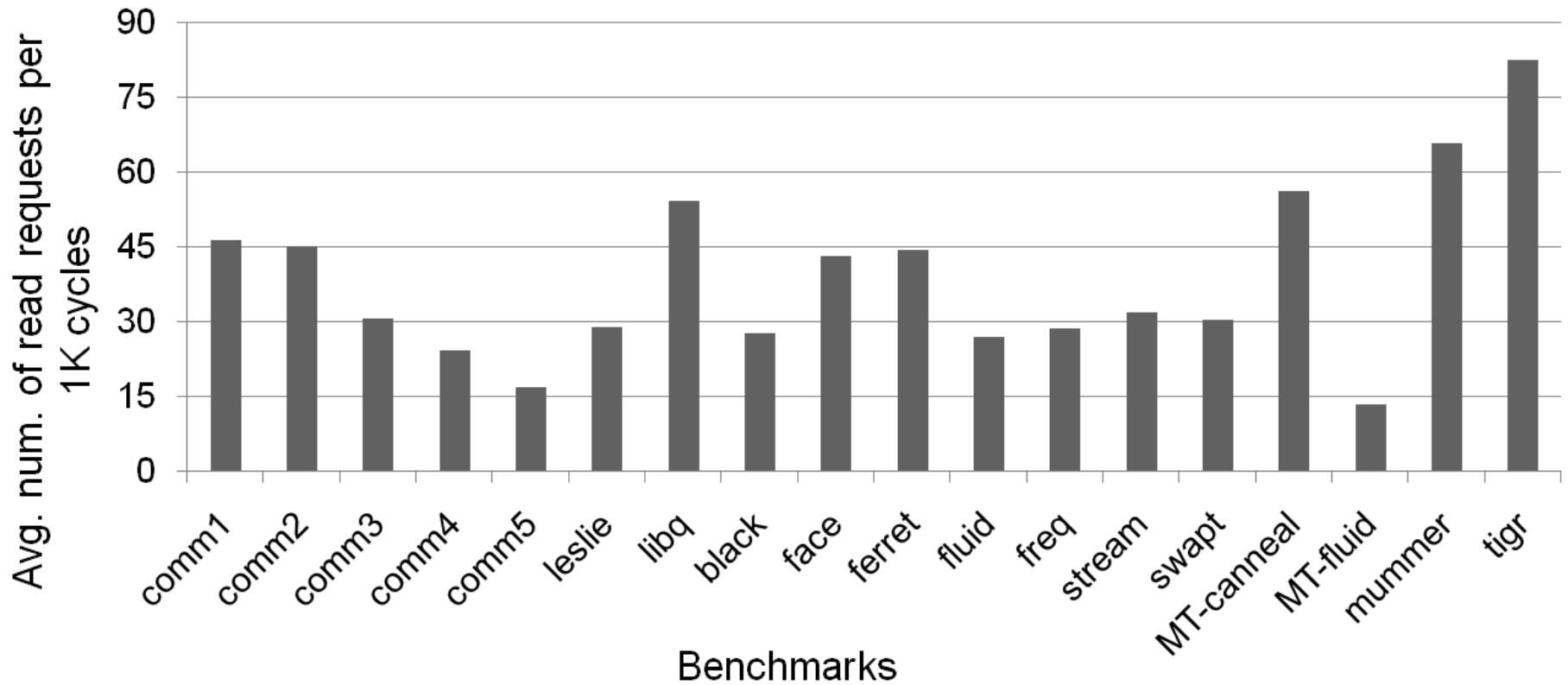
Results – Performance Improvement



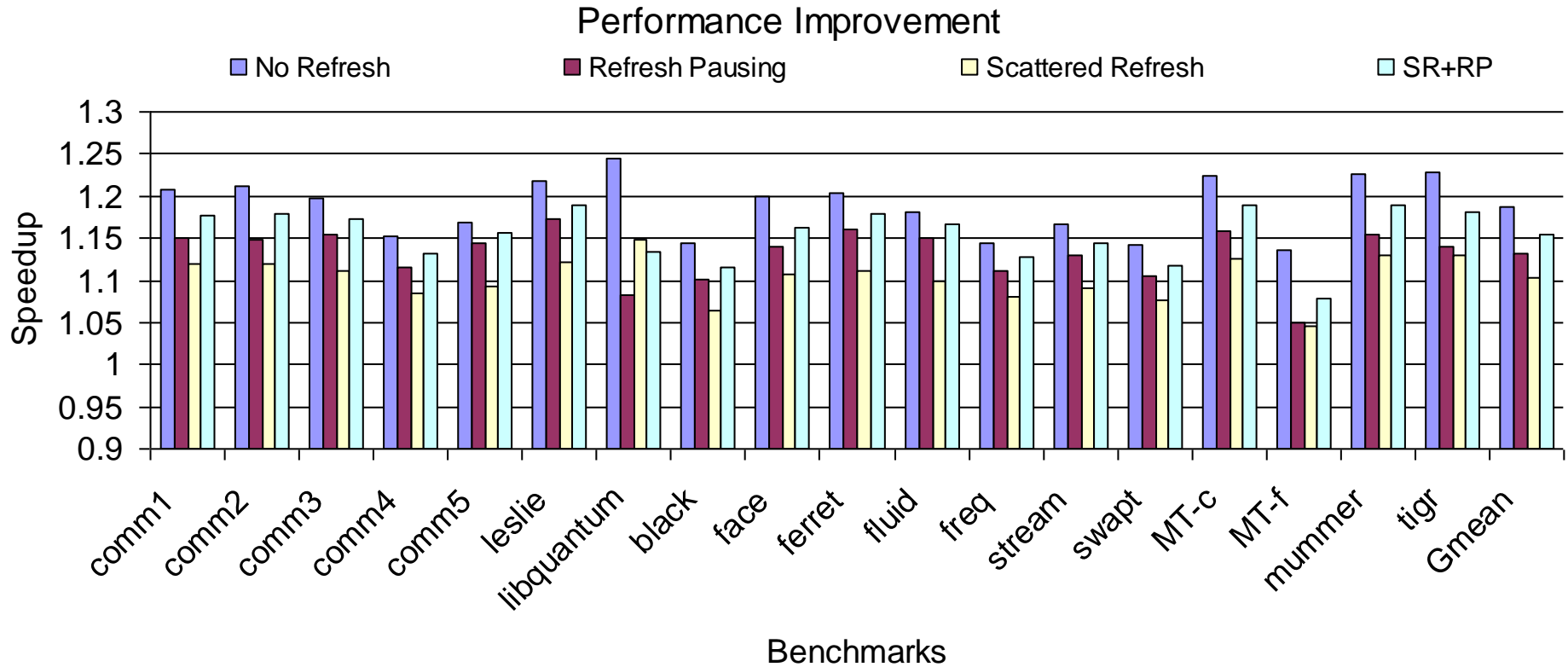
Results - Read latencies



Results – Frequency of Requests



Results – comparison with Refresh Pausing



No Refresh – 18.9%

Scattered Refresh – 10.2%

Refresh Pausing – 13.1%

Scattered Refresh + Refresh Pausing – 15.4%

Conclusions

- Refresh has significant impact on performance.
- Scattered Refresh decreases $tRFC$ by overlapping the ACT and PRE of different rows.
 - Increases the availability of Rank for memory requests.
 - Recovers almost 59% of performance.
- Scattered Refresh is complementary to other refresh handling techniques.

Thank you for your attention!



Questions ?