

# An Overview of Spin-based Integrated Circuits

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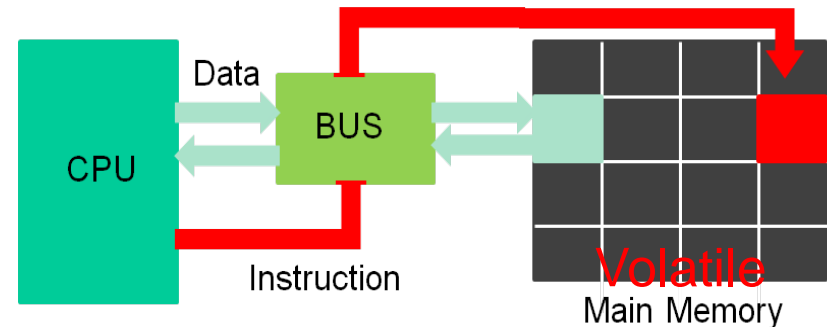
1/12/2014

# Outline

- **Introduction**
- Spintronics fundamental
- Spin-based memory devices and circuits
- Spin-based logic devices and circuits
- Emerging computing paradigms
- Conclusion and perspectives

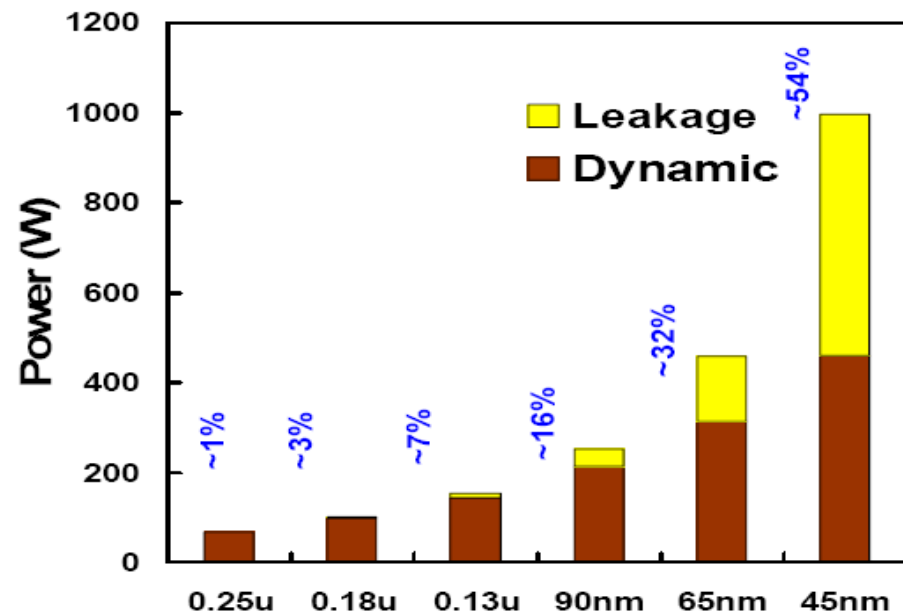
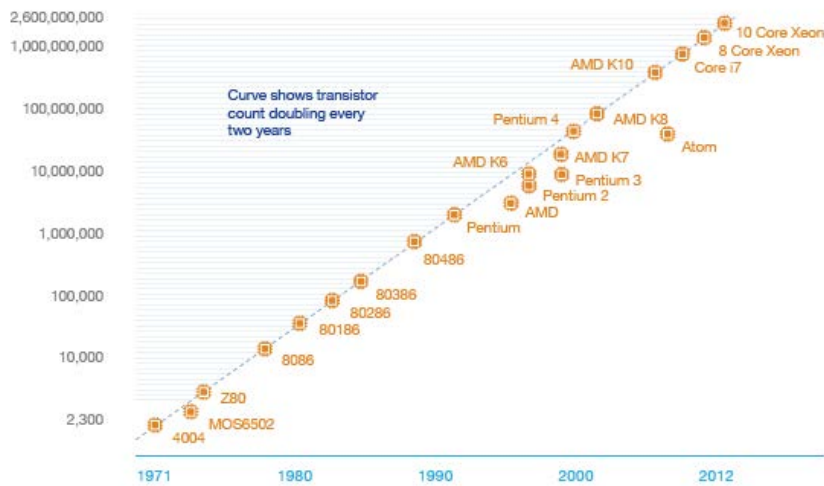
# Moore's Law Ends?

- MOS Scaling Ends???
- Leakage current (static)
- Long traffic (dynamic)
- Reliability issues



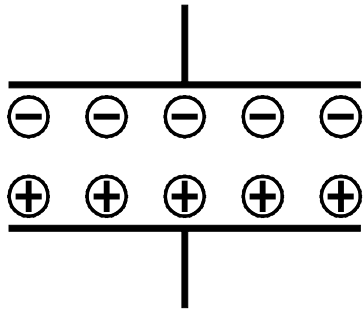
Weisheng Zhao et al, IEEE VLSI-SOC, 2013

Microprocessor Transistor Counts 1971 -2011 & Moore's Law

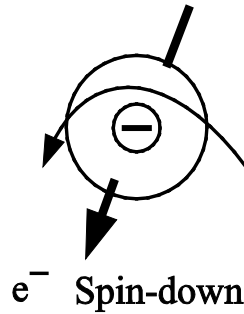
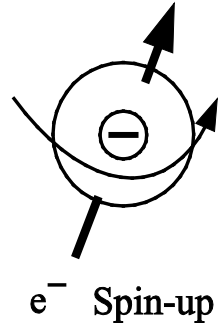


S. E. Thompson, S. Parthasarathy, *Mater. Today*, Vol. 9 No. 6, pp. 20-25, 2006.

# Spintronics is Emerging!

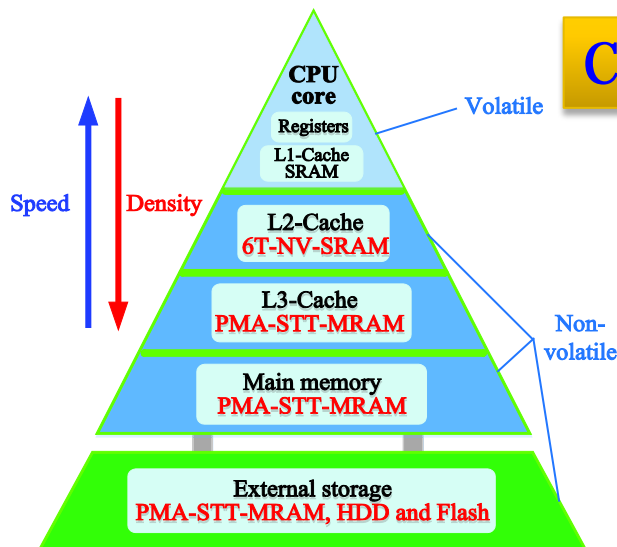


Conventional electronics:  
uses electrical charge

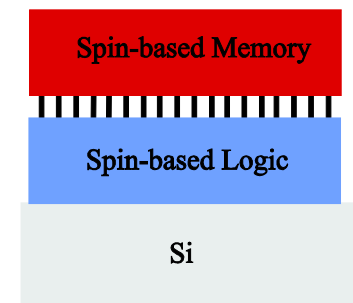
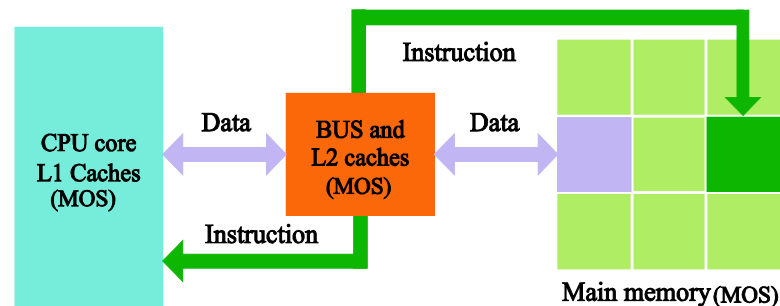


Spintronics: uses spin of electrons  
in addition to electrical charge

- Non-volatility
- 3D integration
- fast access speed
- ultra-low power



Completely or partially replace CMOS technology



Weisheng Zhao et al, IEEE VLSI-SOC, 2013

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# Spintronics History

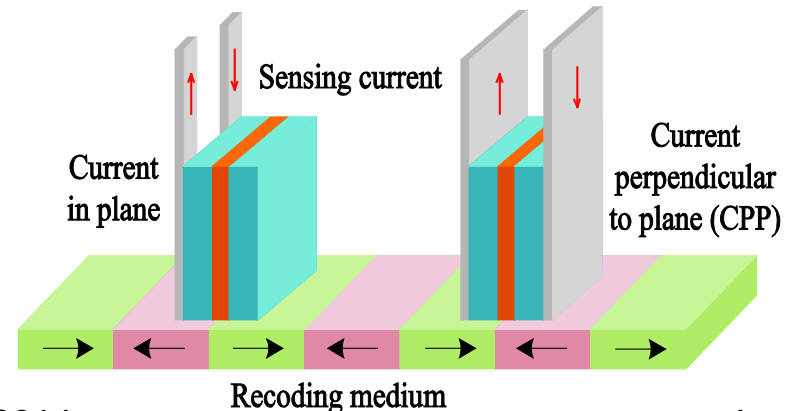
- The origins of Spintronics can be traced back to the 1970s [Juliere 1975]
- The discovery of spin valve or GMR in 1988 (Nobel Prize Physics 2007 for A. Fert and P. A. Grunberg)
- The discovery of MTJ and STT in 1995 [Moodera et al., Miyazaki et al., and Berger and Slonczewski]
- The spin-valve sensor was firstly commercialized by IBM in 1997



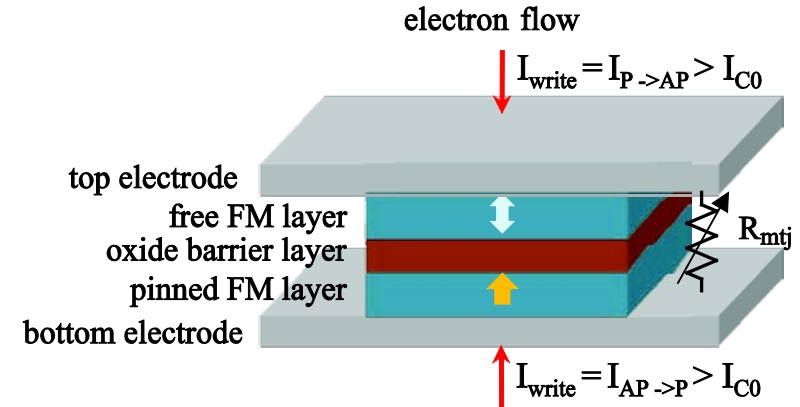
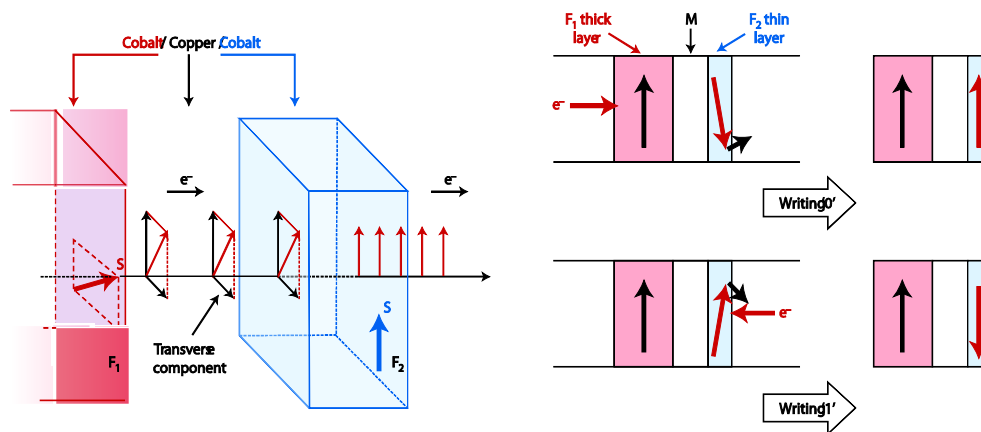
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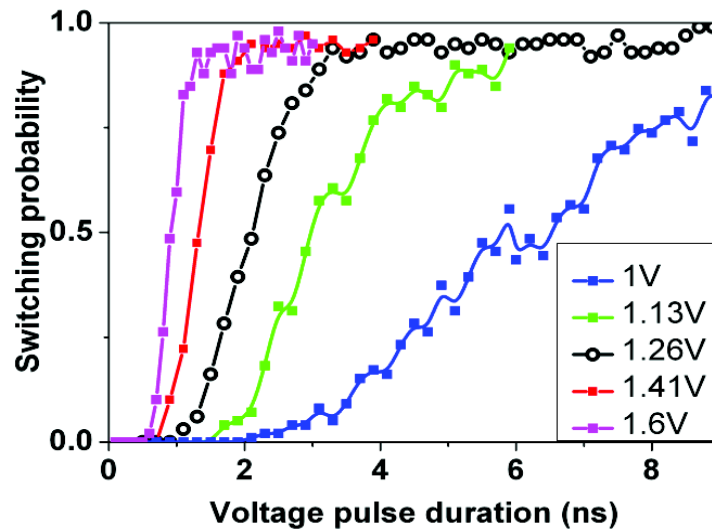
ASP-DAC 2014



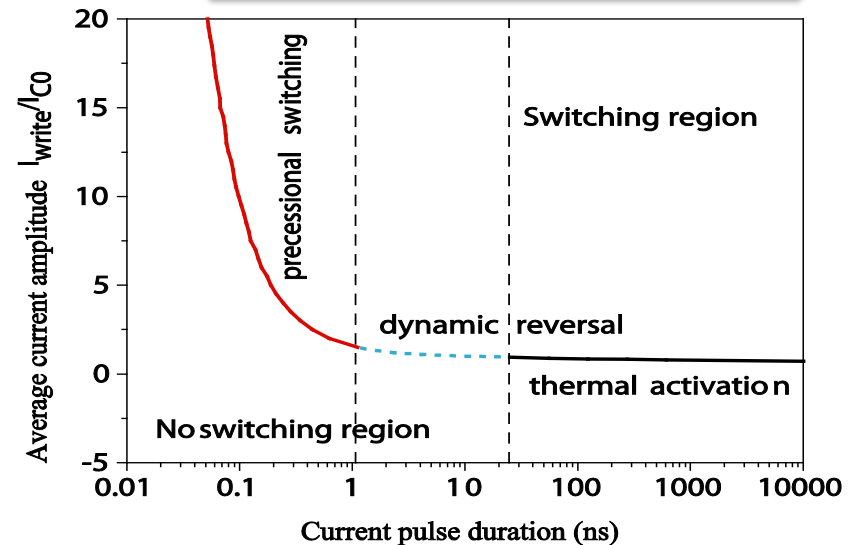
# STT-MTJ



## Stochastic switching



$$\text{TMR} = (R_{AP} - R_P) / R_P$$



# STT-MTJ modeling

- Critical current

$$I_{C0} = \alpha \frac{\gamma e}{\mu_B g} (\mu_0 M_s) H_K V = 2\alpha \frac{\gamma e}{\mu_B g} E$$

- Precessional switching region,

$$\Pr(t_{pulse}) = 1 - \exp\left(-\frac{t_{pulse}}{\tau_1}\right), \frac{1}{\tau_1} = \left[ \frac{2}{C + \ln(\pi^2 \Delta)} \right] \frac{\mu_B P}{em(1 + P^2)} (I_{write} - I_{C0})$$

- Thermal activation region,

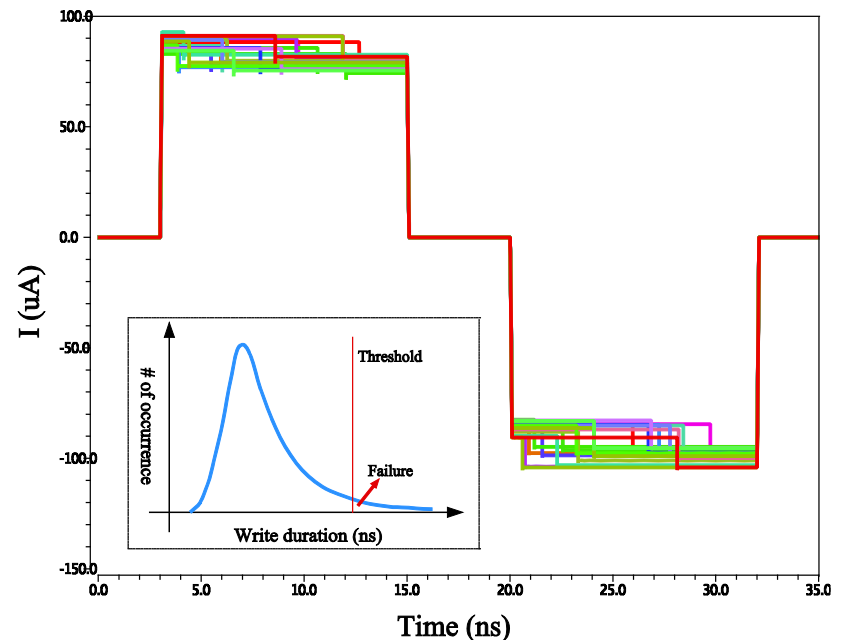
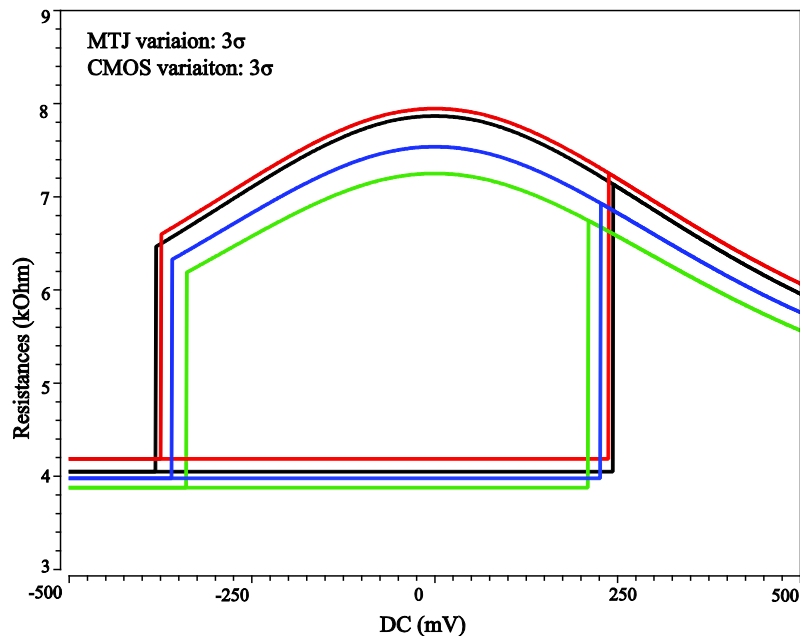
$$\frac{d \Pr(t_{pulse})}{(1 - \Pr(t_{pulse})) dt} = \frac{1}{\tau_2}, \tau_2 = \tau_0 \exp\left(\frac{E}{k_B T} \left(1 - \frac{I_{write}}{I_{C0}}\right)\right)$$

- Dynamic reversal region, no explicit formulas



# STT-MTJ modeling (Cont.)

- Verilog-A language
- STMicroelectronics 40 nm design-kit
- DC and transient simulation



Y. Zhang et al., *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp.819-826, 2011.

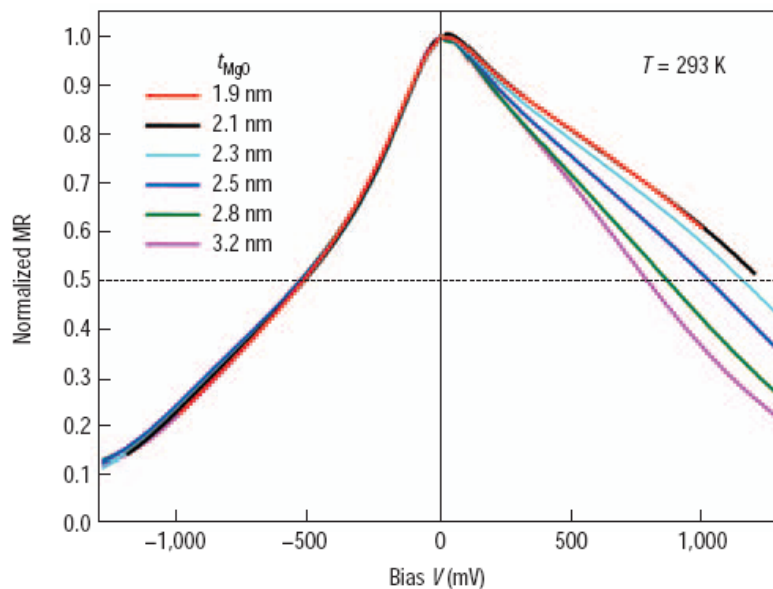
# Reliability issues

- STT **stochastic** switching—write errors

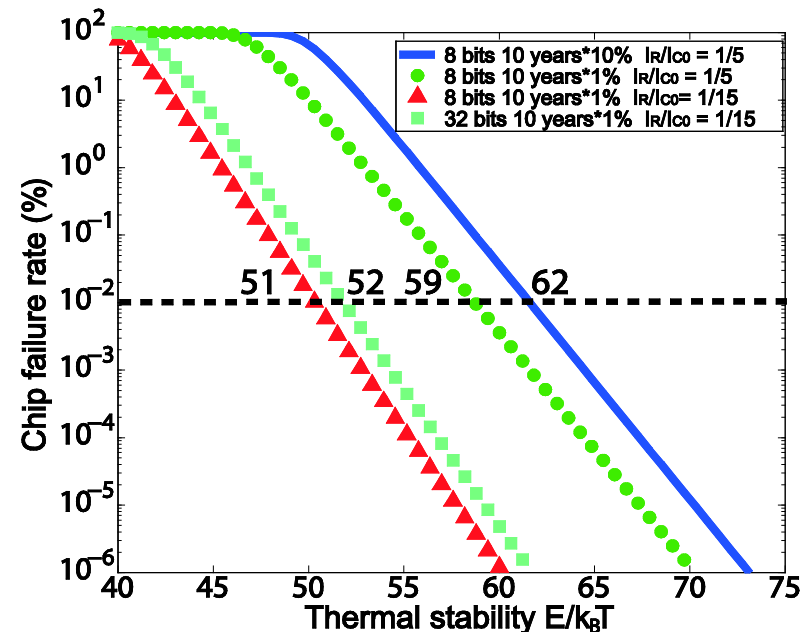
- TMR reduction—read errors

- Read disturbance—read errors  $Pr_{dis}(t_{read}) = 1 - \exp(-N \frac{t_{read}}{\tau_0} \exp(-\Delta(1 - \frac{I_{read}}{I_{C0}})))$

$$TMR_{real} = \frac{TMR(0)}{1 + V_{bias}^2 / V_h^2}$$



S. Yuasa et al, *Nat. Mat.* (2004)



W. S. Zhao, et al, *Microelectron. Reliab.*, vol. 52, pp. 1848-1852, 2012.

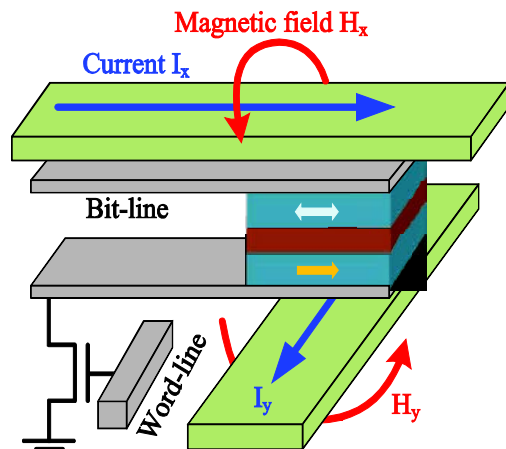
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# Magneto RAM (MRAM)

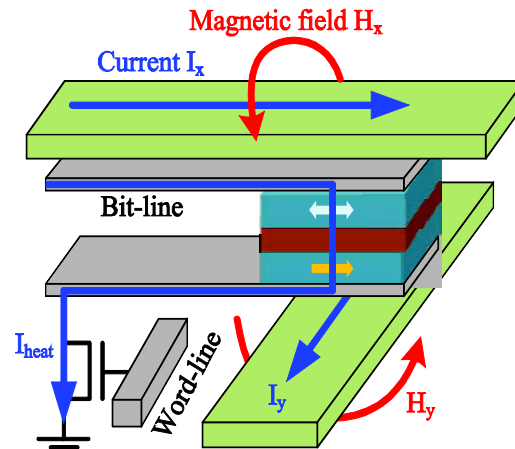
- Mainly based on the hybrid structure, i.e. MTJ+MOS

Field driven  
FIMS-MRAM



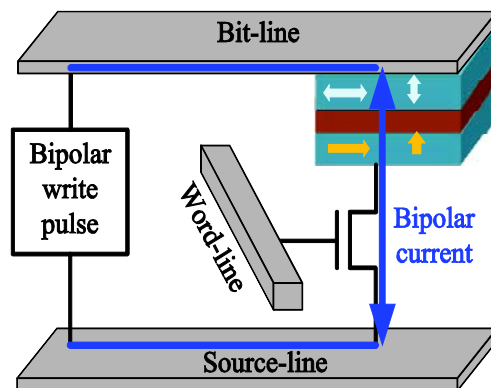
(a)

Thermal Assisted  
TA-FIMS-MRAM



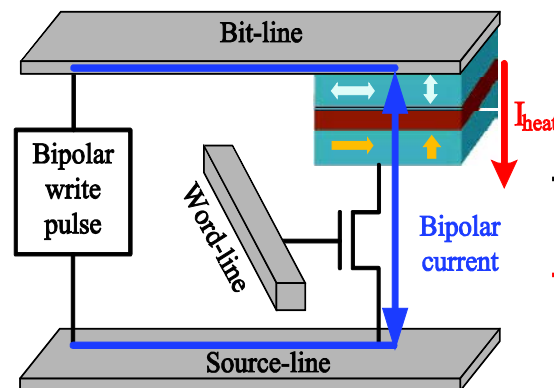
(c)

STT driven  
STT-MRAM



(b)

Thermal Assisted  
TA-STT-MRAM



(d)

# MRAM (Cont.)

- MRAM uses MTJ as non-volatile storage element
- Read based on the TMR ratio of MTJ
- ITRS reported that STT-MRAM is one of the most promising candidates for the next generation non-volatile memory.
- Many prototypes or small-scale chips have been proposed or commercialized in markets currently
- Intrinsic anti-radiation, promising for aerospace applications



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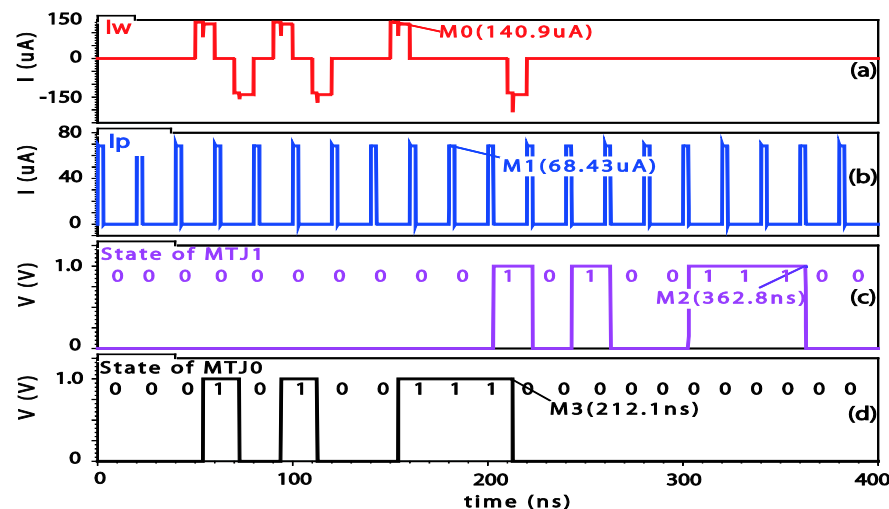
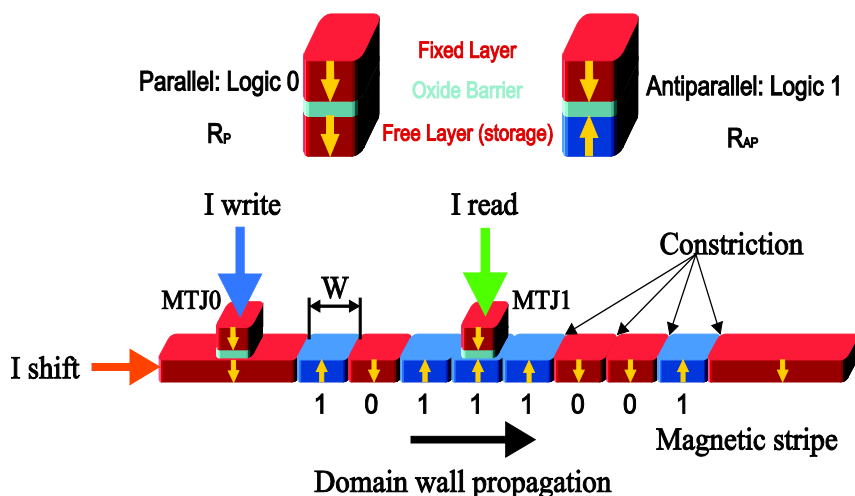
ASP-DAC 2014



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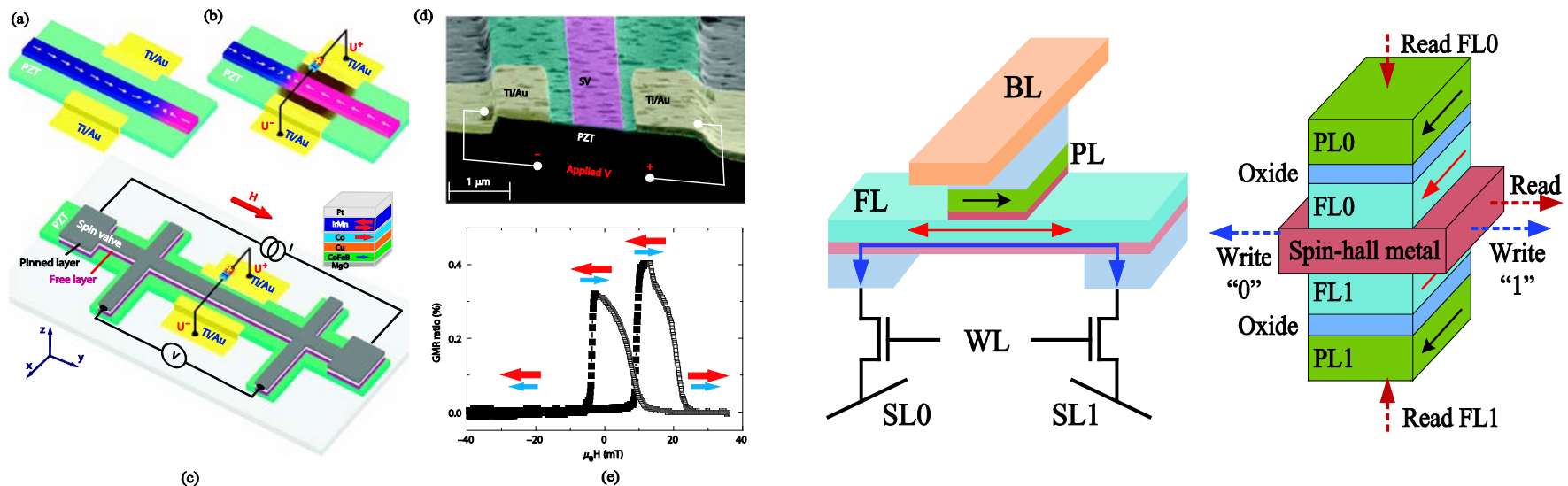
# Racetrack Memory

- Based on domain wall (DW) motion
- With MTJ as write and read heads
- Ultra-high storage density and low power operation
- One of the key challenges to build RM is to avoid any **pinning defects** in the magnetic strips



# Advanced Spin-based Memories

- Voltage-Controlled (DC) MRAM or DW motion
- Spin-Orbit Coupling memory devices
- Further reduce programming power VS STT
- Far away for practical applications



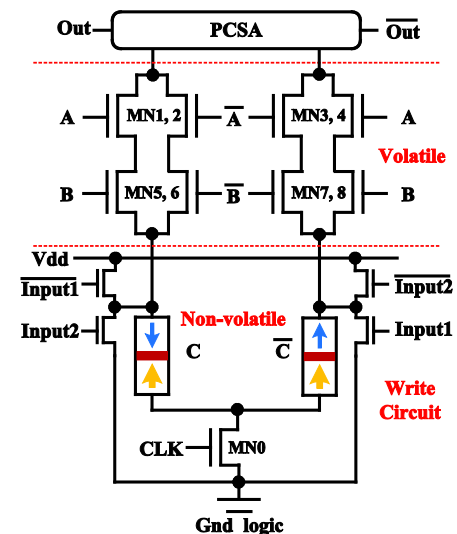
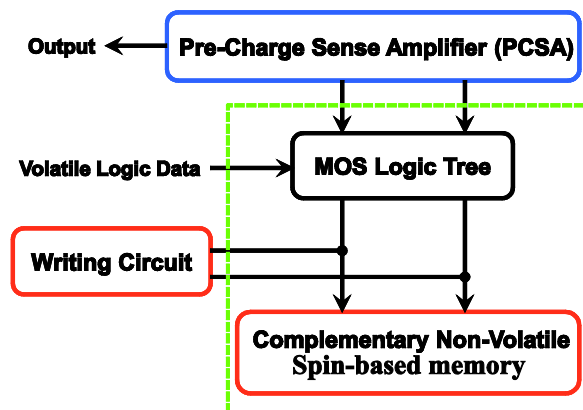
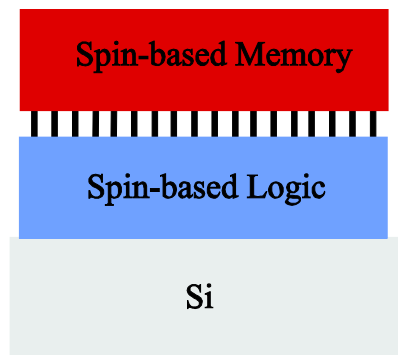
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# Hybrid MTJ/CMOS Logic Circuits

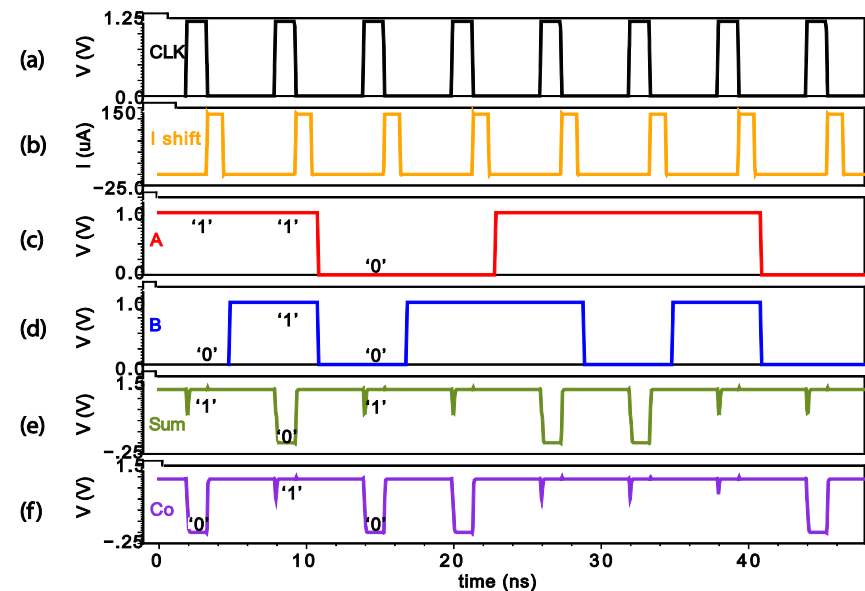
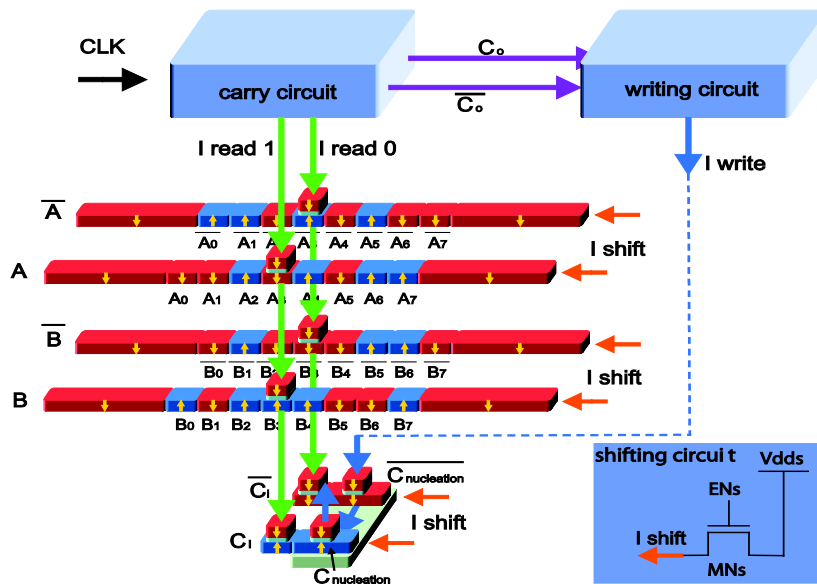
- Mainly based on the **logic-in-memory** structure
- Inputs partly volatile, partly non-volatile
- **3D integration** shortens traffic delay and power
- Low power and high speed



Erya Deng et al., *IEEE Trans. Magnetics*, vol.49, pp.4982-4987, 2013

# Domain Wall based Logics

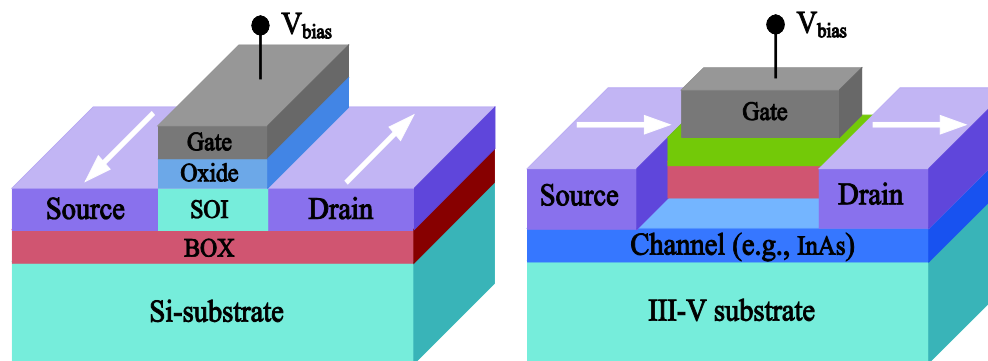
- All the data inputs are stored in non-volatile states
  - Area, power, delay overheads
- Same challenges as racetrack memory
  - Defects in magnetic nanowires



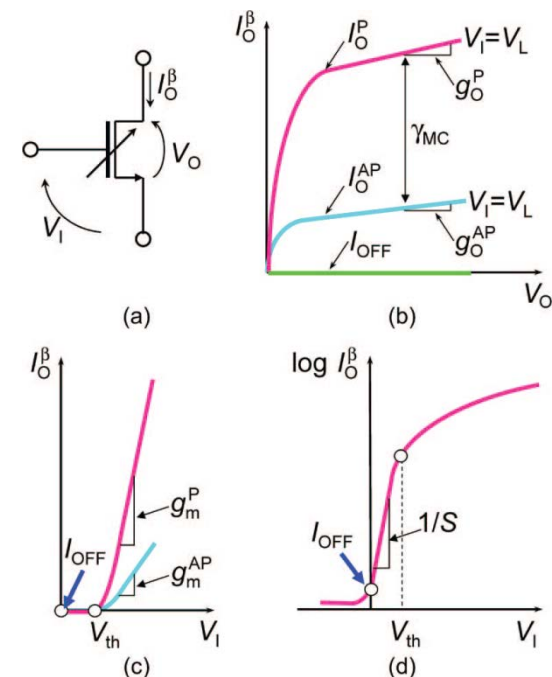
H-P Trinh, et al., *IEEE . Circuits and Systems I*, vol.60, pp.1469-1477, 2013.

# Spin-Transistors

- Concept has been predicted early in the 1990s, but it was experimentally developed recently
- **Most critical challenge for spin transistors is the “magic” material for the spin transport channel**
- Graphene has been proved generally the potentiality and capability for the channel material
- Spin-MOSFET and Spin-FET



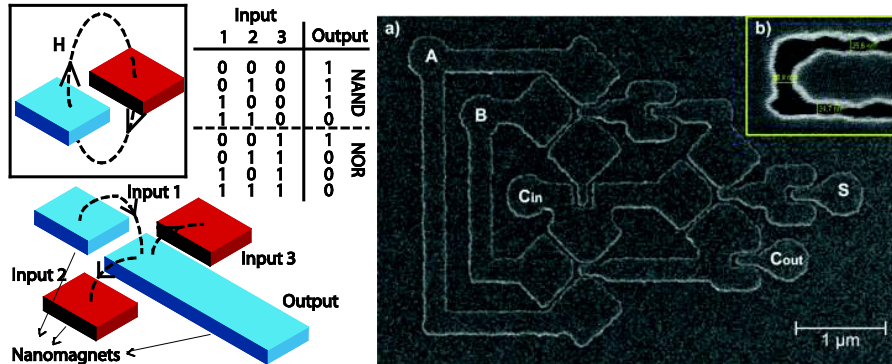
Sugahara S, Nitta J. Proceedings of the IEEE, 2010, 98(12): 2124-2154.



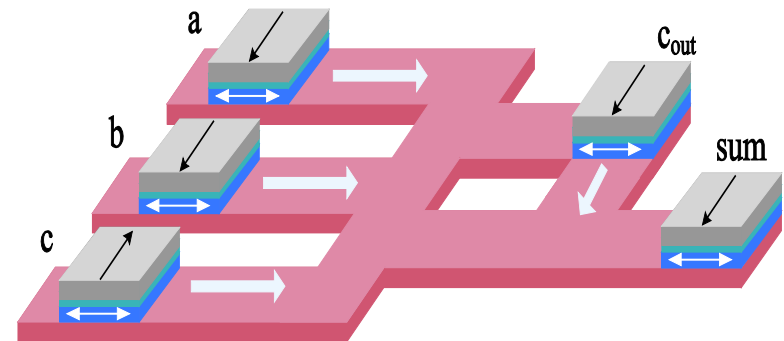
# All-Spin Logic and Nano-Magnetic Logic

- Uses nano-magnets as digital spin capacitors to store data and spin to communicate, realizing logic gates based on the **spin majority evaluation**
- **Ultra-low power and full spin system**
- Challenges for material, fabrication and controllability

Majority gate

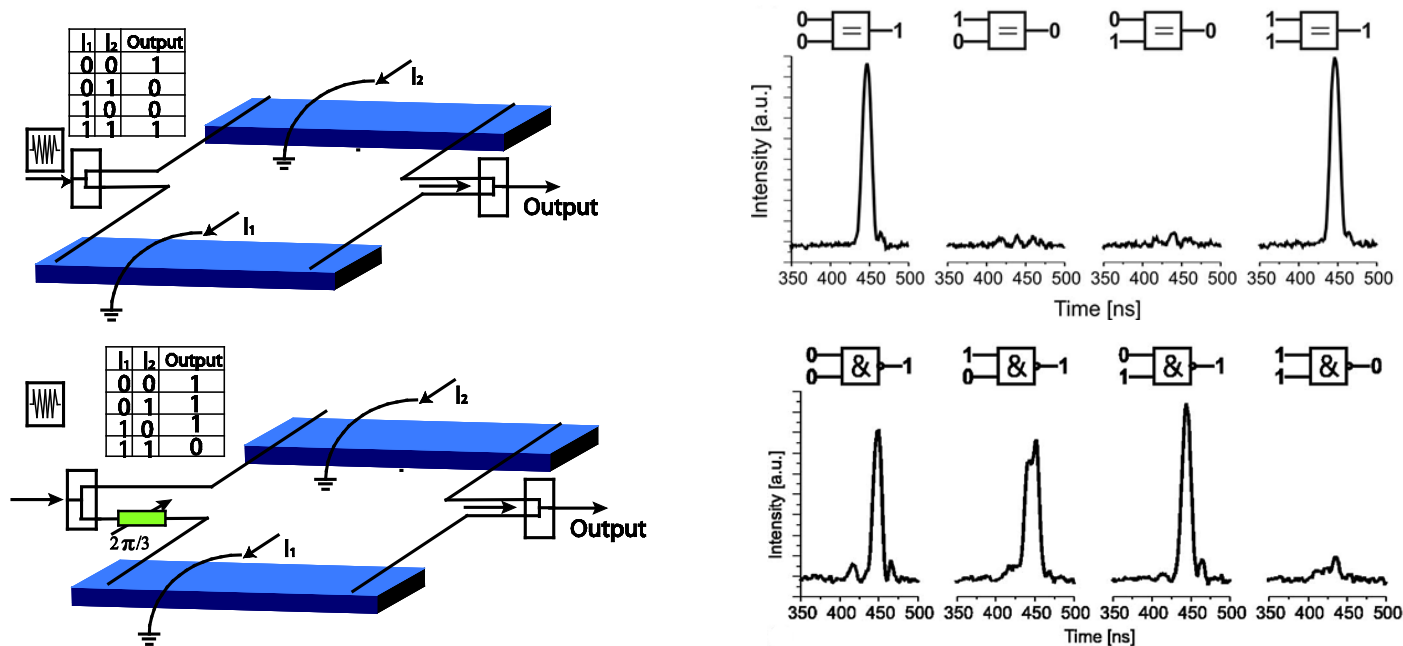


All spin full adder



# Spin Wave Logic

- It uses magnetic films as spin conduit of wave propagation, information can be coded into a phase or amplitude of the propagating spin wave
- Challenges: Spin wave amplitude decay and low spin wave phase velocity

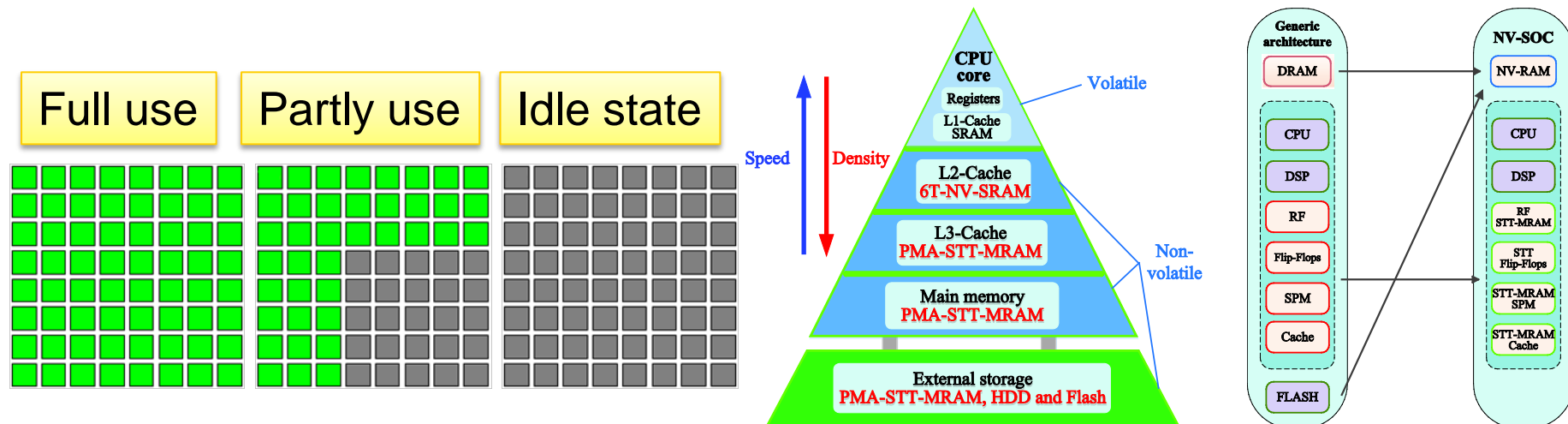


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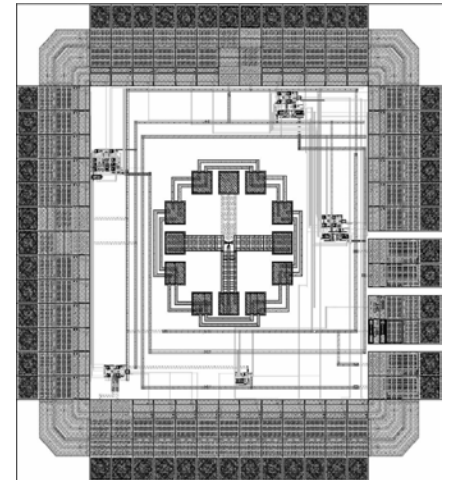
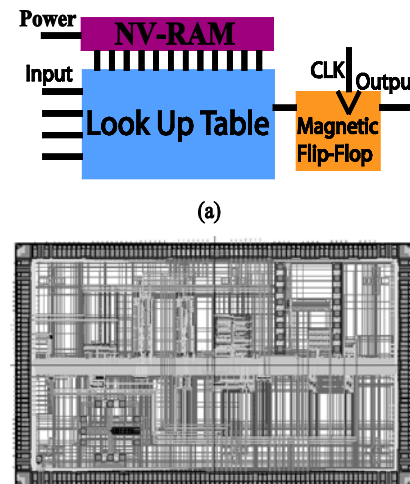
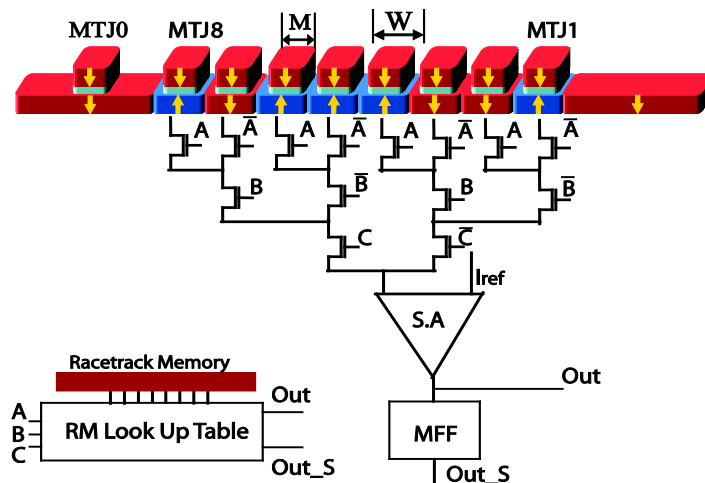
# Normally-Off Computing Systems

- Non-volatile storage: no static power
- “Instant on/off” capability
- Normally-Off when the CPU is in standby state
- Normally-On after power is reset
- Ultra-low power computing system



# Dynamic Reconfigurable Systems

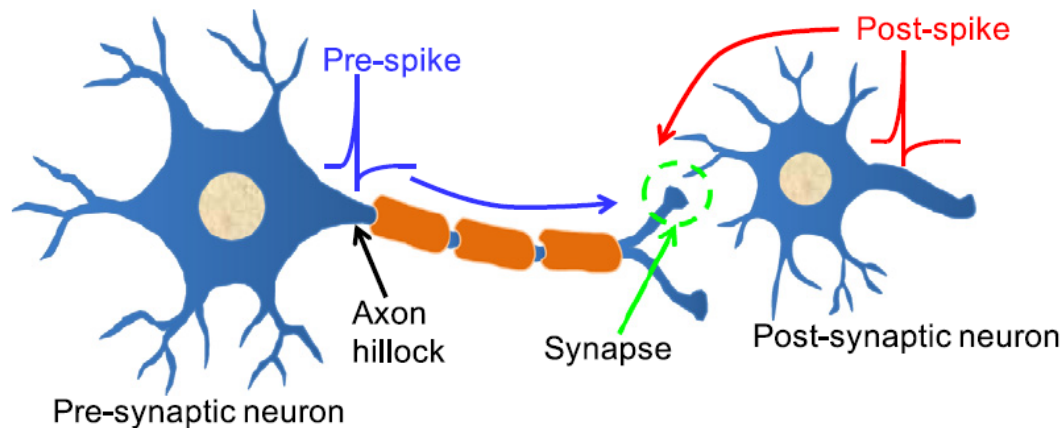
- FPGA with SRAM to store the configuration
  - Low power efficiency and logic density
  - Challenge for dynamically reconfigurable or in run-time
- Spin-based memory as configuration
  - STT-MRAM, TA-MRAM and racetrack memory etc



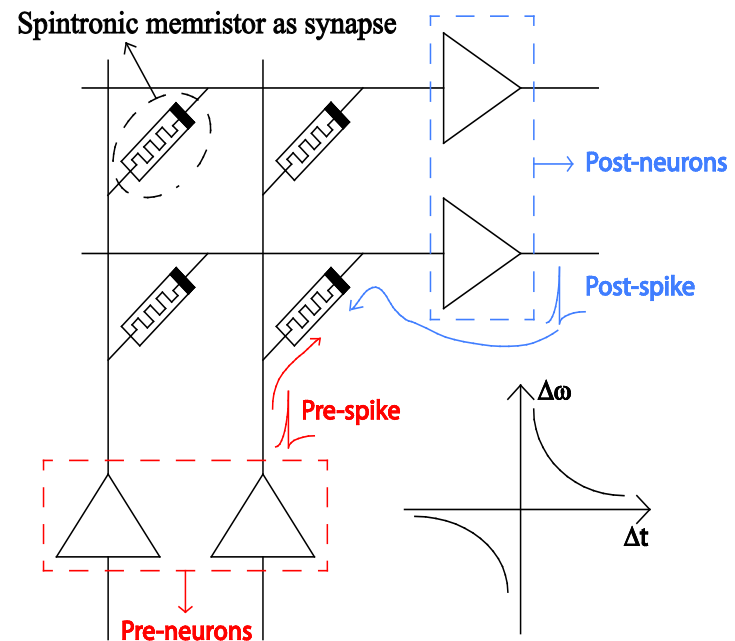


# Neuromorphic Systems

- Circuits and systems that work analogously to the brain
- Spintronics devices and memristor are the most promising candidates as synapse in neuromorphic systems currently
- Ultra-low power consumption
- Artificial intelligence



M. Sharad et al., IEEE Trans. Nano., Vol. 11, pp. 843-853, 2012.



K. Roy et al., IEEE ISLPED, pp.139-142, 2013.

# Conclusion and perspectives

- Overview of spin-based devices and circuits, their challenges and merits in current applications
- Emerging novel computing paradigms and architectures beyond Von-Neumann architecture
- In the short term (i.e., 5-10 years), **STT-MTJ/CMOS hybrid memory and logic** could be the major candidates to achieve the commercial steps.
- In the long term (i.e., 10-20 years), there isn't any evidence for any other devices or structures (e.g., **Graphene** based devices) to become the mainstream solution.

# Acknowledgement

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Thanks for your attention!  
Questions??