Asia and South Pacific Design Automation Conference ASP-DAC

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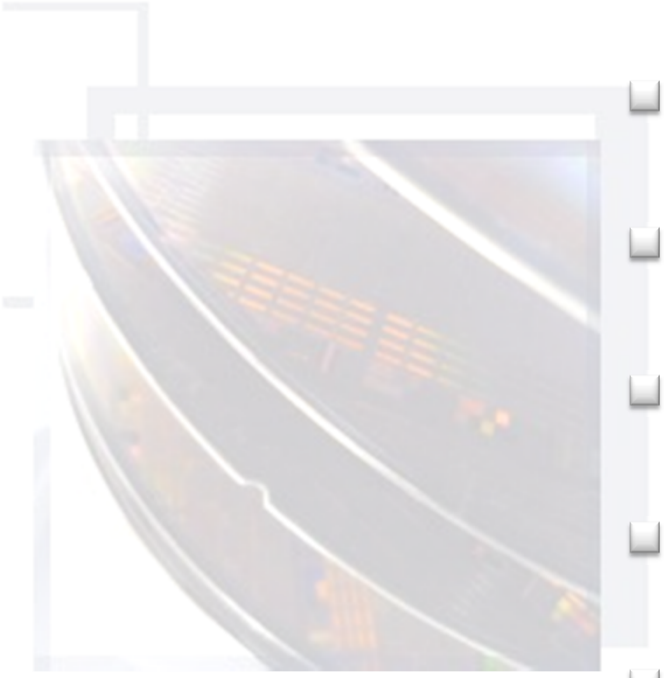
Hybrid CMOS / Magnetic Process Design Kit and SOT-based Non-volatile Standard Cell Architectures

CONTENT



- Introduction
- Magnetic Tunnel Junction overview
- Hybrid CMOS / SOT-Magnetic PDK
- Hybrid non-volatile flip-flop architectures
- Conclusion

Introduction

Magnetic Tunnel Junction overview

Hybrid CMOS / SOT-Magnetic PDK

Hybrid non-volatile flip-flop architectures

Conclusion

Need of MRAM / MTJ in Integrated Circuits

- **Adding non-volatility in ASIC**
  - → **Reducing the power consumption**
  - → **Improving the reliability of systems**

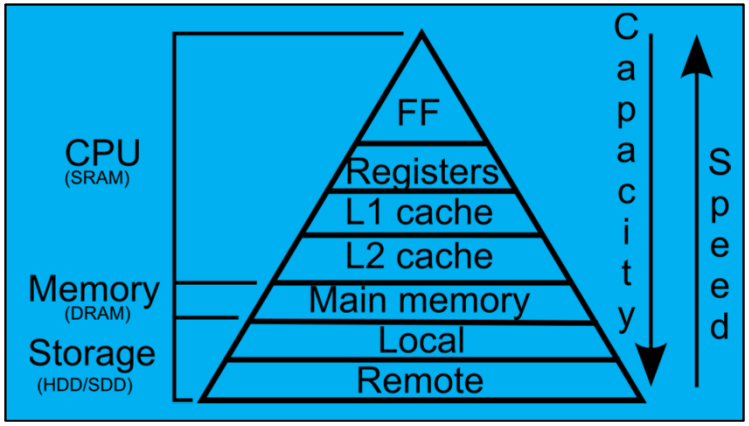


FIG. 1 : Memory hierarchy

- **MTJs can be integrated at several levels of memory hierarchy**
  - → **Memories** (not addressed in the presentation)
  - → **Logic blocks** (focus of this talk)
  - → **Differential reading :**

  1 Parallel and 1 anti-parallel

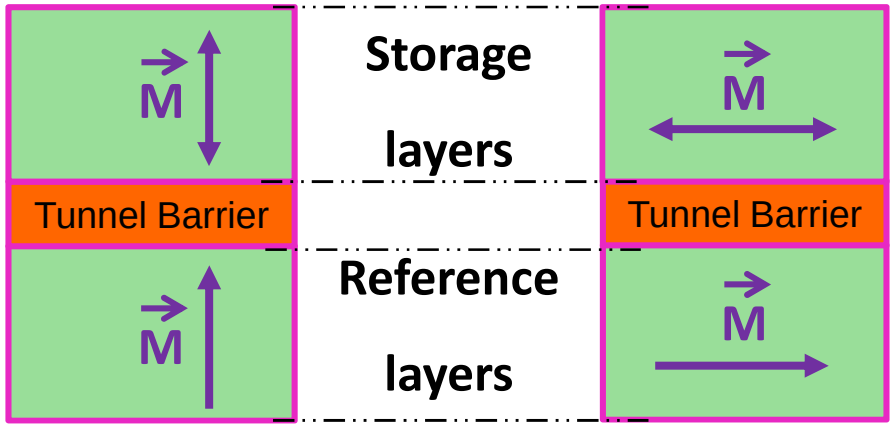


FIG. 2 : Perpendicular-to-plane and in-plane MTJ

Introduction

Magnetic Tunnel Junction overview

Hybrid CMOS / SOT-Magnetic PDK

Hybrid non-volatile flip-flop architectures

Conclusion

FIMS: Field Induced Magnetic Switching

- First generation of Magnetic Tunnel Junction
- Writing using an external field: ~60 Oe
- Combination of 2 field lines selecting 1 row and 1 column.
- Reading is activated by a select transistor
- ☺ Enable to start combining spintronics and microelectronics, mature process
- ☹ Scaling, selectivity, power consumption

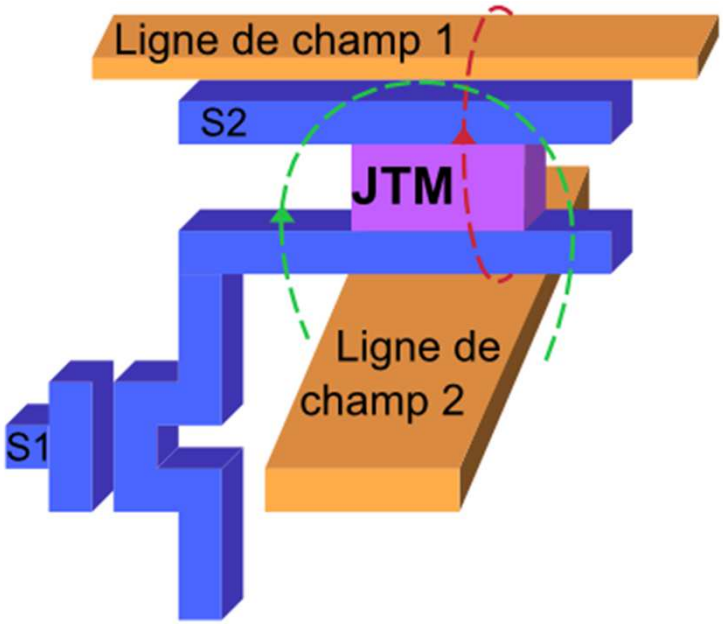


FIG. 3 : FIMS - MTJ

FIMS – Toggle: improvment of FIMS

- Storage layer = Synthetic Anti-Ferromagnet (SAF layer) composed of 2 FM layers
- Writing using an external field: ~90 Oe, based on a specific sequence
- 2 field lines as standard FIMS.
- ☺ Only product commercialized

  → Everspin
- 😐 Selectivity
- ☹ Scaling, power consumption

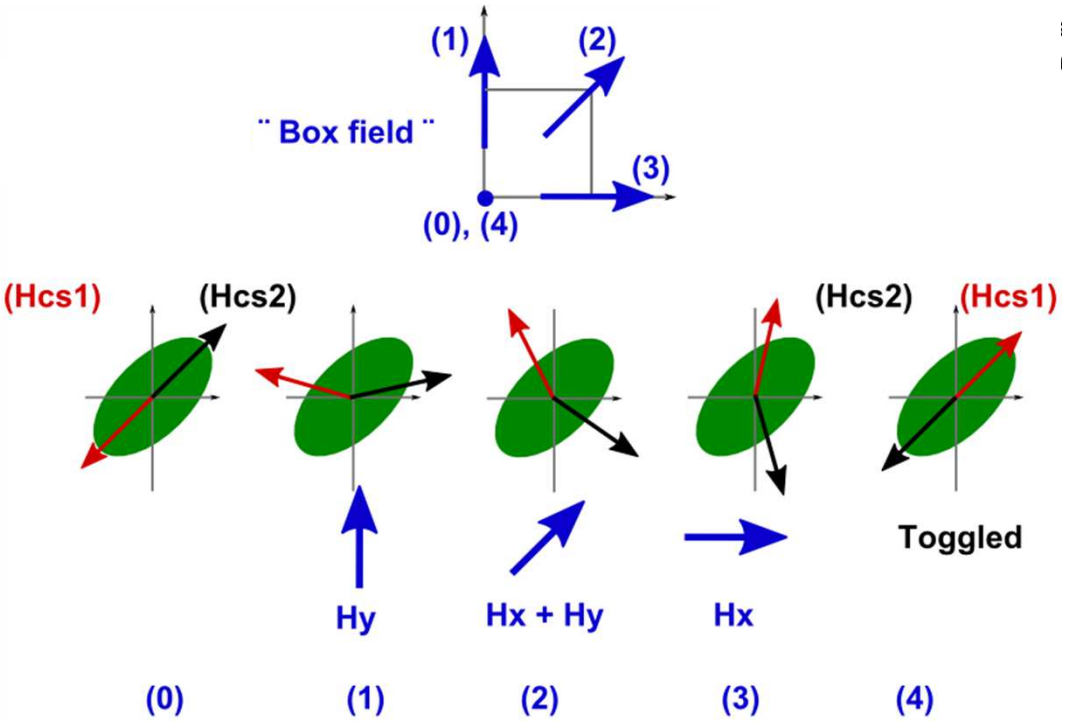


FIG. 4 : FIMS-Toggle writing mechanism

TAS: Thermally Assisted Switching

- Firstly proposed by Spintec Laboratory – France
- Industrialization by Crocus Technology
- Stability ensured by exchange energy with an Anti Ferro Magnet (AFM)
- Writing by a reduced external field, eased by heating the MTJ.

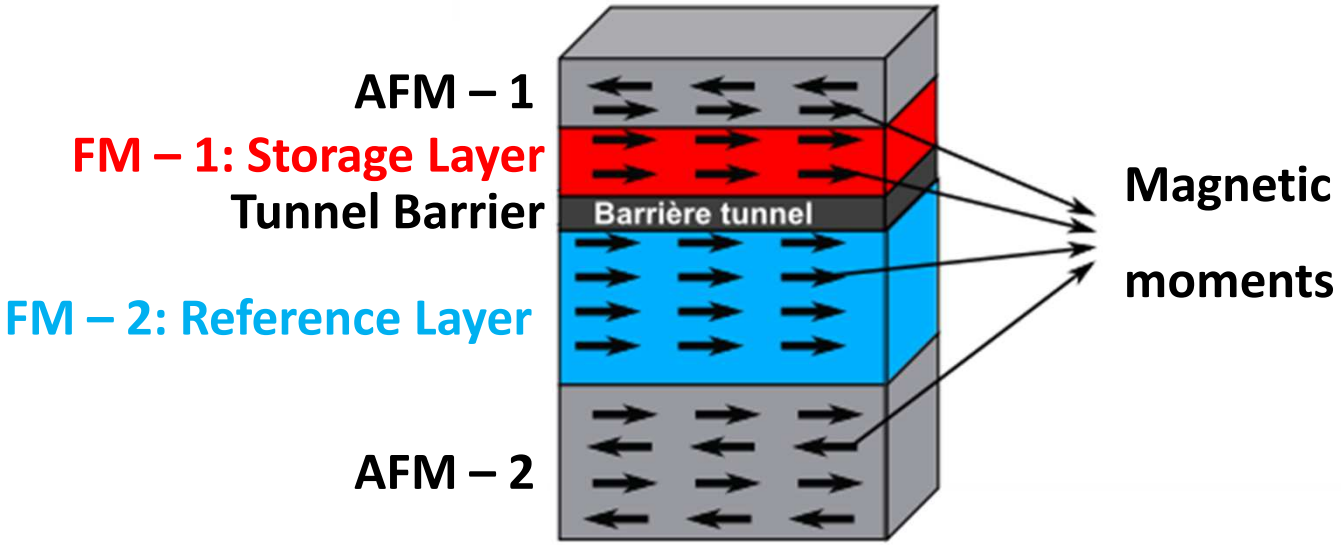


FIG. 5 : TAS - MTJ stack

TAS: Thermally Assisted Switching

- Only 1 field line
- ☺ Selectivity
- 😐 Scalability, reduced writing field, power consumption
- ☺ Thermal stability
- ☹ Writing speed limited by heating / cooling

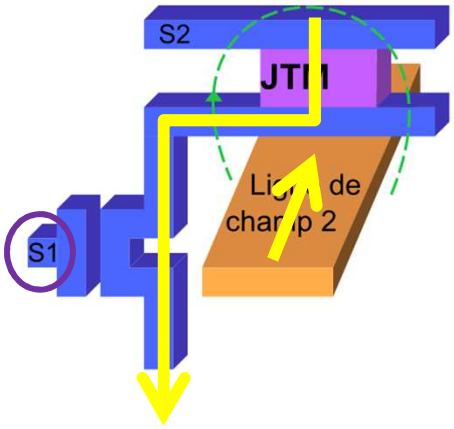


FIG. 6 : TAS - MTJ

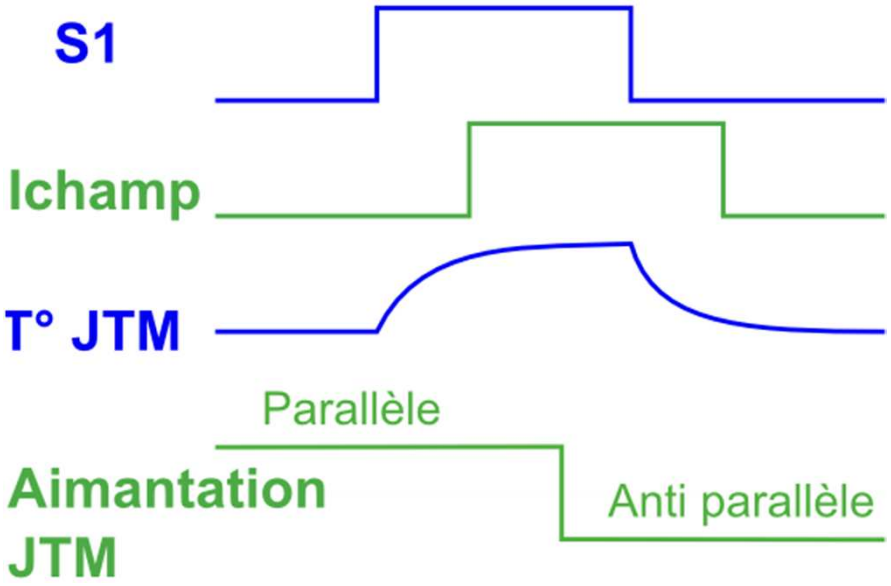


FIG. 7 : TAS writing mechanism

STT: Spin Transfer Torque switching

- Writing with spin polarized current
- In-plane or perpendicular-to-plane anisotropy

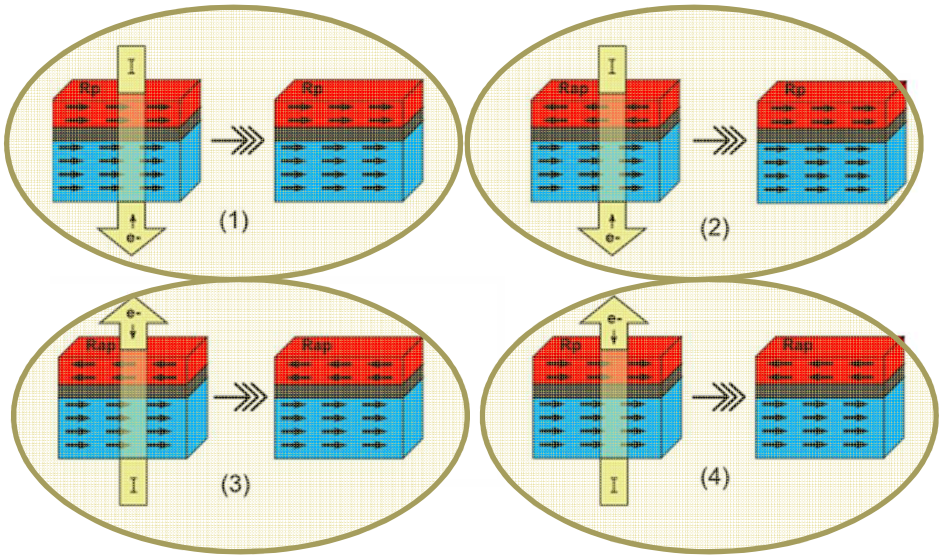


FIG. 8 : STT - MTJ writing mechanism

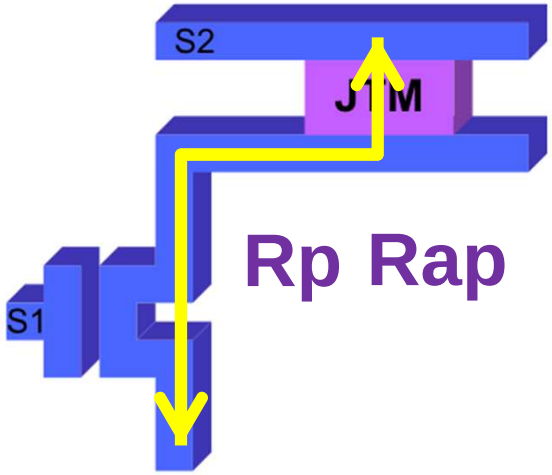


FIG. 9 : STT - MTJ

- ☺ Selectivity, low writing current, W/R high speed (~2-5 ns), density, scalability
- ➔ The current most promising MRAM technology
- 😐 Read disturb: writing during a reading phase + barrier damaging when writing, stochastic effects

SOT: Spin Orbit Torque switching

- Writing with in-plane polarized current at the interface conductor / storage layer

  → Rashba and Spin Hall effect

- 3-terminal device

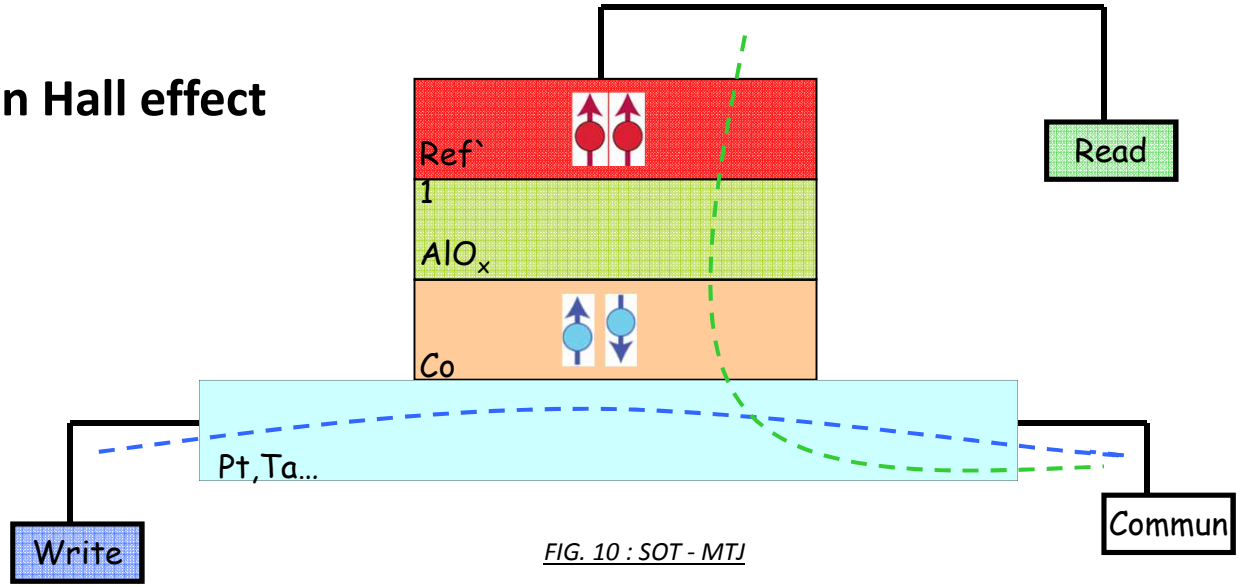


FIG. 10 : SOT - MTJ

- ☺ Reliability : different reading and writing path → no more read disturb and no tunnel barrier damaging, symmetrical writing P / AP.

- ☺ Ultra fast writing (~0.5-2 ns), fast reading, low writing energy, scalability

- 😐 Last MTJ generation → process under development, density depending on the architectures but can be as dense as STT

Introduction

Magnetic Tunnel Junction overview

Hybrid CMOS / SOT-Magnetic PDK

Hybrid non-volatile flip-flop architectures

Conclusion

Hybrid CMOS / SOT-Magnetic PDK

- Need full hybrid CMOS / magnetic Process Design Kit (PDK)
- → Electrical simulation model: developed
- → Schematic environment
- → Layout environment
- → Design Rule Checking: DRC
- → Layout Vs Schematic: LVS
- → Parasitic extraction

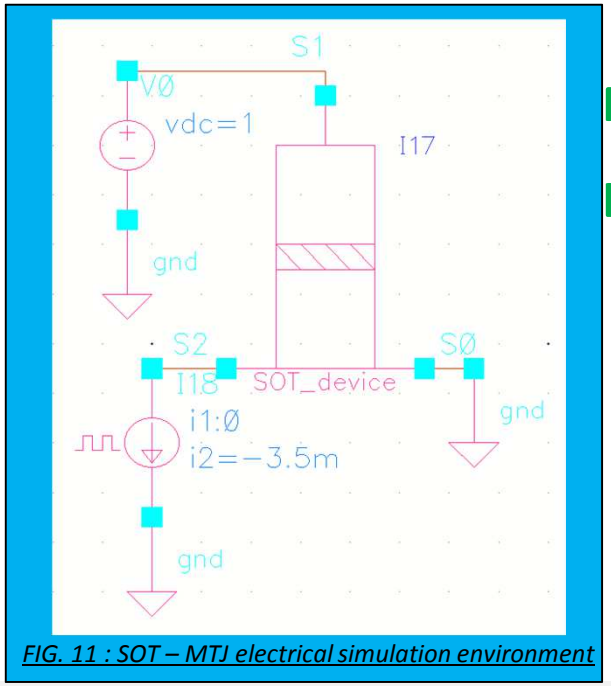
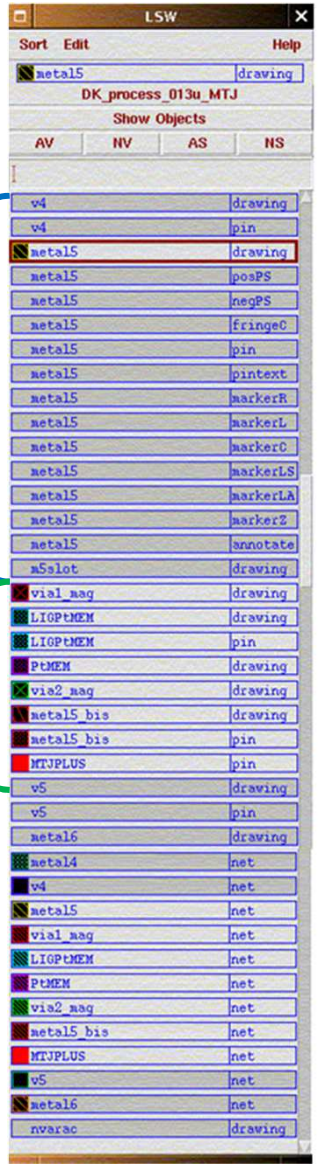


FIG. 11 : SOT – MTJ electrical simulation environment



CMOS Layers

Magnetic Layers

FIG. 12 : Hybrid LSW

SOT compact simulation model

- Verilog A language: compatible with all electrical simulators (Spectre, Eldo, …)
- Behavioral and very accurate versions, based on physics
- Composed of 2 modules: * Landau–Lifshitz–Gilbert equations (LLG)

  * Tunnel Magneto Resistance variation (TMR)

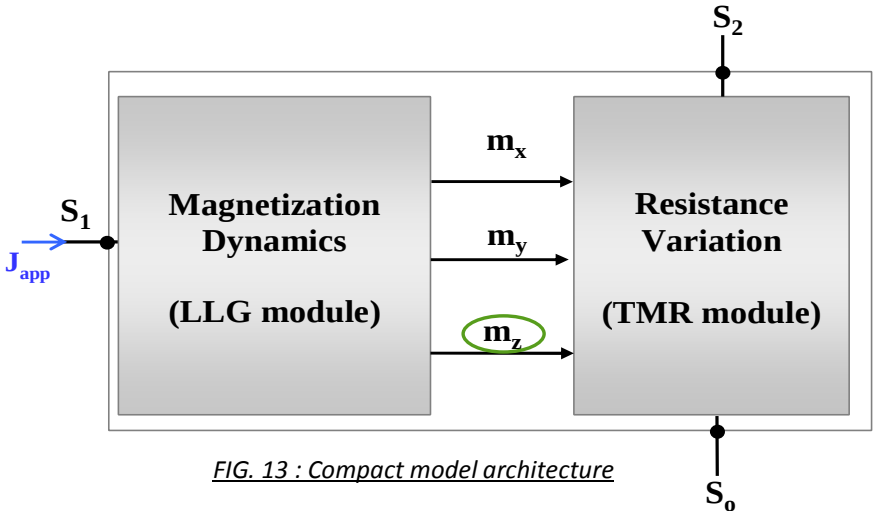


FIG. 13 : Compact model architecture

- Current density applied as input (Japp)
- Resistance value and variation as output.

SOT: Compact simulation model

- **LLG Module** → Crystalline anisotropy field
  → Demagnetizing field
  → Rashba field
  → Spin Hall Effect field
  → External applied field

$$\vec{H}_{eff} = \vec{H}_k + \vec{H}_d + \vec{H}_R + \vec{H}_{SHE} + \vec{H}_a$$

- **TMR Module (Tunnel Magneto Resistance)**
  → Magnetization (Mx, My, Mz) from LLG as inputs
  → Resistance variation as output
  → Gives the dynamic resistance of the SOT-MTJ: essential for logic design
  → Jullière, Slonczewski, Brinkman and Simmons's theory (MR, tunneling…)
  → TMR depends on the voltage applied to the SOT-MTJ: very important effect for designers, especially for the reading phases (TMR_0 lowered)

SOT compact model: validation and study

Validation of the dynamic behavior

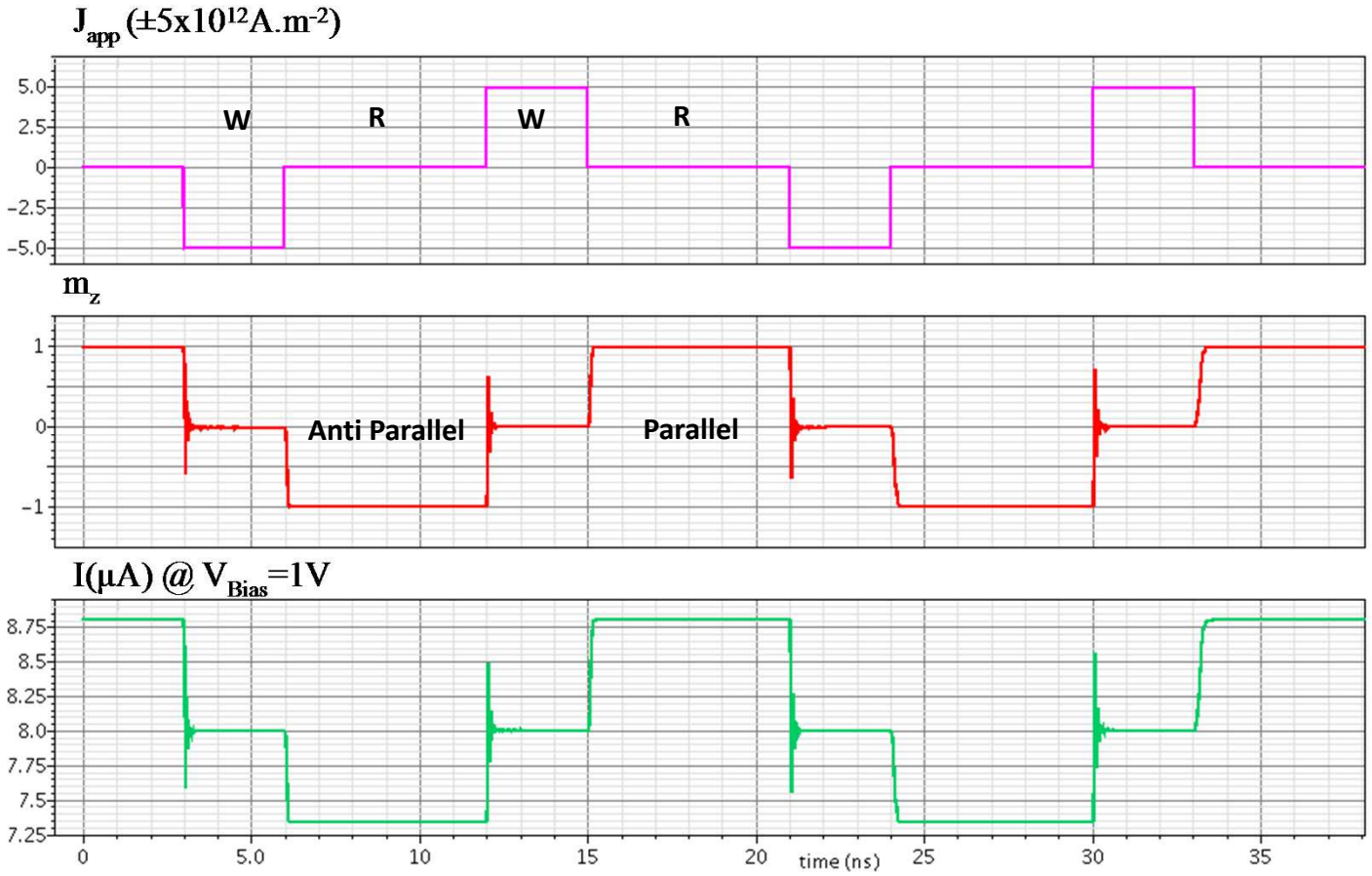


FIG. 14 : Validation of the magneto resistance variation according to current pulses or MTJ states

➔ **Complete studies based on several effects are possible**

SOT compact model: validation and study

- **Electrical simulation without external field (Ha = 0)**

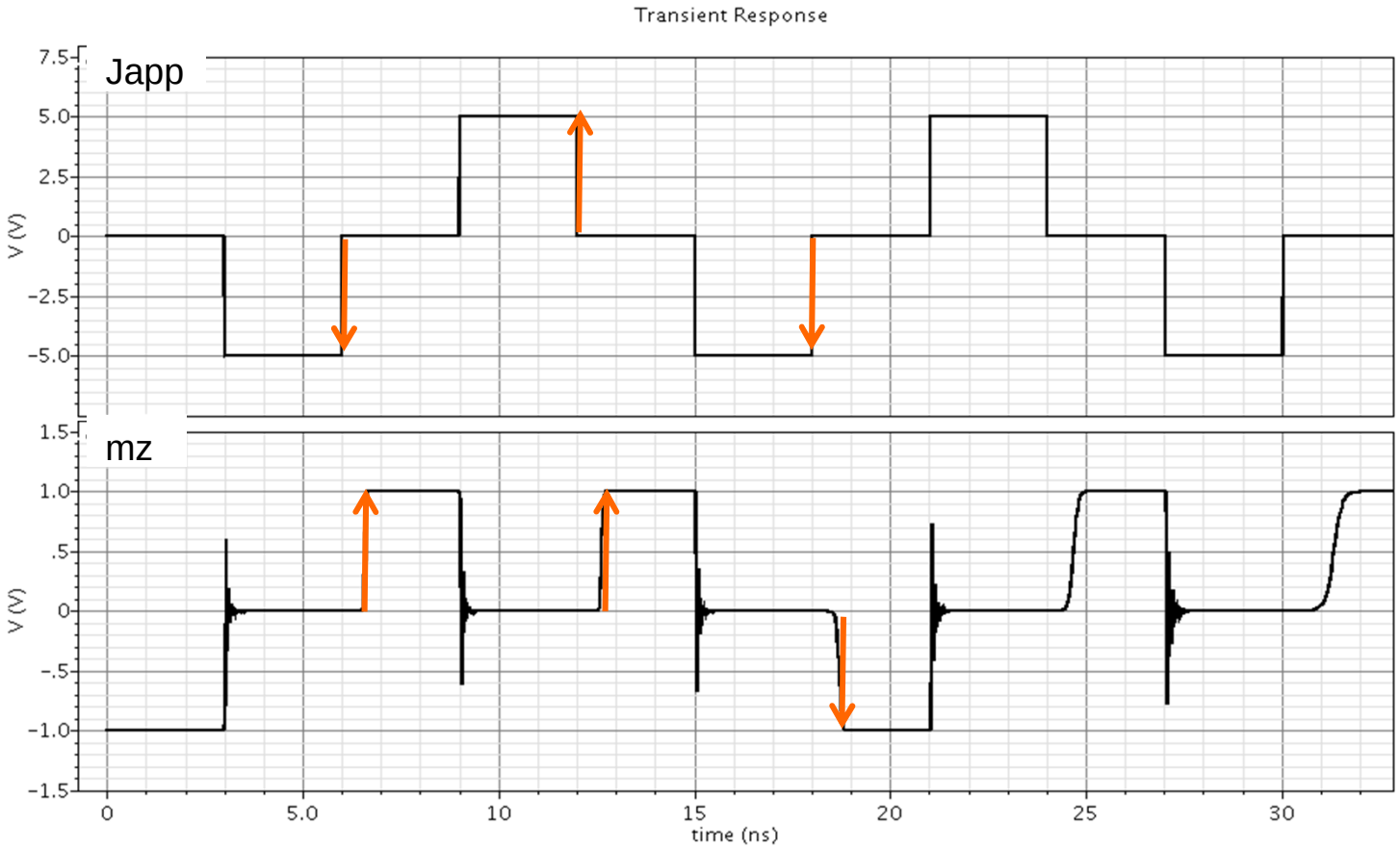


FIG. 15 : Influence of the external field

➔ **Without external field the magnetization switching is random**

SOT compact model: validation and study

Electrical simulation with external field (Ha ≠ 0)

3ns pulse, $J_{app}=5^{E}12$ A/m², Ha_x= -5mT

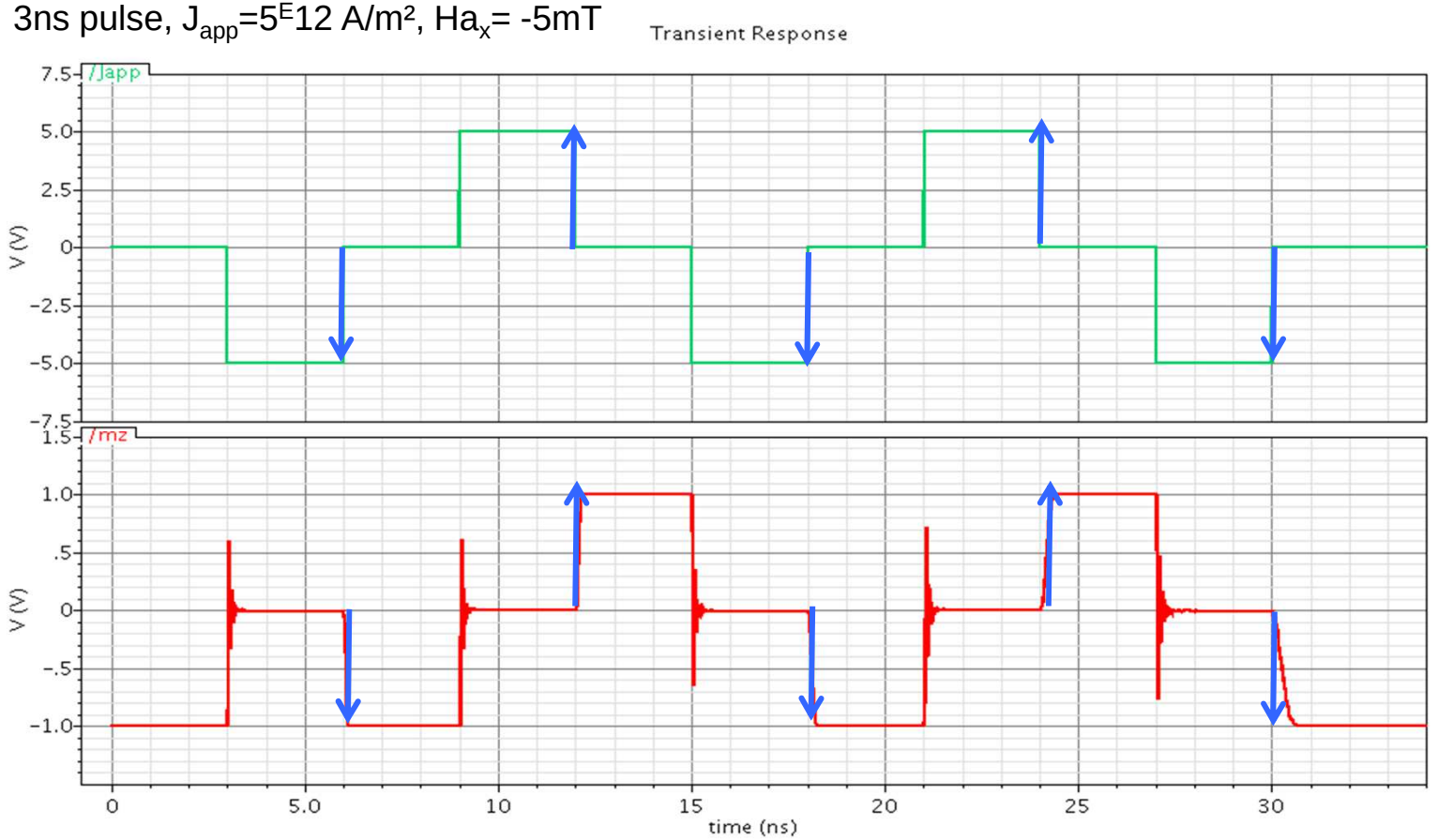


FIG. 16 : Influence of the external field amplitude

➔ **With an external field the magnetization switching is deterministic. It depends on its orientation (Ha > 0 or Ha < 0)**

SOT compact model: validation and study

Electrical simulation with an external field (Ha ≠ 0)

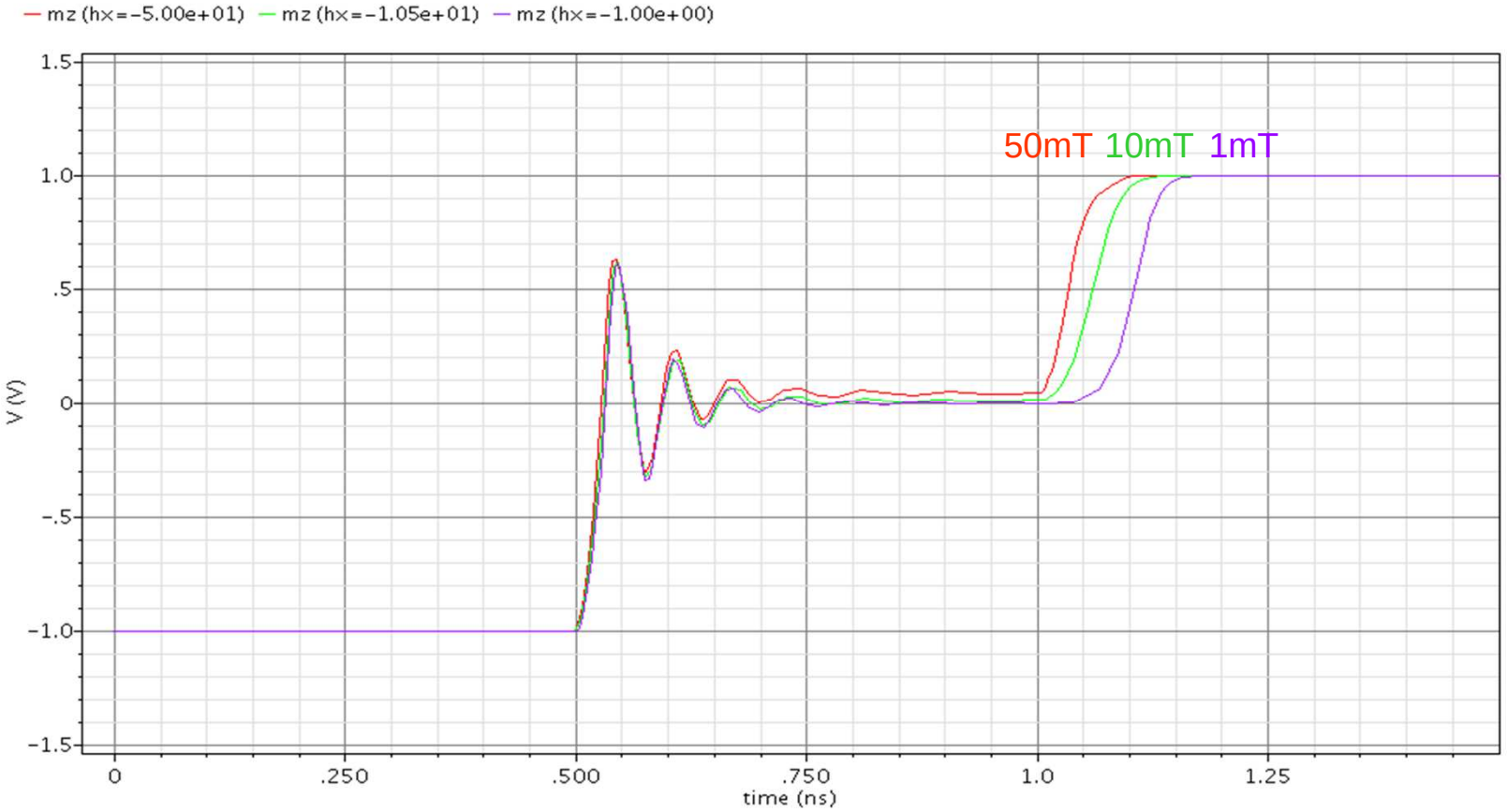


FIG. 17 : Influence of the external field amplitude

➔ **The higher the external field, the faster the magnetization switching**

SOT compact model: validation and study

- **Variation of Japp from 1.10^{12} A/m² to 8.10^{12} A/m²**

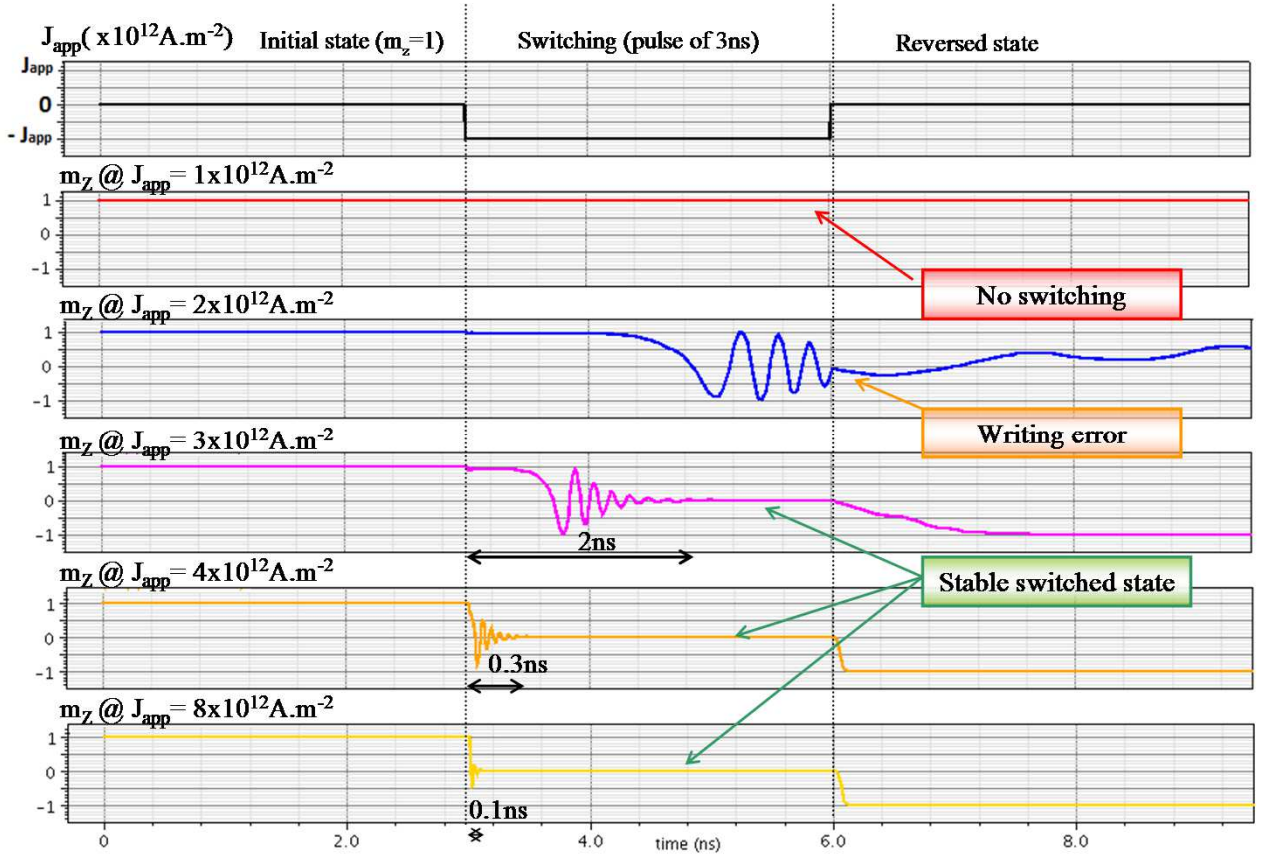


FIG. 18 : Evolution of m_z according to the current density J_{app}

➔ **The higher writing current density, the faster the magnetization switching**

SOT compact model: validation and study

- **Variation of pulse width from 3ns to 12ns**

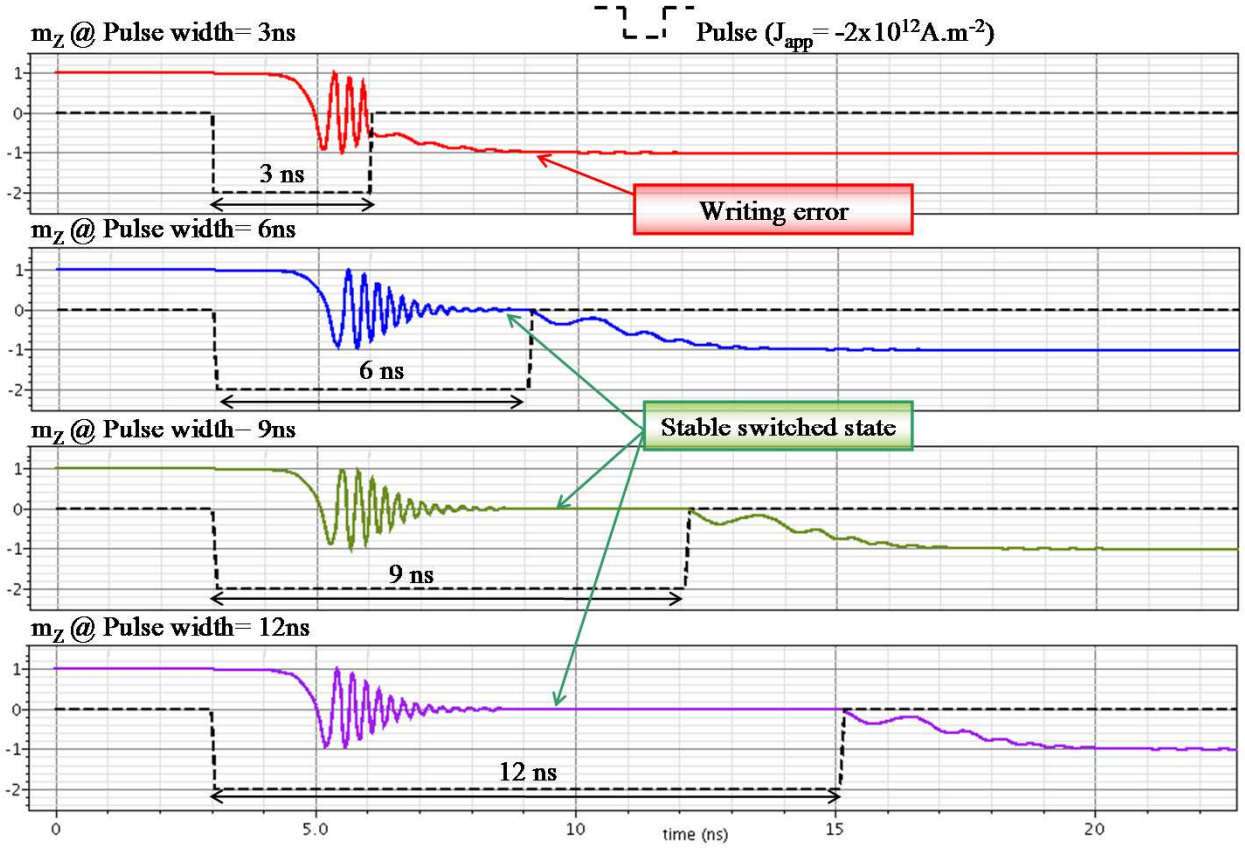


FIG. 19 : Evolution of m_z according to the pulse width @ J_{app} = -2x10^{12} A.m^{-2}

➔ **The larger the writing pulse, the safer the magnetization switching**

Introduction

Magnetic Tunnel Junction overview

Hybrid CMOS / SOT-Magnetic PDK

Hybrid non-volatile flip-flop architectures

Conclusion

Memory in logic

- **Adding MTJ in the logic can:**
  - → **Ease the power gating technics**
  - → **Reduce the power consumption**
  - → **Quasi "zero" standby leakage**
  - → **Instant on / normally off**

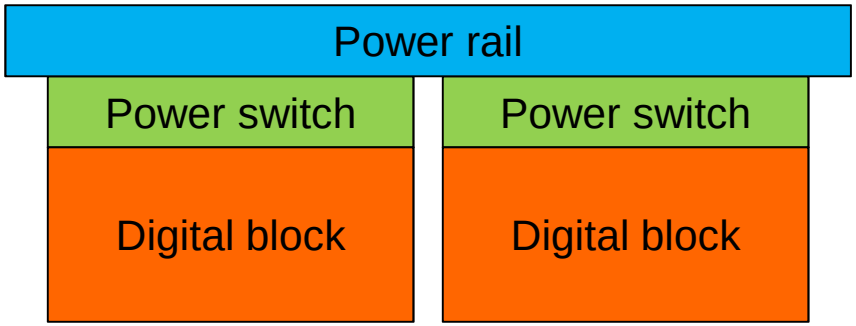


FIG. 20 : Digital floorplan

- **Increase the reliability of systems**
  - → **Save / restore the flip-flop outputs**
  - → **Store a configuration in a register file**
    - ➔ **Need of non-volatile flip-flops**

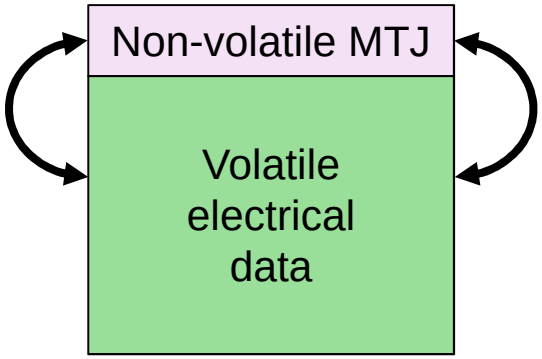
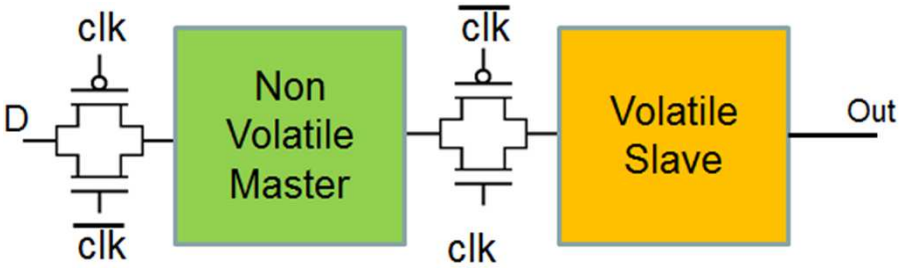


FIG. 21 : Electrical and magnetic data exchange

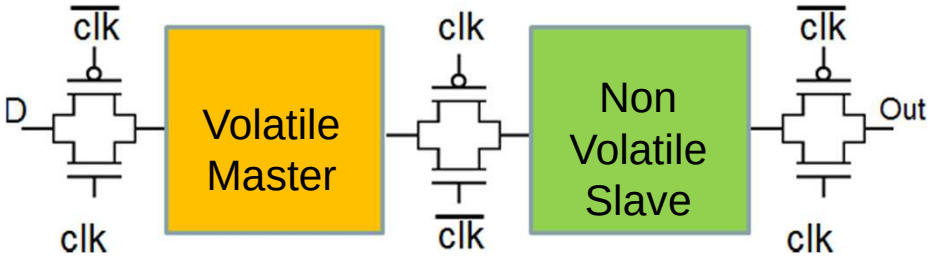
Hybrid non-volatile flip-flop

Non-volatility within the master



- The save and restore phases can be done between 2 clock edges. The flip-flop output is always valid.
- The input capacitance can be quite high depending on the SOT-MTJ features (large transistors for writing) → slower behavior

Non-volatility within the slave



- The flip-flop capacitance input is the same as a CMOS flip-flop → the speed CMOS speed is preserved
- Need two additional pass-gates cell to disconnect the flip-flop from the following blocks of the IP.

FIG. 22 : non-volatile flip-flop principle

Hybrid non-volatile latch: TAS based

- PMOS Low Vt ; NMOS High Vt
- 2 TAS-MTJ → differential reading
- 2 additional PMOS for writing (2 phases)

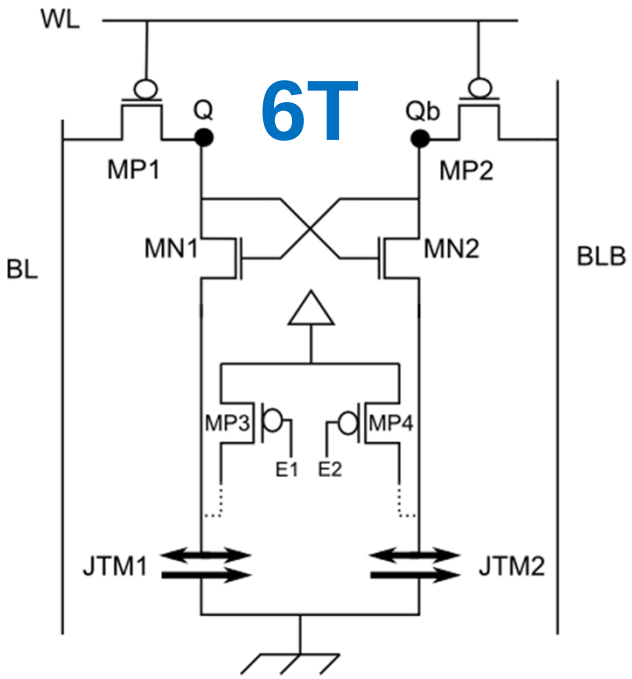


FIG. 24 : non-volatile 4T load less latch with writing transistors

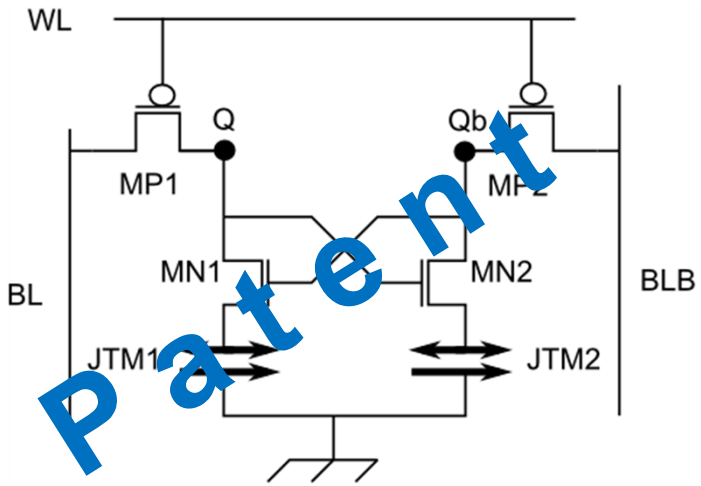


FIG. 23 : non-volatile 4T load less latch

4T Load less SRAM based

Hybrid non-volatile latch: TAS based

- ~~2additional PMOS for writing~~ : same writing and reading path
- Specific writing sequence

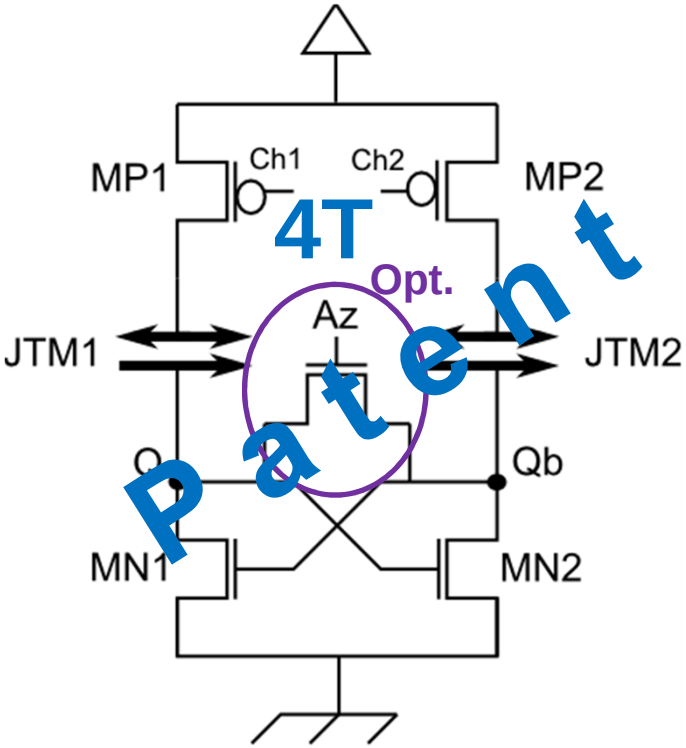


FIG. 25 : non-volatile 4T load less latch with no additional writing transistors

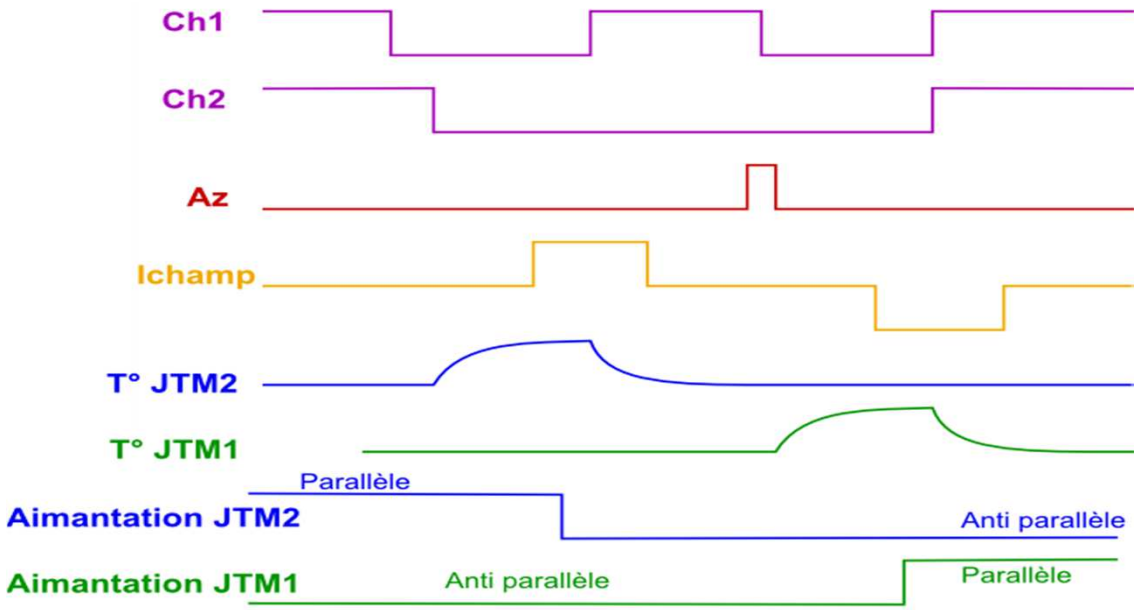


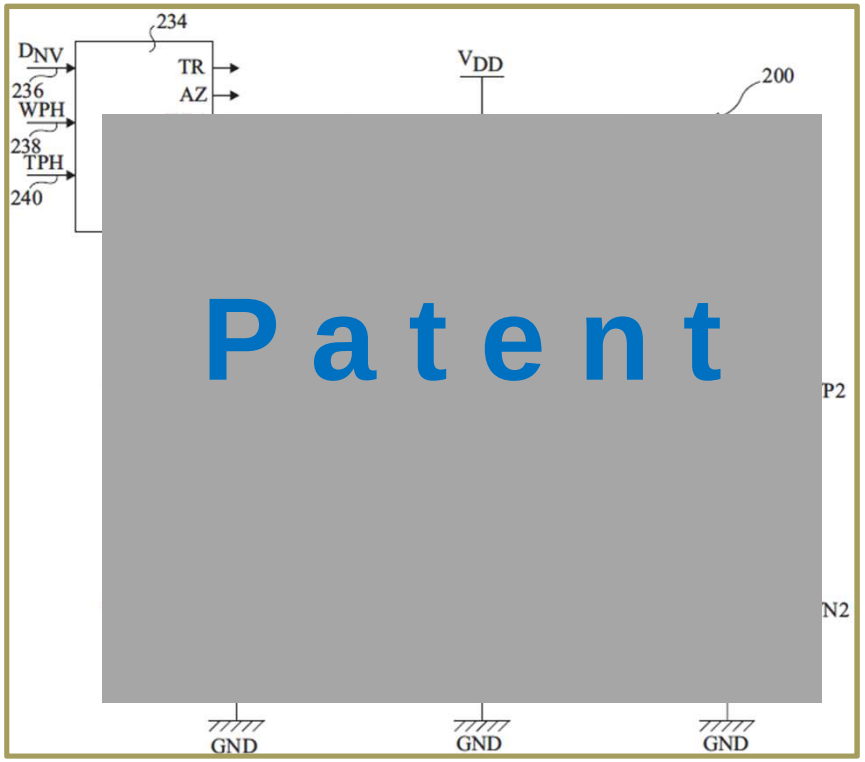
FIG. 26 : non-volatile 4T load less latch with no additional writing transistors chronogramme

- ☺ Very dense
- ☹ Speed (2 phases)

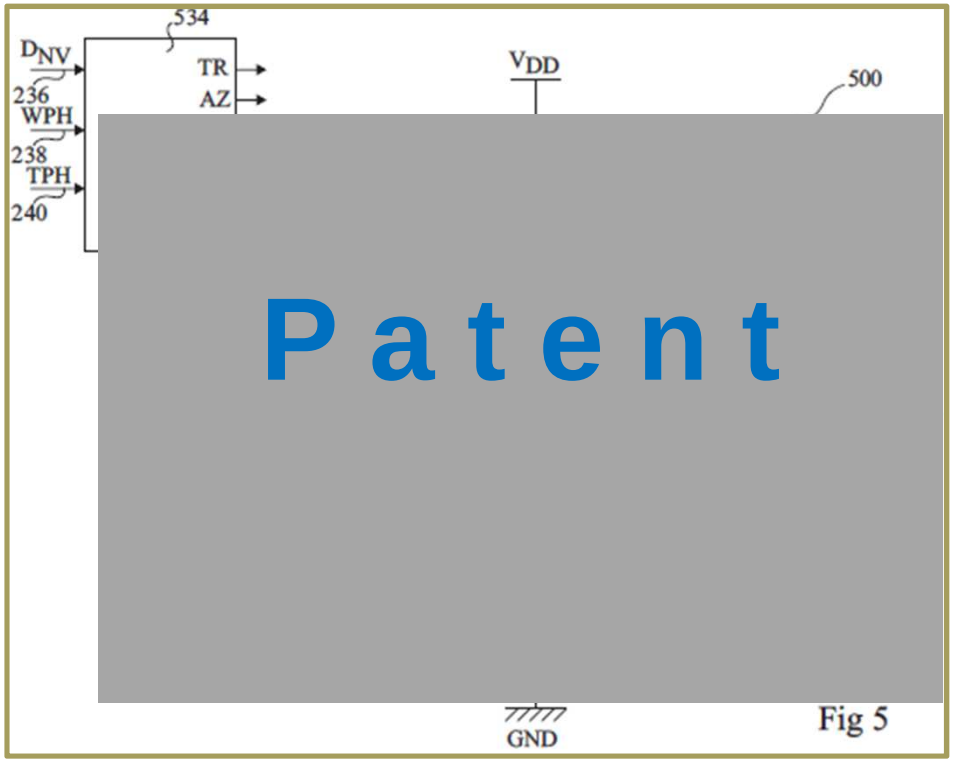
Hybrid non-volatile latch: STT based

- Cross-coupled based
- High Vt and Low Vt transistors
- Dense architecture
- Both CMOS and Magnetic behavior

- Simple control logic
- Denser architecture
- Use of body biasing in FD-SOI technology → number of transistors reduced



Patent



Patent

Fig 5

Hybrid non-volatile latch: SOT based

Cross-coupled based latch: validated by electrical simulation using the compact model

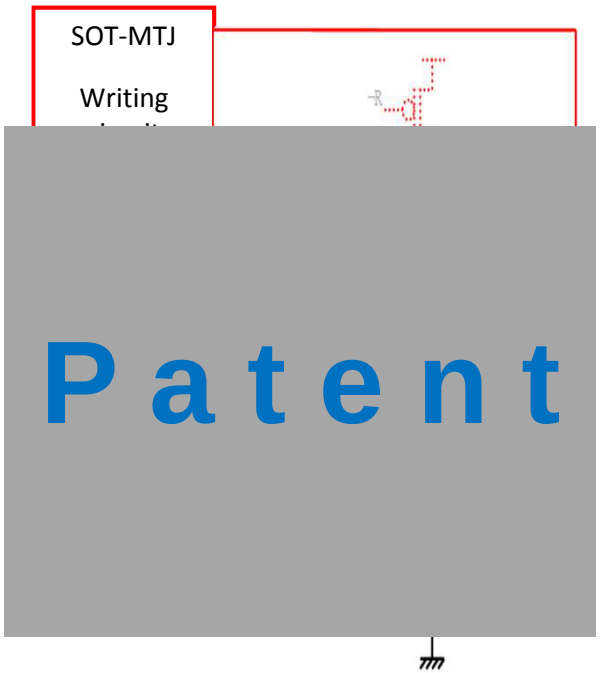


FIG. 27 : Cross-coupled-based non-volatile latch

Dense architecture

Hvt and Lvt transistors, higher standby leakage

SRAM based latch: validated by electrical simulation using the compact model

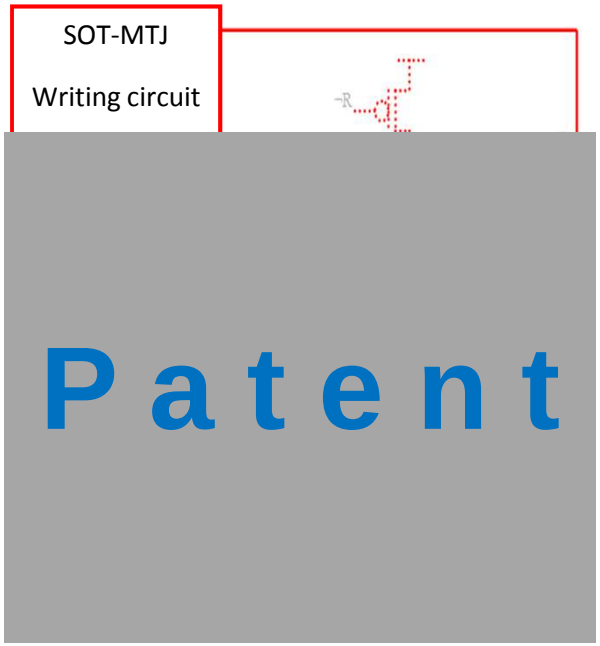


FIG. 28 : SRAM-based non-volatile latch

Well know architecture, stable, few standby leakage

Need more transistors.

Optimized SRAM based latch: use of precharge

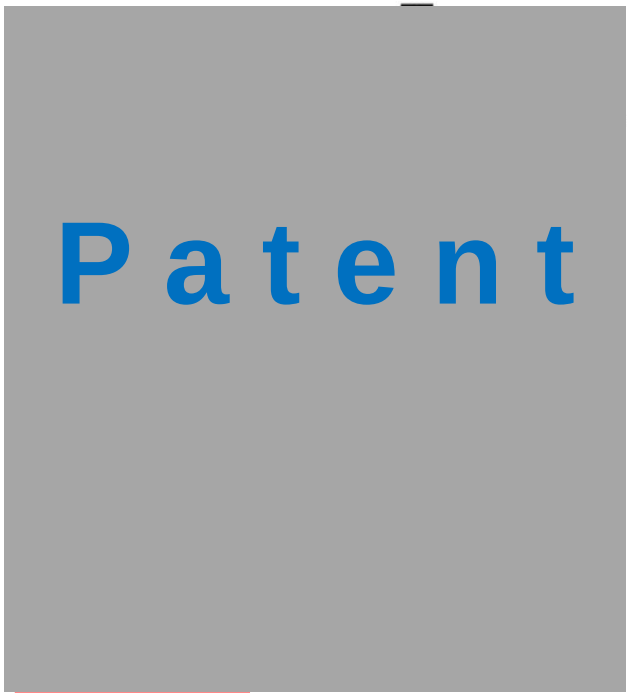


FIG. 29 : Optimized SRAM-based non-volatile latch

Same as SRAM-based + speed increased, reliability

Need more transistors.

Introduction

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Hybrid CMOS / SOT-Magnetic PDK

Hybrid non-volatile flip-flop architectures

- **Conclusion**

Conclusion

- Very good knowledge on the MTJs physics within Spintec
- Able to develop compact model for electrical simulation
- Full hybrid CMOS / Magnetic Process Design Kit currently under development
- Enable process improvement according to the simulation study
- Many flip-flops architectures proposed for all MTJ generations

FUTUR WORK

- Integrate these flip-flops within digital block and / or higher design level
- Design more complex ASICs

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