Design and Control Methodology for Fine Grain Power Gating based on Energy Characterization and Code Profiling of Microprocessors

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Outline

- Background
- Conventional techniques and problems
- Our approach
- Experimental results
- Conclusions and future work

Background

- Leakage power: most important issue in nanometer
- Power gating (PG)
  - Coarse-grain PG
    - granularity: processor-core(s) / IPs e.g. Intel's Nehalem
    - powered-off period: tens of μs - ms
    - drawback: limited opportunities to reduce leakage
  - Fine-grain PG
    - granularity: logic blocks within a core / IP
    - powered-off period: order of ns

Issues in fine-grain PG (FGPG)

- Quick wakeup from sleep (powered-off) state
- Suppression of ground-bounce noise at wakeup
- Energy overhead due to power-off / power-on

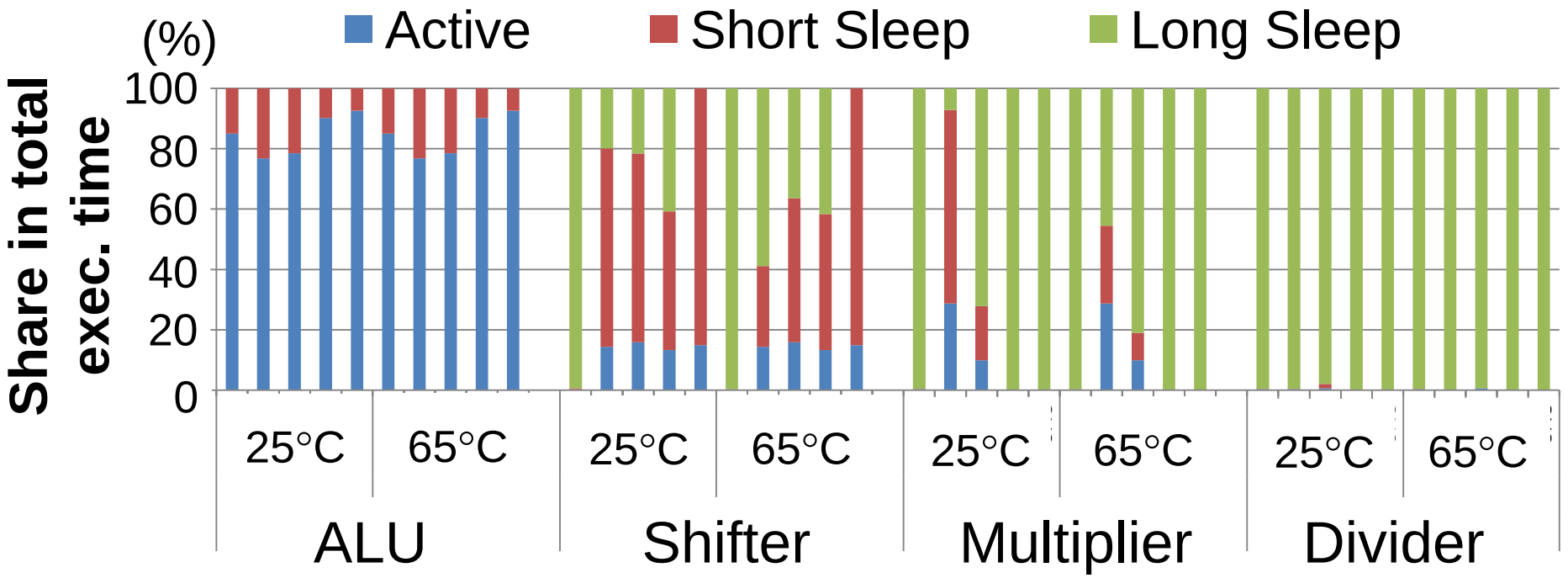
  ➔ Too short powered-off period does not lead to energy reduction

- Break-even time (BET)
  - Minimum powered-off time to gain in energy savings

Characteristics of idle periods

- Analyzed length of idleness and occurrence at "function units" in 32-bit MIPS microprocessor for 5 different apps.

Short (Long) sleep: idleness shorter (longer) than BET



Conventional techniques for FGPG

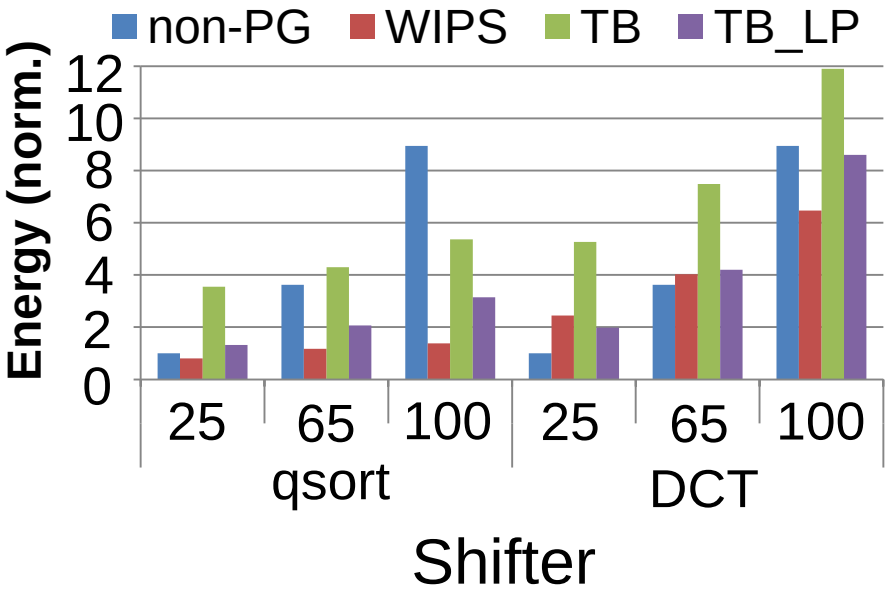
- Time-based (TB) policy [Hu04]
  - Count idle cycles, power gate if the numb. reaches BET
  - Pro: Suppresses ineffective power-off for Short Sleep
  - Con: Requires additional circuits (e.g. counter, controller)
- Whenever-Idle-Put-to-Sleep (WIPS) policy [Seki08]
  - Power off after finishing execution irrespectively of BET
  - Pro: No additional circuits needed
  - Con: Power off even at Short Sleep, wasting energy

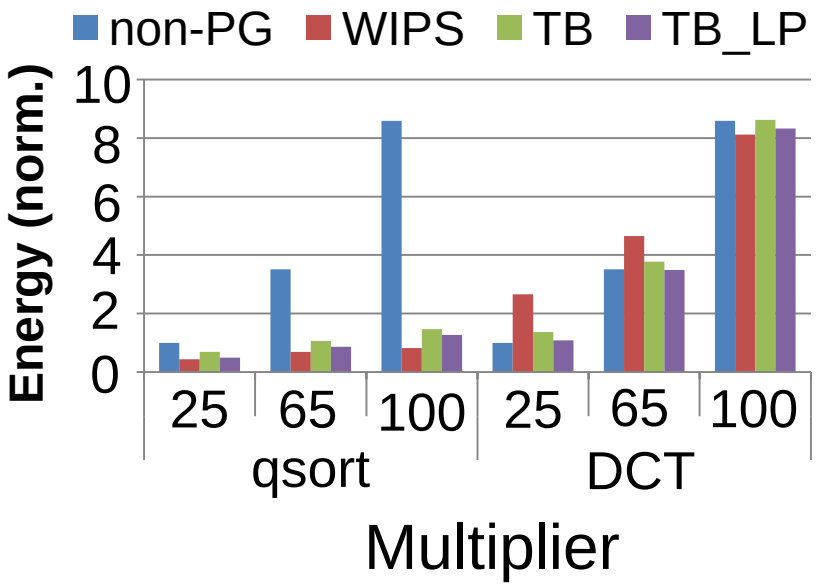
[Hu04] Z. Hu et al., "Microarchitectural techniques for power gating of execution units," ISLPED'04.

[Seki08] N. Seki et al., "A fine grain dynamic sleep control scheme in MIPS R3000," ICCD'08.

Conv. techniques for FGPG (cont.)

- In evaluation of TB policy, energy overhead of control circuit (incl. counter and comparator) has not been discussed so far.
- We designed the control circuit in RTL, synthesized in 65nm commercial lib. and evaluated.



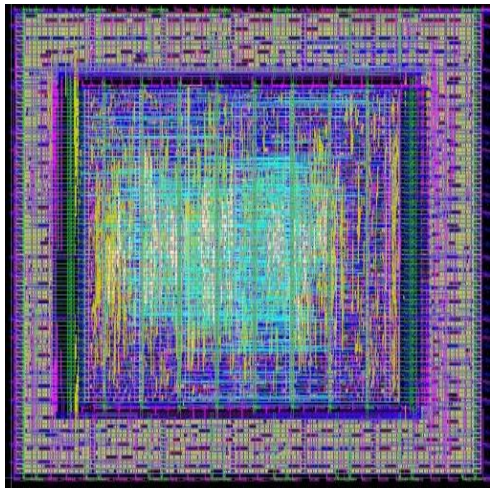


Our Approach

- Propose a control scheme for FGPG
  - to switch "enabling PG" and "disabling PG" depending on temperature and application program
- Key components:
  - Microprocessor with function units for which FGPG can be enabled/disabled by on-chip control registers
  - On-chip leakage monitor to measure temperature-dependent leakage current
  - OS to activate the leakage monitor, reads the result and change the value in the control registers
  - Adaptive WIPS (A-WIPS) sleep policy based on energy characterization and code profiling

Microprocessor with FGPG

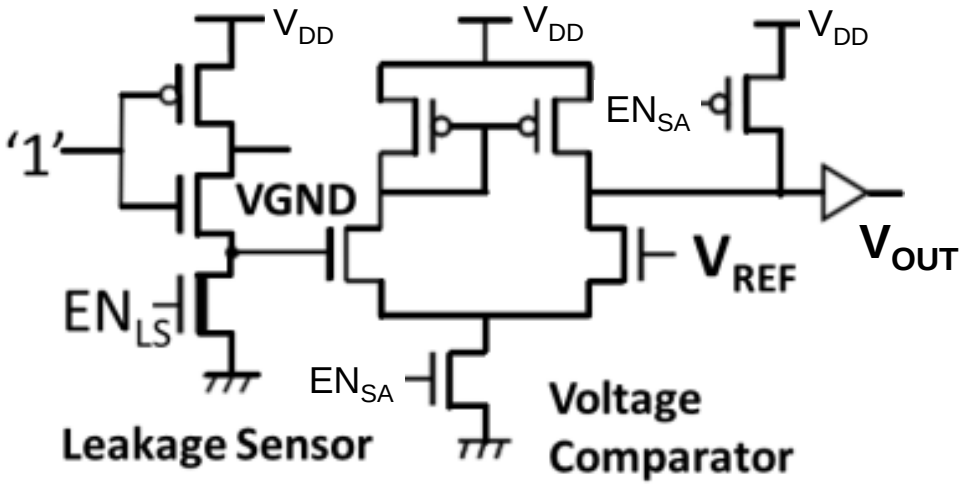
- We designed a microprocessor, Geyser-3
  - based on 32-bit MIPS architecture
  - 5-stage pipeline, 8KB I-cache and 8KB D-cache
  - implemented in Fujitsu 65nm CMOS technology
- Power gated ALU, shifter, multiplier and divider at instruction-by-instruction basis



Layout of power-gated Multiplier

- 3ns wakeup time at 45mV ground bounce
- Unbalanced buffer tree structure to drive the power switches

On-chip leakage monitor circuit



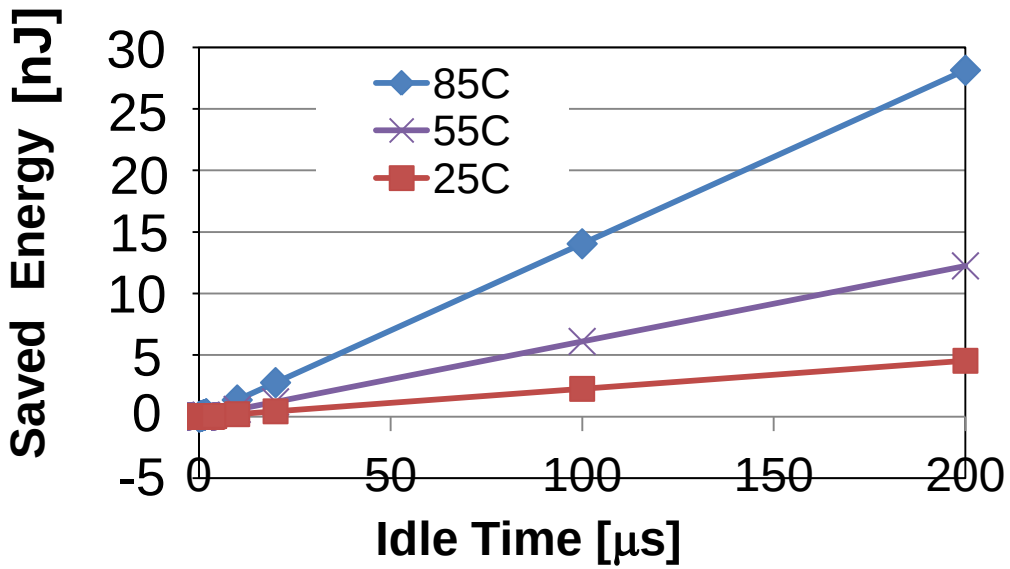
- Use to monitor the temperature
- Circuit structure based on [Koyama08]
- OS activates the monitor and reads the result

[Koyama08] Koyama, Takeda, Usami, "Design and Analysis of On-chip Leakage Monitor using an MTCMOS circuit," ITC-CSCC'08.

Energy Characterization

- Conduct simulations for extracted RC from layout
- Analyze energy dissipation of each function unit at enabling / disabling PG

$$E_{SAVED} = E_{PG\_DISABLED} - E_{PG\_ENABLED}$$

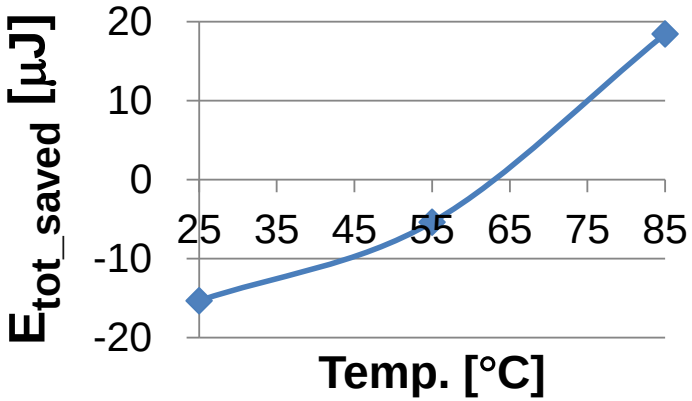


Results for Multiplier

Code Profiling

- For target program, analyze
  - Occurrence of idle events
  - Length of each idle event

  at each function unit



Total saved energy for Multiplier at "matrix"

- Compute total saved energy for target prog. at various temperatures

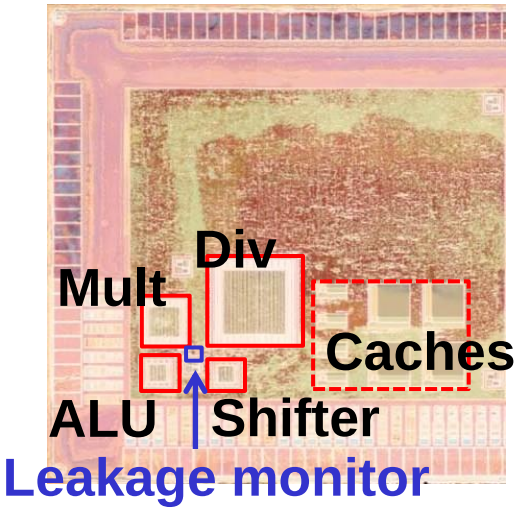
$$E_{tot\_saved} = \Sigma E_{SAVED,\, i} \times n_i$$

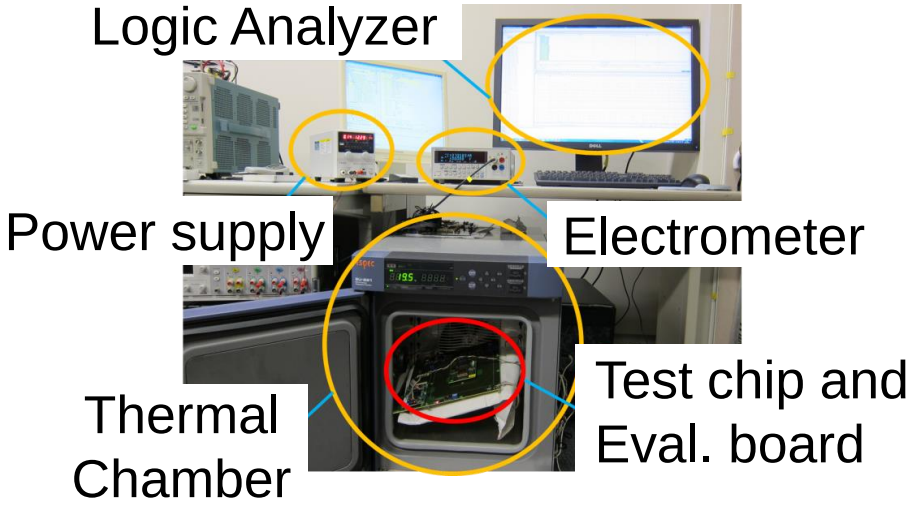
Decisions to enable (E) PG or disable (D) PG

	Shifter					Multiplier				
	mat	qs	Dh	bit	bf	mat	qs	Dh	bit	bf
25°C	D	D	D	D	D	D	E	E	E	E
55°C	D	D	E	D	D	D	E	E	E	E
85°C	D	D	E	D	E	E	E	E	E	E

Experiments

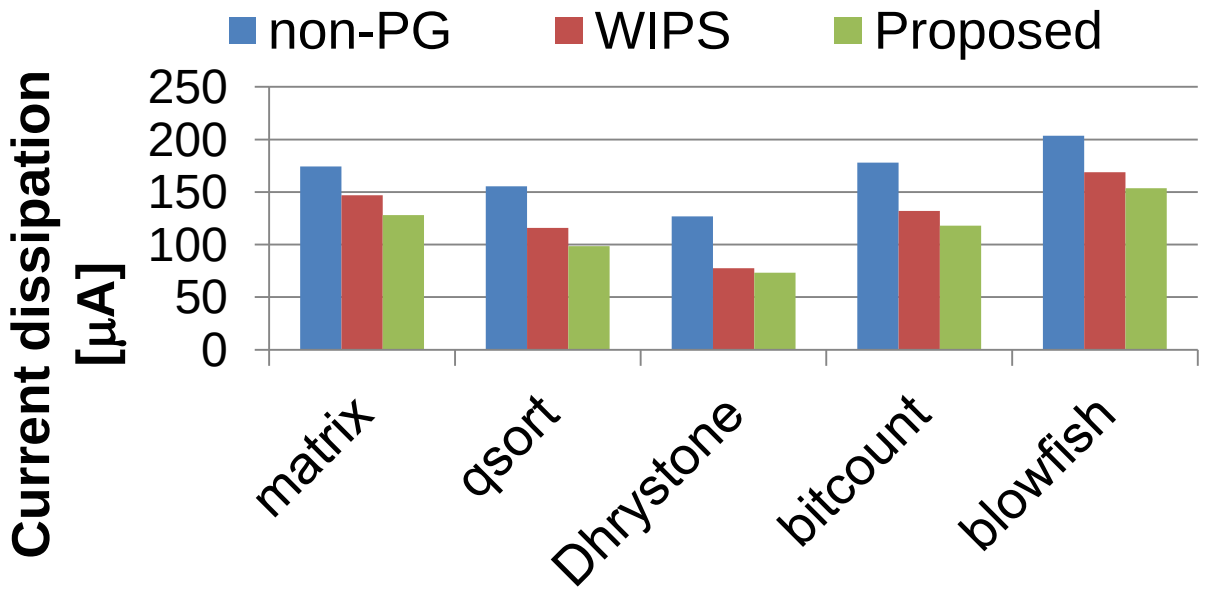
- Fabricated a microprocessor chip Geyser3 in 65nm
- Confirmed that OS activates leakage monitor, reads results, switches control bit to enable/disable PG
- Applied our sleep policy based on energy characterization and code profiling





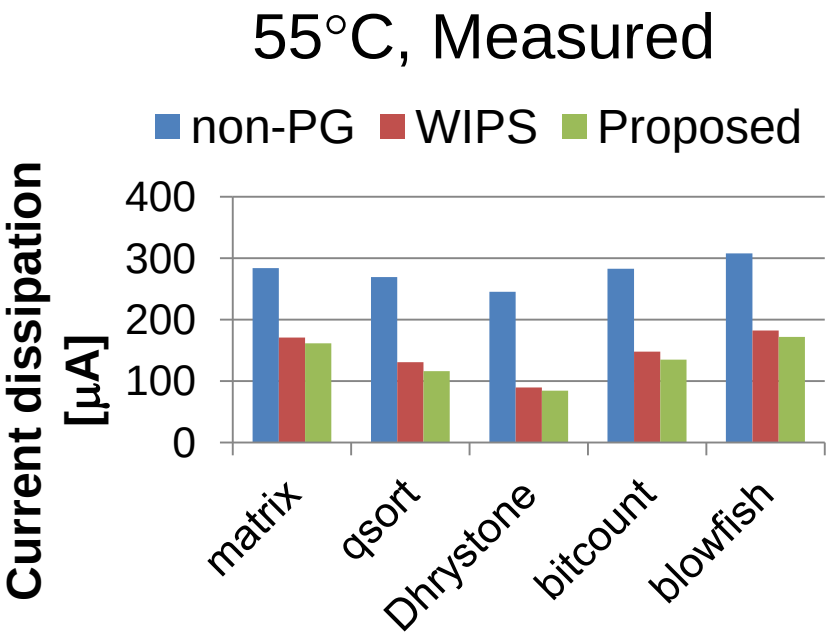
Results

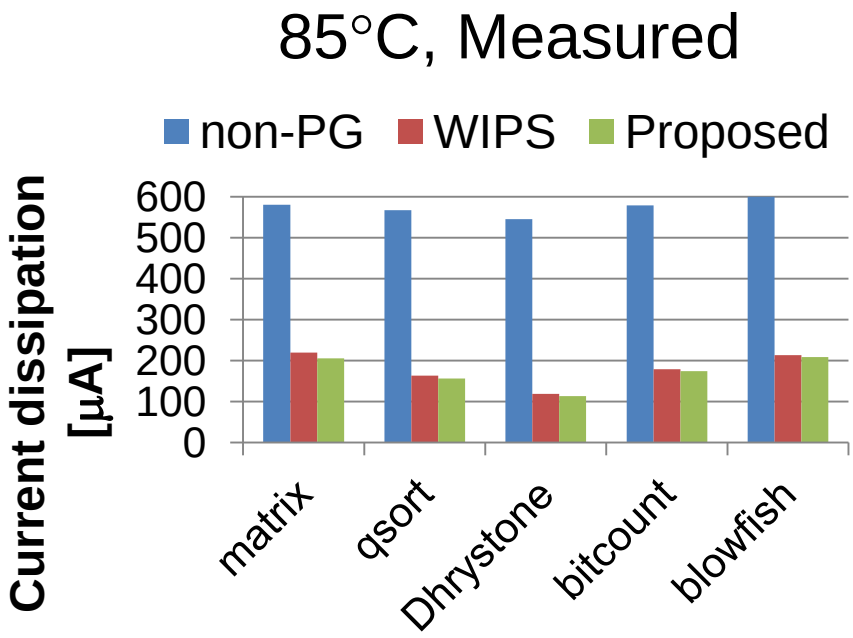
- Executed 5 application programs on Geyser3
- Measured current dissipation of entire function units at 25°C



- Proposed scheme reduces energy dissipation of function units by 5-15% over conv. WIPS

Results (cont.)





- Proposed scheme reduces energy over conv. WIPS both at 55°C and 85°C
- As compared to non-PG, energy dissipation is reduced to 1/3 - 1/5 by our scheme

Conclusions and future work

- Designed and implemented microprocessor whose function units are power gated
- Proposed sleep control scheme for FGPG based on energy characterization and code profiling under the support of OS and leakage monitor
- Measured results demonstrated effectiveness of our approach under temperature variation
- Future work
  - Study the influence of process variation