A Performance Enhanced Dual-switch Network-on-Chip Architecture

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Outline

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- Proposed Method
- Experimental Results
- Conclusion

Introduction

As the technology of semiconductor developed,

Bus-based system is insufficent
- Power Consumption
- Bandwidth Limitation
- Scalability

$\Downarrow$

Packet switch Network-on-Chip
- Low Latency
- High Throughput
- Low power

However, there exist one of major challenges: as the whole network becomes more congested, packets will be blocked more frequently.

Related Work

Various techniques based on additional input buffers were proposed,

- More packets can be transmitted and buffered.
- Power consumption becomes a challenge.
  Input buffer alone consumes almost 46% of the total power of a network.[1]

This research focuses on improving network performance with modest power overhead.

[1] A. K. Kodi, A. Sarathy, A. Louri, 35th ISCA, 2008

Wormhole Flow Control

The merits of wormhole control compared with:

Packet-buffer flow control (cut-through etc.)

- Save buffer size.
- Decrease contention latency.

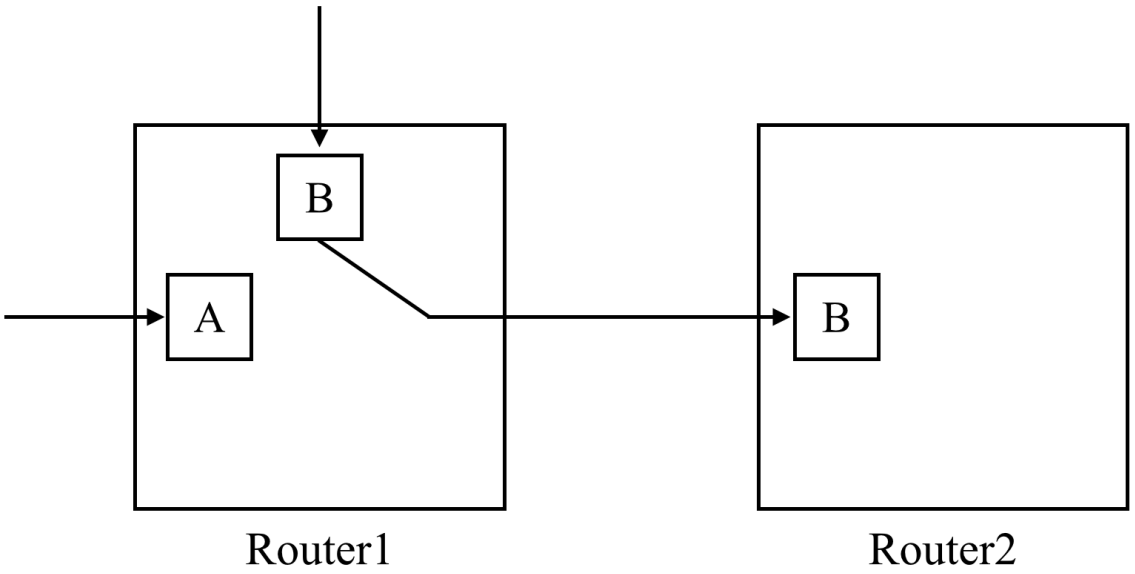
Other flit-buffer flow control (virtual channel)

- Save hardware cost.
- Decrease average latency.

Wormhole Control (cont.)

The drawbacks of wormhole flow control:

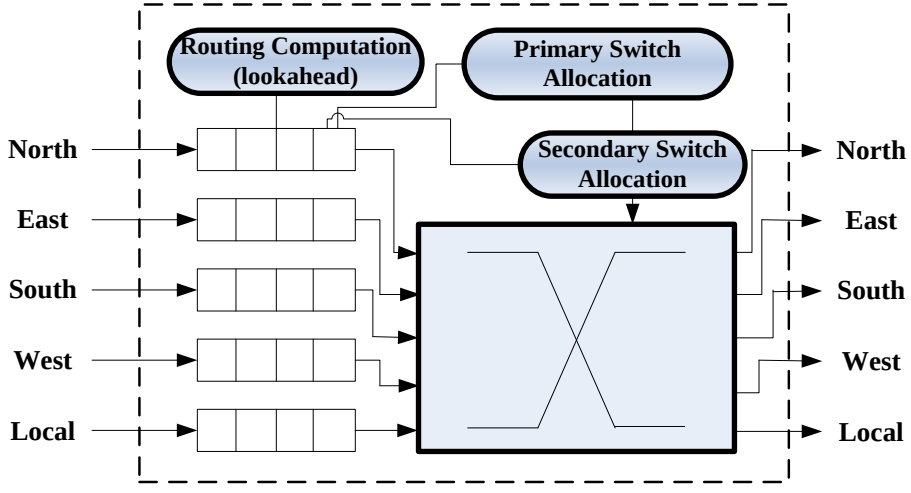
- Packet A and B arrive at same time.
- Both desire the east direction.



Proposed Architecture

A Dual-Switch Allocation (DSA) Architecture is proposed in this research,

- Primary switch allocation (PSA).
- Secondary switch allocation (SSA).
- Lookahead technique in routing computation.

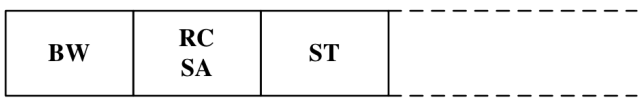


Pipeline Architecture

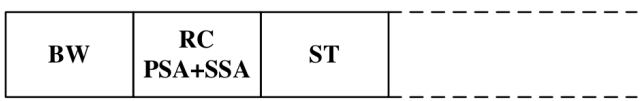
By utilizing lookahead technique, reducing pipeline stages from four to three.

- BW: buffer writing, RC: routing computation, SA: switch allocation and ST: switch traversal.

(a) Basic four-stage pipeline



(b) Lookahead three-stage pipeline



(c) DSA three-stage pipeline

The Delay Through Pipeline Stage

We adopt existing delay model [2] to estimate the delay through pipeline stage.

Router	SA(τ)†	ST(τ)
Baseline(four-stage)	48.04	100
Lookahead(three-stage)	48.04	100
DSA(three-stage)	87.08	100

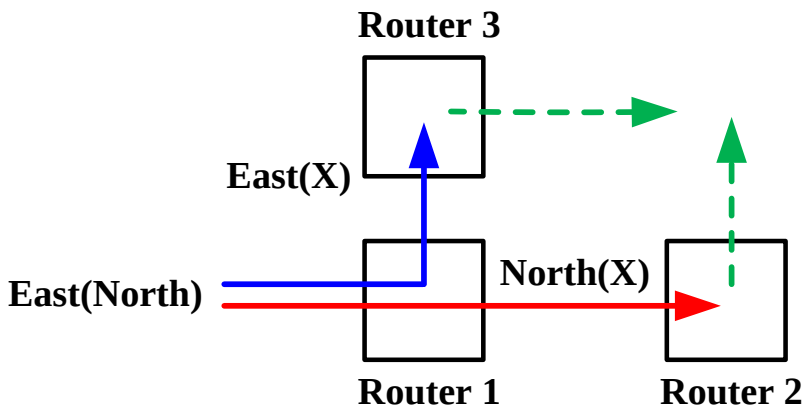
† the delay of an inverter with identical input capacitance.

As a result, the penalty of additional SA in DSA will be hidden in router pipeline.

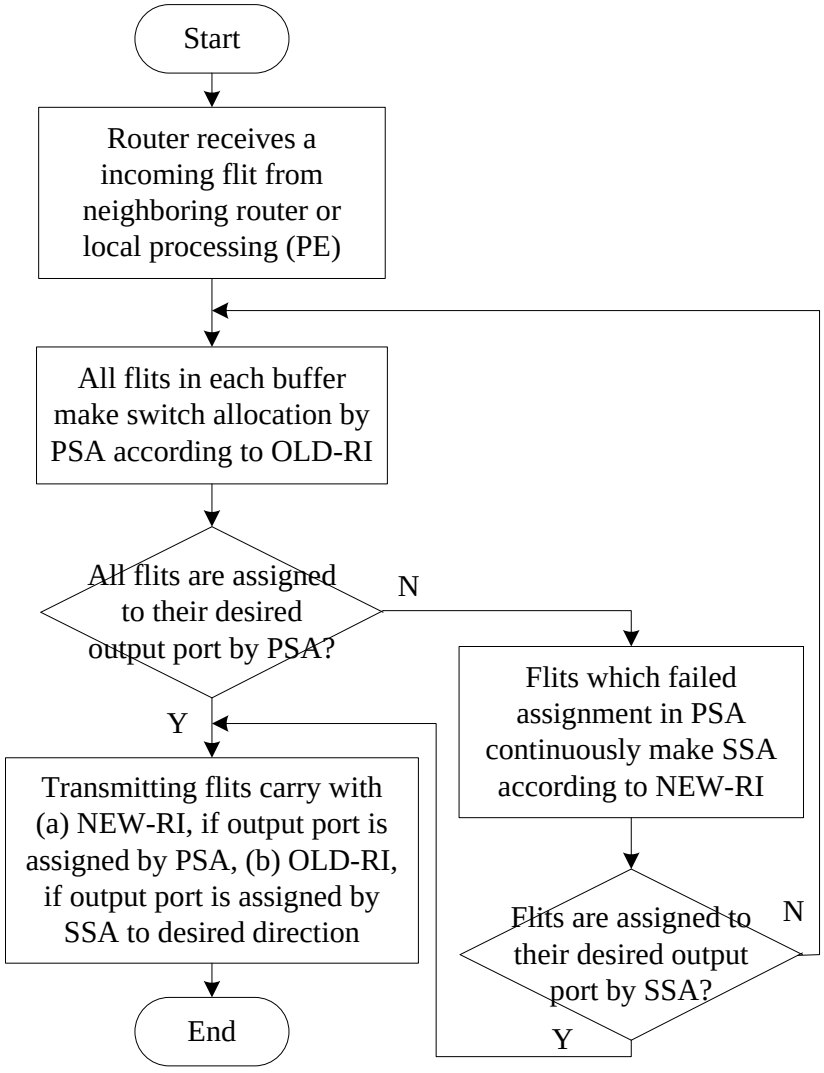
[2] L. S. Peh, W. J. Dally, 7th HPCA, 2001

Method of Dual-Switch Allocation

- Red arrow indicates PSA, blue arrow indicates SSA
- Routing information carried with incoming flit is OLD-RI.
- Routing information calculated by current router is NEW-RI.

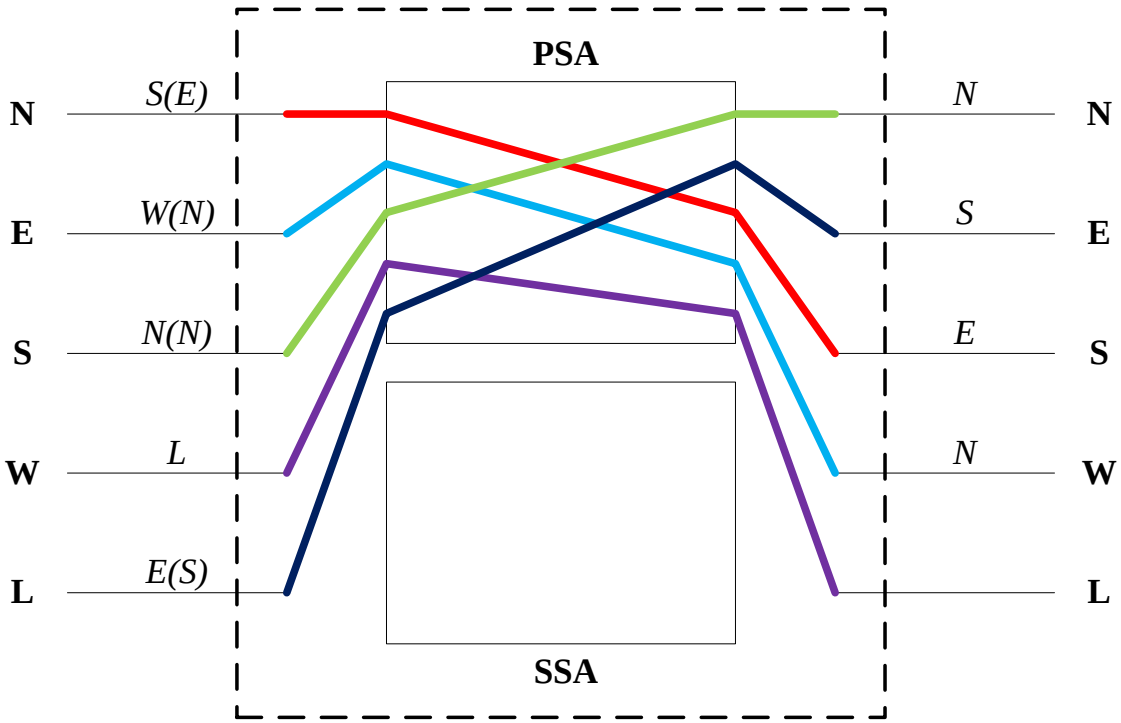


Flowchart of Proposed Method



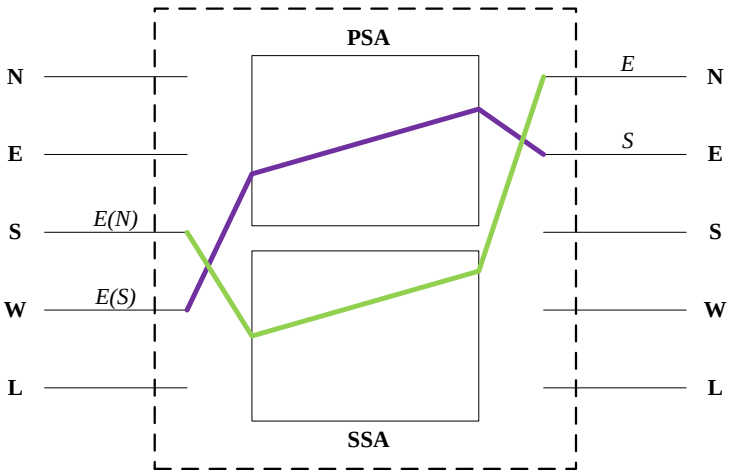
An Example of DSA with No Conflict

- Flits in each input port desire different output ports.
- Local direction always assign in PSA.
- The letter outside bracket is OLD-RI and the letter inside bracket is NEW-RI.

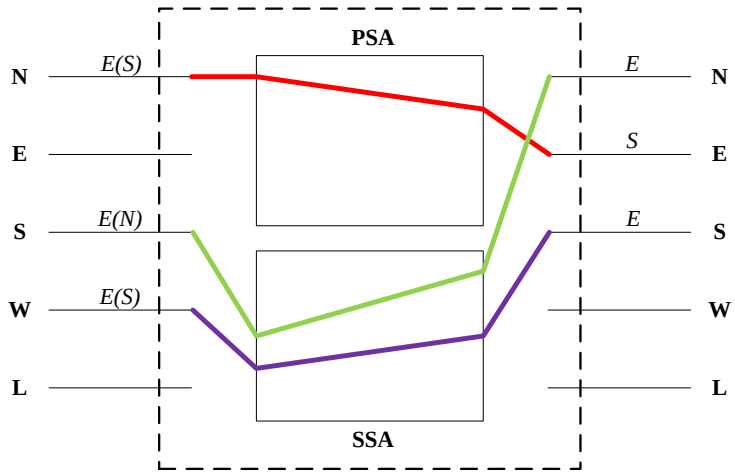


Examples of DSA with Conflict

- Exactly two flits desire the same output.

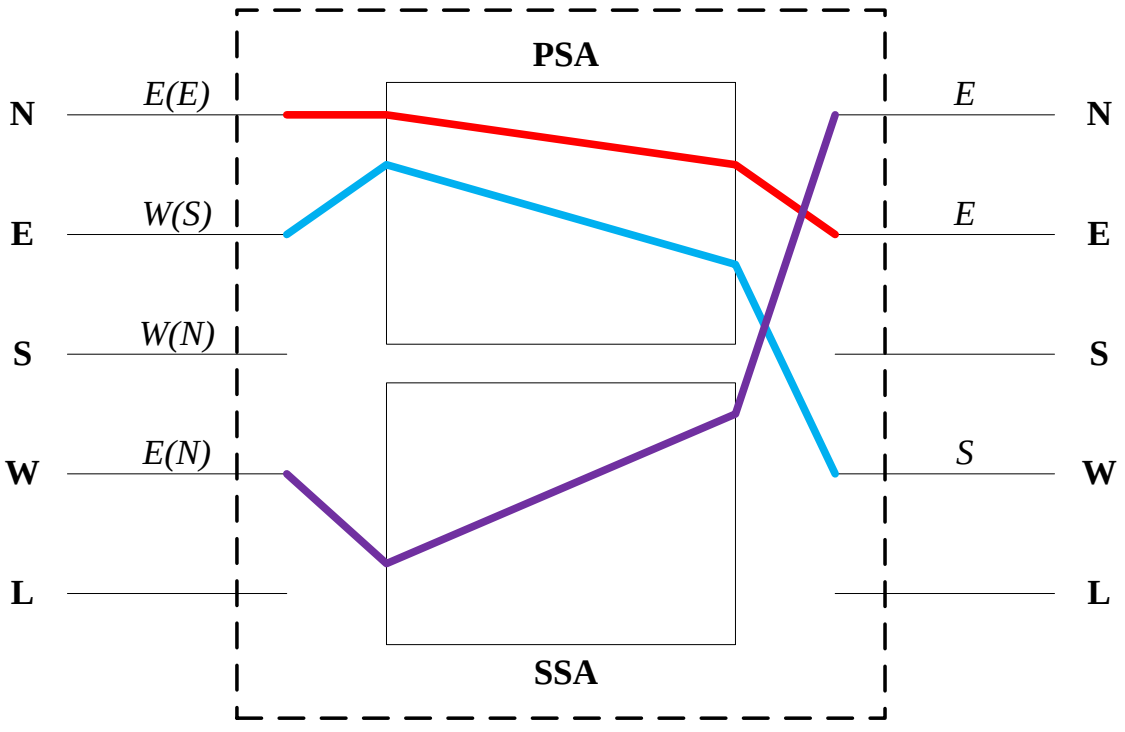


- More than two flits desire the same output.



Examples of Conflict (cont.)

Flit in south input port will fail in PSA and SSA, in this case, flit will wait for next PSA.



Delay Analysis

The average latency of a network can be expressed[3],

$$T_{average} = H_{min} t_{router} + \frac{D_{min}}{v} + \frac{L}{b} + t_{contention}$$

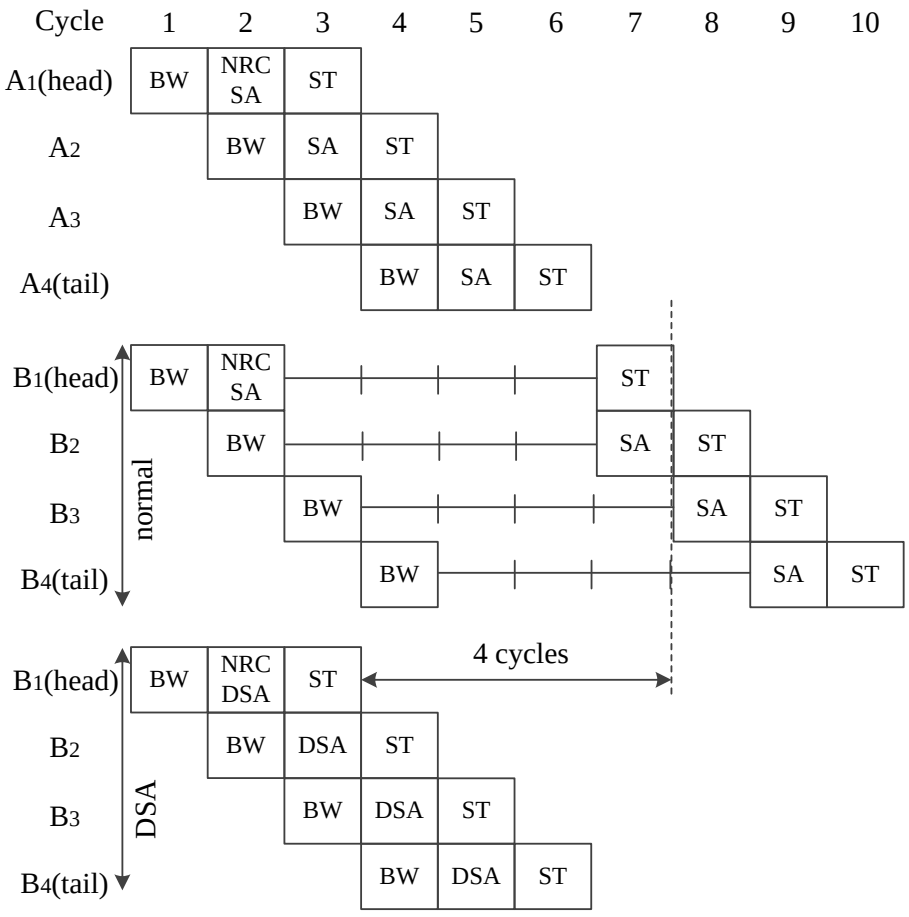
- H_{min} is the average hop counts.
- t_{router} is the delay of a single router.
- D_{min} is an average distance between source and destination, v is a propagation velocity, $\frac{D_{min}}{v}$ is the time spent on the wires.
- L is a packet of length and b is channel bandwidth, $\frac{L}{b}$ is serialization latency.

[3] W. J. Dally, B. Towles, 2004

Delay Analysis (cont.)

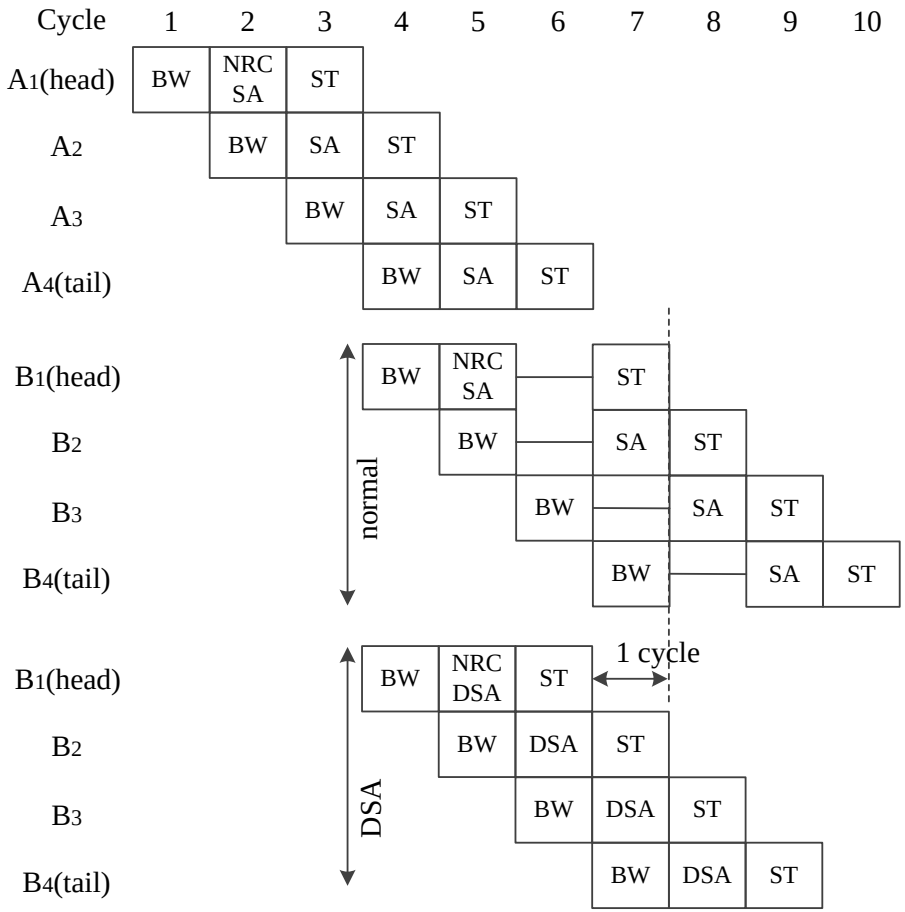
The head flit of packet A and B arrive at the same time.

- NRC: next hop routing computation.



Delay Analysis (cont.)

The tail flit of packet A and the head flit of packet B arrive at the same time.



Experimental Results

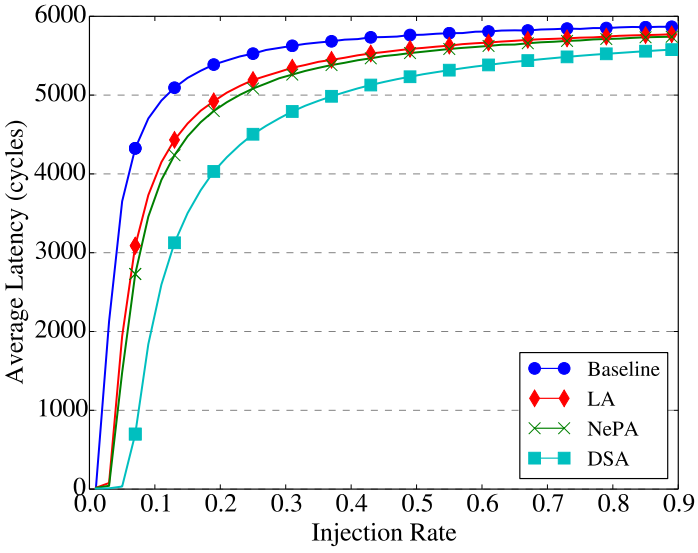
First, we estimate the network performance at Synthetic traffic,

- 8×8 mesh.
- Compared with baseline, lookahead and NePA[4]
- An injection rate consecutive simulation where injection rate varies from 0.01 to 0.90 using random traffic pattern.
- Other different traffic pattern at injection rate 0.5.

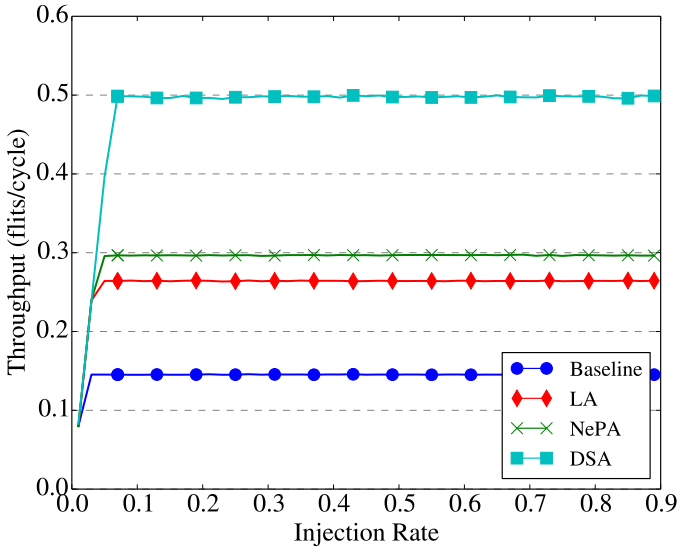
Second, we evaluate the area and power of our proposed router.

[4] J. H. Bahn, S. E. Lee, Y. S. Yang, J. Yang, N. Bagherzadeh, Parallel Processing Letters, 2008

Results of Consecutive Simulation



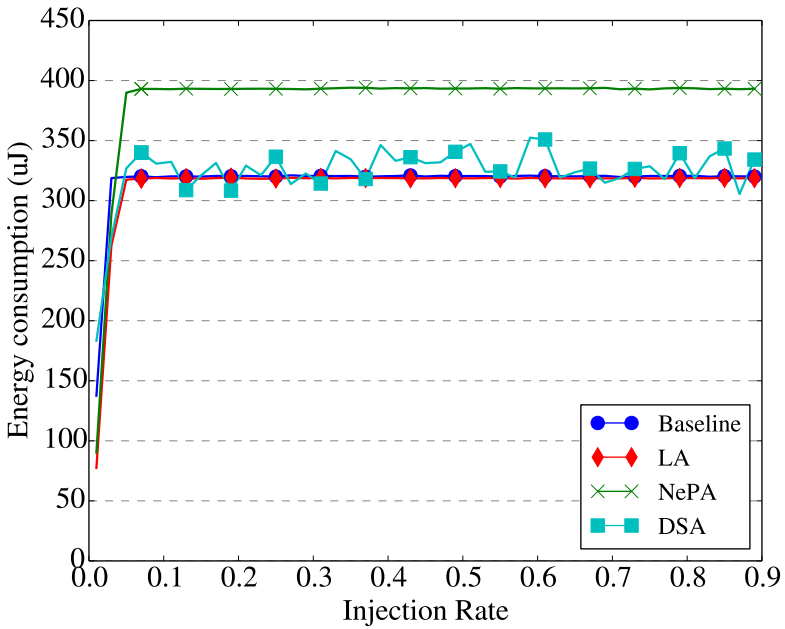
Latency



Throughput

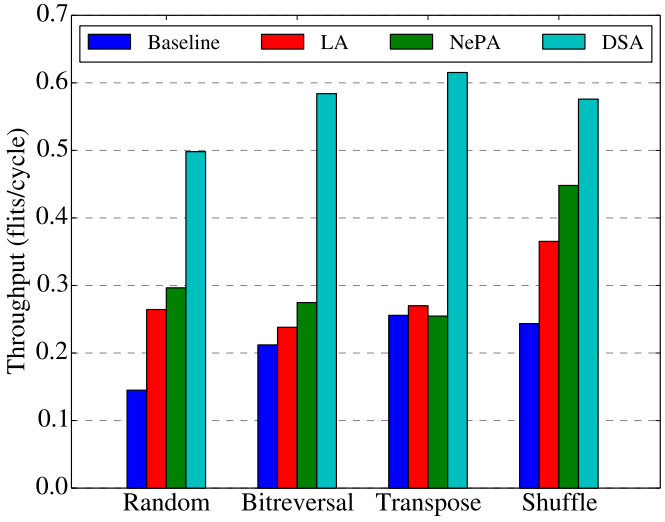
Consecutive Simulation cont.

At low traffic loads, DSA consumes almost same energy with baseline and LA designs, as PSA is utilized more frequently. However, as traffic loads increasing, both PSA and SSA will be used and energy increases.

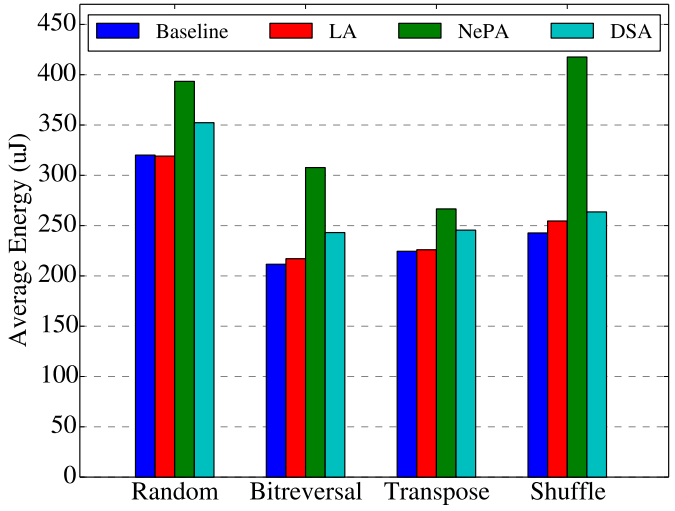


Energy

Other Traffic Patterns Estimation



Throughput



Energy

Router Area and Power

We use Orion 2.0 in 8×8 mesh to estimate router area and power,

- 65nm technology.
- 1GHz and $1\bar{v}$.
- Flit size is 128 bits

Designs	Area (mm^2)	Power ($pJ/flit$)
Baseline	0.3084	245.18
Lookahead (LA)	0.3084	245.07
NePA	0.6016	460.05
DSA	0.3101	245.09 (min) 247.54 (max) 246.31 (average)

Conclusion

A Dual-Switch Allocation (DSA) architecture is proposed, which can utilize idle output port as far as possible to make more packets being buffered and transmitted. Latency and throughput are improved with modest power overhead.

Thank you for your attention.