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Pursuing Excellence

An HDL-Synthesized Gated-Edge-Injection PLL with A Current Output DAC

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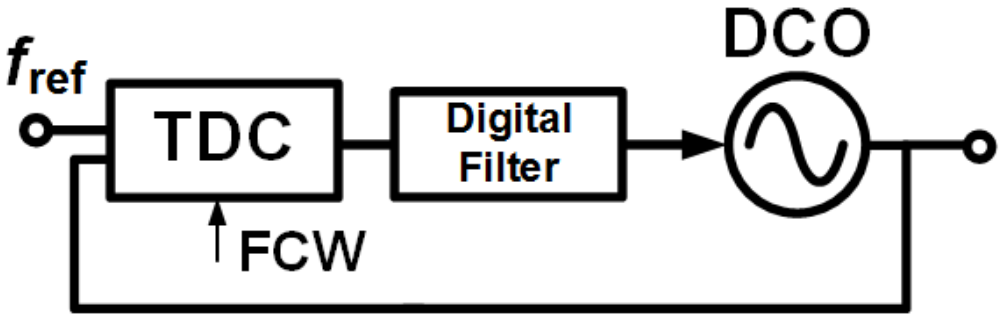
Conventional All-digital PLLs

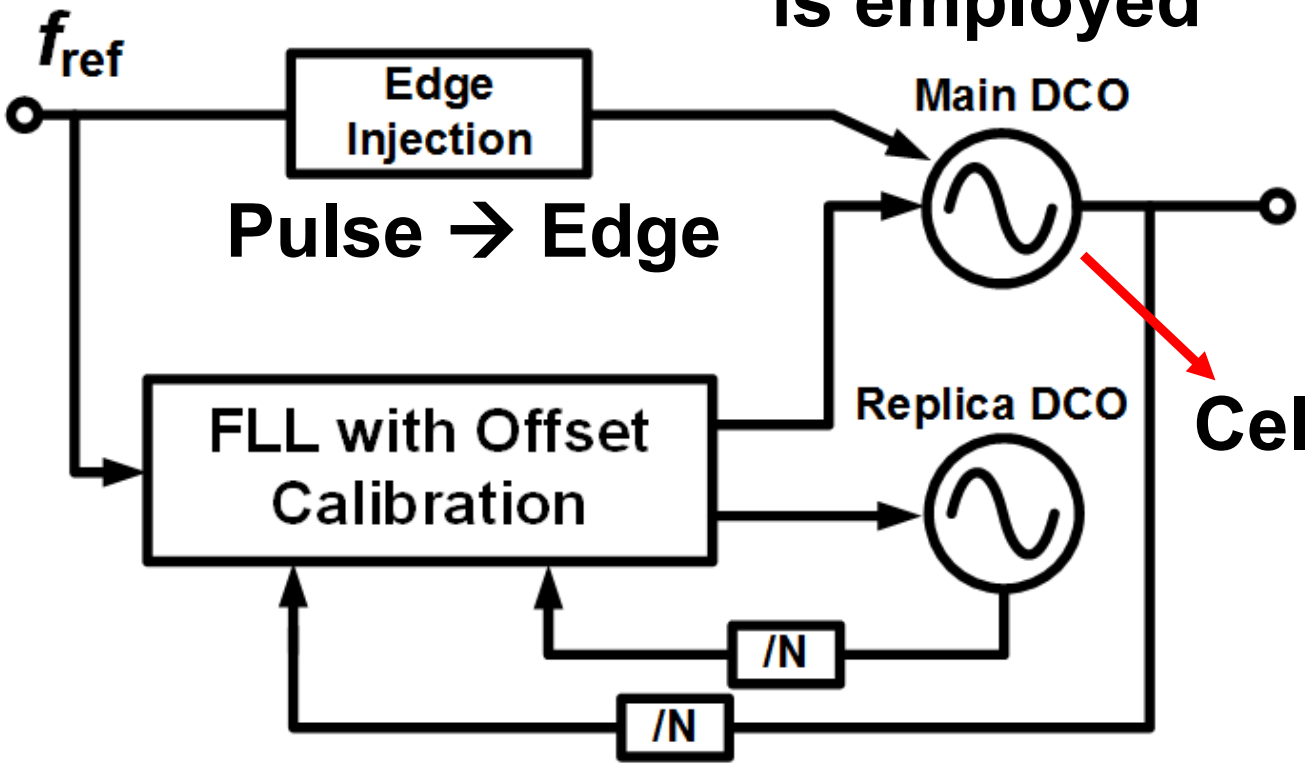
- TDC-based architecture



  - The layout uncertainty degrades TDC and DCO linearity.
- Trade-off between layout area and jitter performance

Proposed IL-based Synthesizable PLL

Injection-Lock (IL) architecture is employed



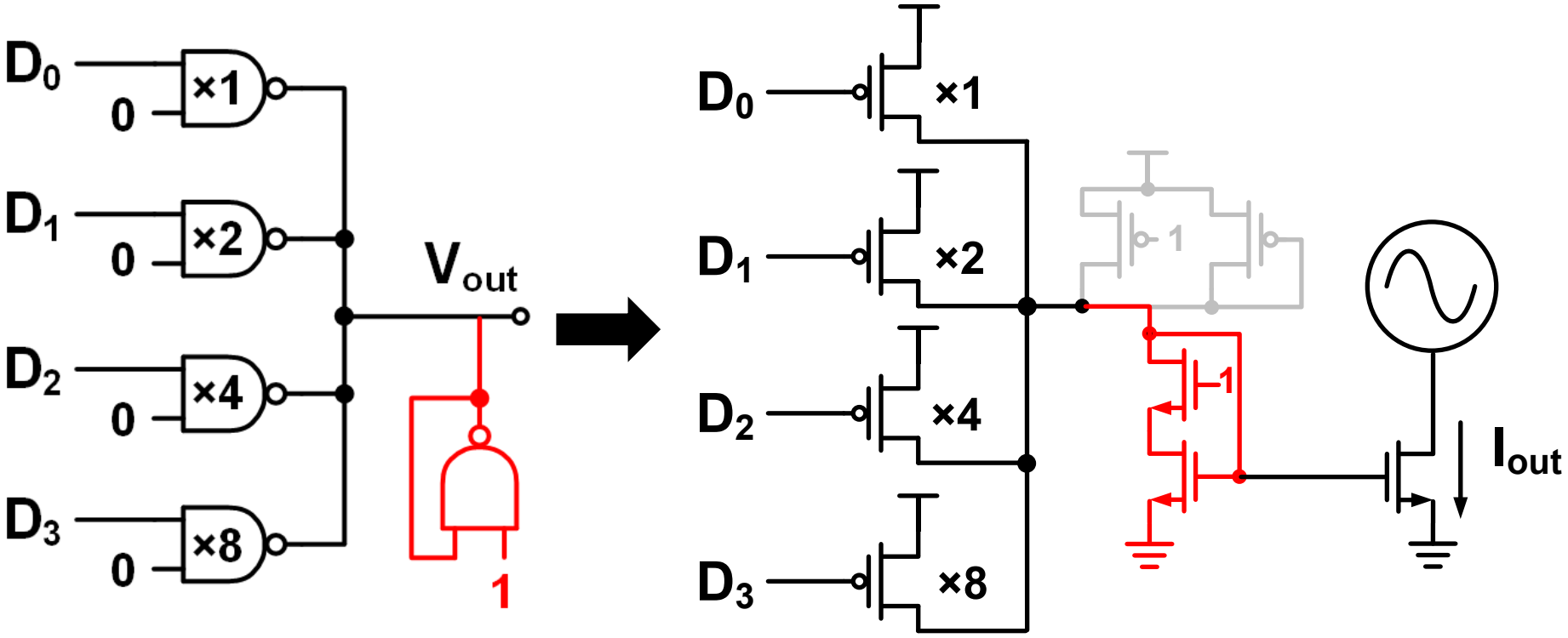
Cell-based I-DAC

Feedback FLL for frequency tracking

Feedforward edge injection for phase locking

[W. Deng, *et al.*, ISSCC 2014]

Proposed Current-linear DAC



- A feedback structure for forming a current mirror.

[W. Deng, *et al.*, ISSCC 2014]

Performance Comparison

	This work 65nm	[1] 28nm	[2] 65nm	[3] 65nm
Power [mW]	0.78 @900MHz	13.7 @2.5GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	0.0066	0.042	0.032	0.1
FOM [dB]	-236.5	-218.6*	-205.5	-214*
W/ custom cells?	No	No	Yes	Yes
Topology	IL-base	TDC-base	TDC-base	TDC-base

*FOM is calculated based on RMS jitter.

The proposed HDL-synthesized PLL can achieve the smallest area with comparable FOM.