1S-10

A Real-time Permutation Entropy Computation for EEG Signals

Xiaowei Ren, Qihang Yu, Badong Chen,
Nanning Zheng and Pengju Ren
E-mail: renxiaowei66@gmail.com

IAIR

西安交通大學
XI'AN JIAOTONG UNIVERSITY

IAIR

Multi-scale Permutation Entropy

Assuming the time series $\{y_t\}_{t=1}^{N}$, we can construct the coarse-grained time series $\{x^{\eta}\}$ with:

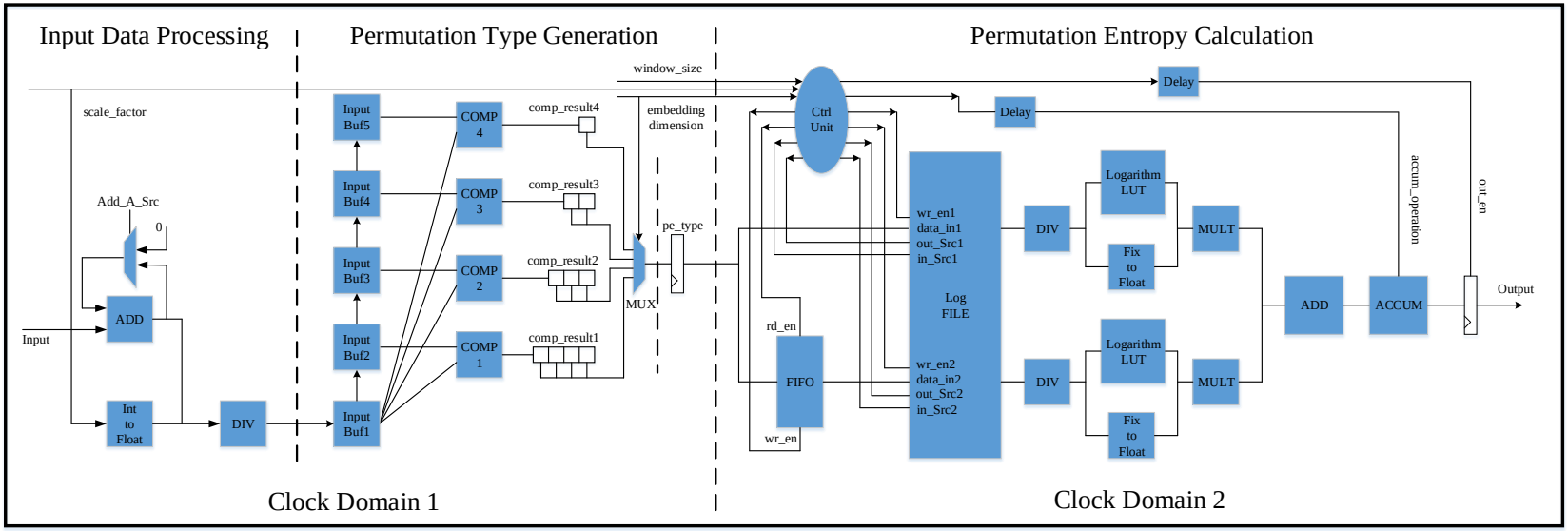
$$x_j^{\eta} = \frac{1}{\eta} \sum_{i=(j-1)\eta+1}^{j\eta} y_i, \qquad 1 \le j \le \frac{N}{\eta}$$

Then, the permutation entropy of $\{x^{\eta}\}$ could be calculated as following:

$$H(n) = -\sum_{i=1}^{n!} p(\pi_i) \log p(\pi_i)$$

$$p(\pi_i) = \frac{\left\| \{t \mid t \le T-n+1, type(X_t^{\eta,n}) = \pi_i\} \right\|}{T-n+1}$$

Microarchitecture of PE



- Could be reconfigured by different input parameters.
- Clock domain 2 is twice faster than clock domain 1.
- Multiple data-paths and pipeline are designed to maximize the parallelism, accelerating the execution speed.

Calculation Error

Window Size	Embedding Dimension	Maximum Error (%)	Average Error (%)
256	3	0.150	0.058
	4	0.256	0.135
	5	0.363	0.206
512	3	0.116	0.063
	4	0.188	0.119
	5	0.231	0.159
1024	3	0.085	0.037
	4	0.115	0.080
	5	0.138	0.093

Speedup versus C

Window Size	Embedding Dimension	FPGA (us)	C (ms)	Average Speedup
256	3	28.230	97.518	3454
	4	28.230	104.299	3695
	5	28.230	115.584	4094
512	3	28.230	91.523	3242
	4	28.230	98.023	3472
	5	28.230	105.304	3730
1024	3	28.230	74.879	2652
	4	28.230	82.096	2908
	5	28.230	87.658	3105

Hardware Cost

Resources	Utilized	Available	Utilization Rate (%)
Flip Flop	461184	2443200	18.88
LUT	454656	1221600	37.22
Memory LUT	1280	344800	0.37
I/O	67	1200	5.58
Block RAM	640	1292	49.54
DSP48	1280	2160	59.26
BUFG	3	128	2.34
MMCM	1	24	4.17