A High Efficient Hardware Architecture for Multiview 3DTV

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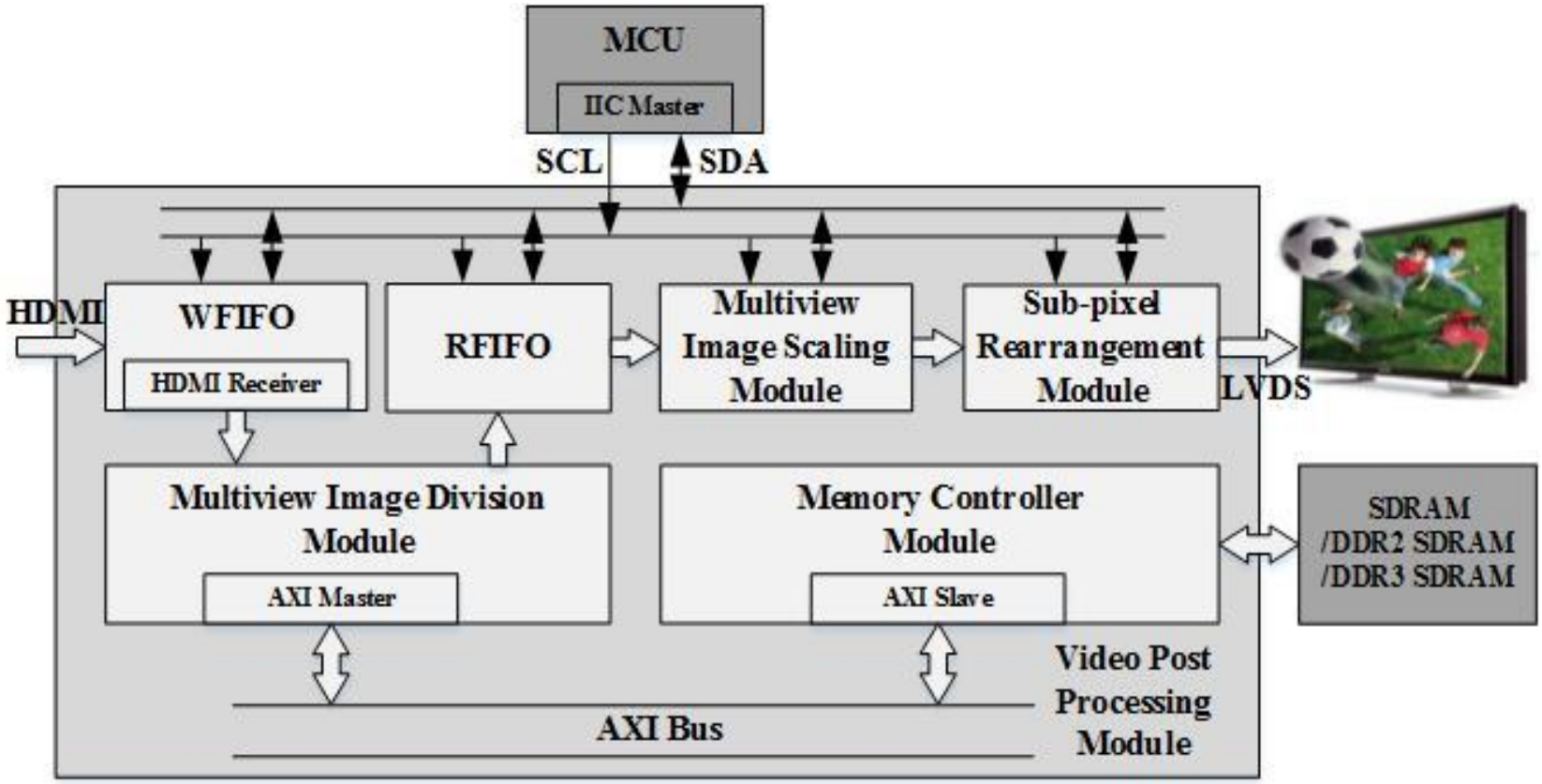
The overall system architecture



Data Storage Strategy in SDRAM

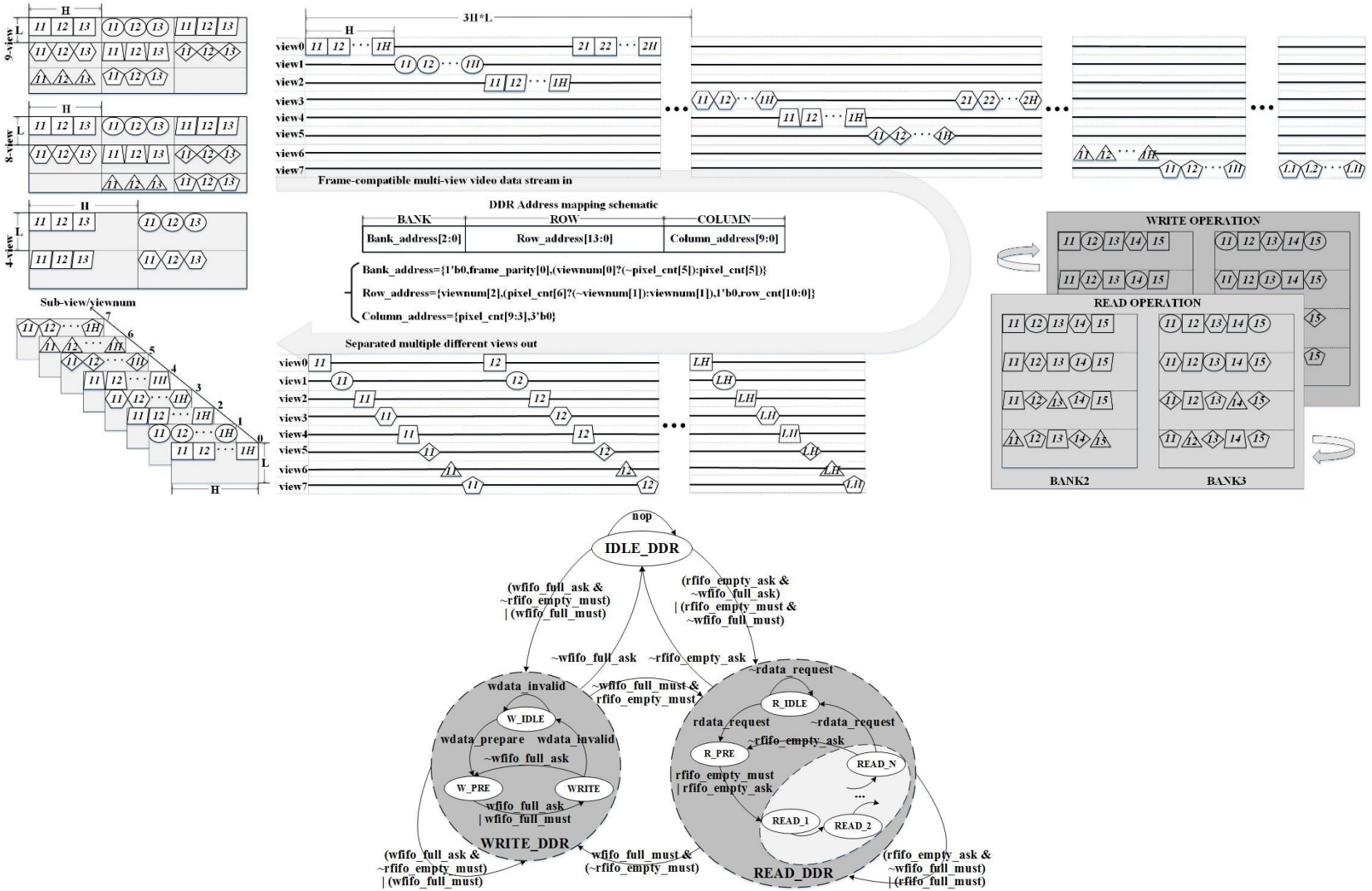
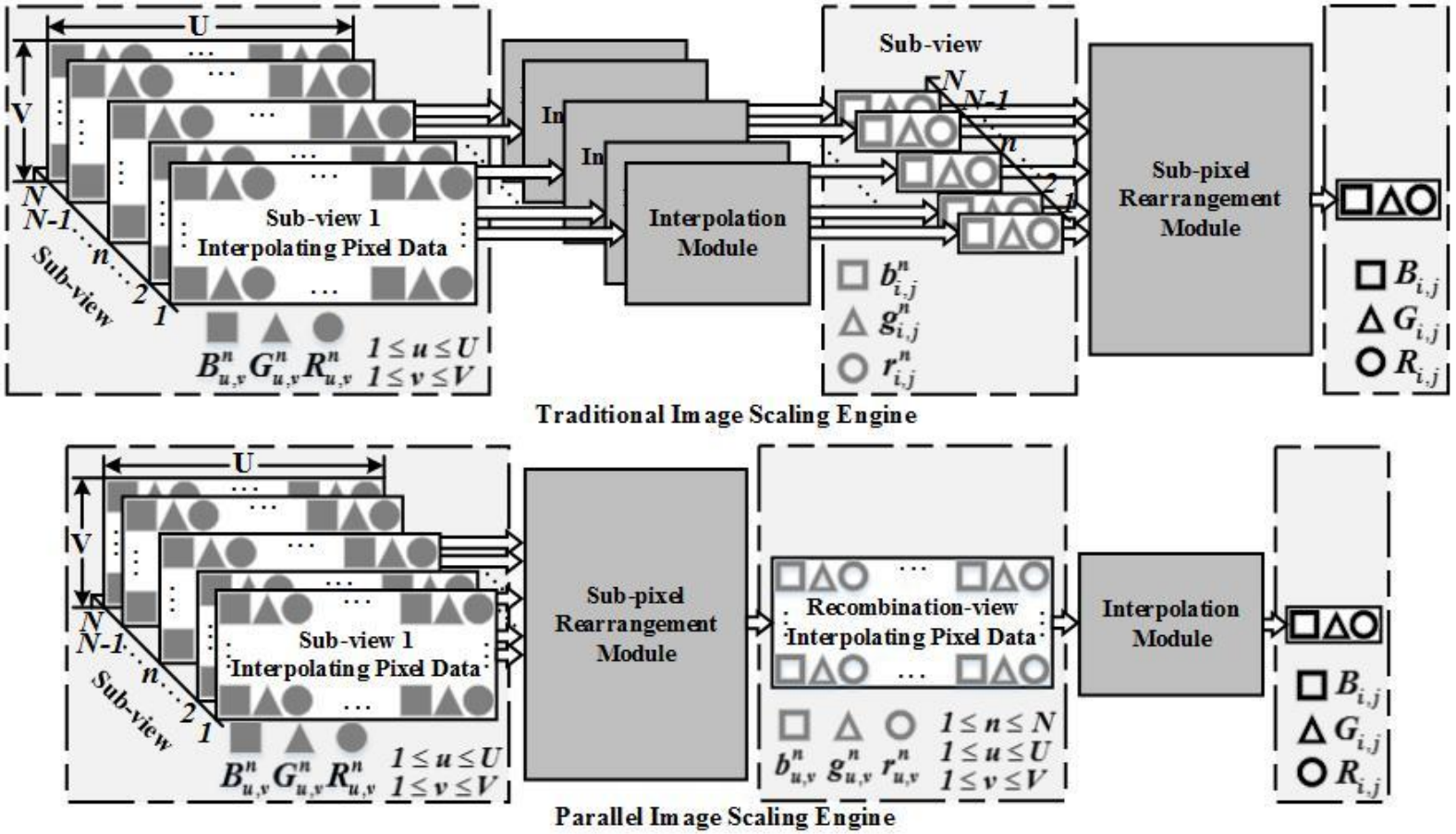


Image Scaling Engine



$$\mathbf{R}_{i,j} = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{r,n} \times \mathbf{r}_{i,j}^{n}) = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{r,n} \times (\sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \mathbf{R}_{u,v}^{n})) = \sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{r,n} \times \mathbf{R}_{u,v}^{n}))$$

$$\mathbf{G}_{i,j} = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{g,n} \times \mathbf{g}_{i,j}^{n}) = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{g,n} \times (\sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \mathbf{G}_{u,v}^{n})) = \sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{g,n} \times \mathbf{G}_{u,v}^{n}))$$

$$\mathbf{B}_{i,j} = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{b,n} \times \mathbf{b}_{i,j}^{n}) = \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{b,n} \times (\sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \mathbf{B}_{u,v}^{n})) = \sum_{u=1}^{U}\sum_{v=1}^{V}(\mathbf{P}_{u,v}^{i,j} \times \sum_{n=1}^{N}(\mathbf{F}_{i,j}^{b,n} \times \mathbf{B}_{u,v}^{n}))$$

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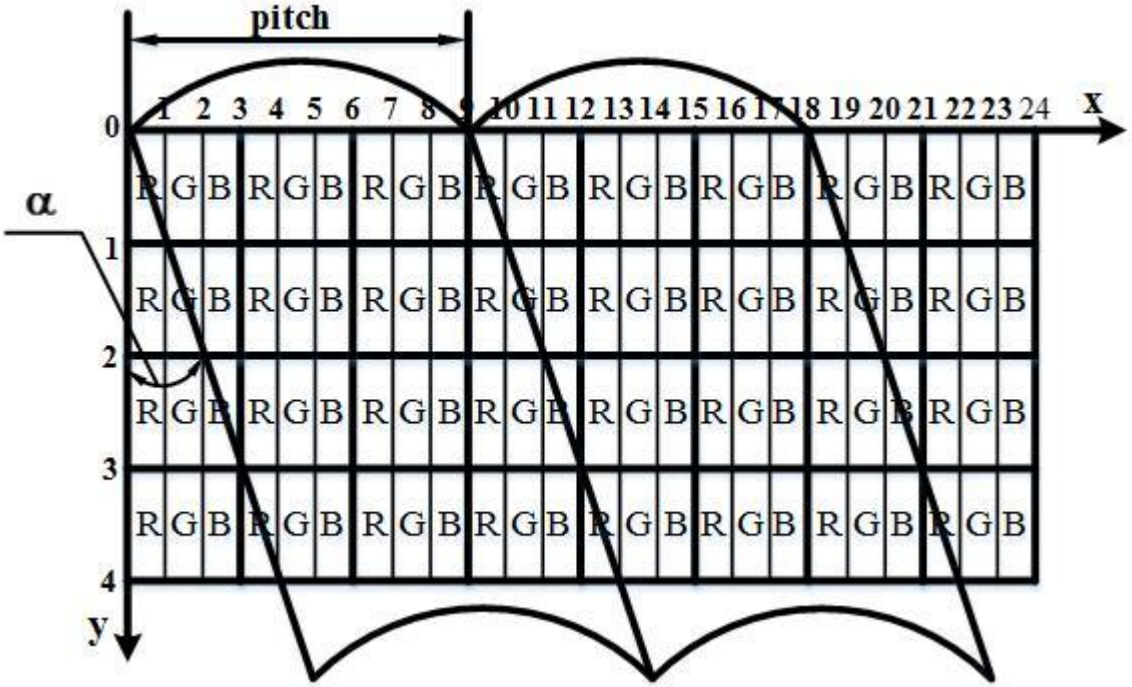
Float-point Sub-pixel Rearrangement



$$N(x,y) = \frac{(x - x_{off} - 3y \times \tan\alpha)\%pitch}{pitch} \times N_{tot} \quad (1)$$

$$T(x,y) = (x - x_{off} - 3y \times \tan\alpha)\%pitch \quad (2)$$

$$N(x,y) = T(x,y) / pitch \times N_{tot} \quad (3)$$

$$T(x+3,y) = (T(x,y) + 3\%pitch)\%pitch \quad (4)$$

$$T(x,y+1) = (T(x,y) - (3\tan\alpha)\%pitch)\%pitch \quad (5)$$

The experimental results

DEVICE UTILIZATION

Slice Logic	Used	Available	Utilization
Slice Registers	115,486	207,360	55%
Slice LUTs	107,955	207,360	52%
Occupied Slices	39,740	51,840	76%
BlockRAM/FIFO	69	288	23%