Design and Analysis for ThruChip Design for Manufacturing (DFM)

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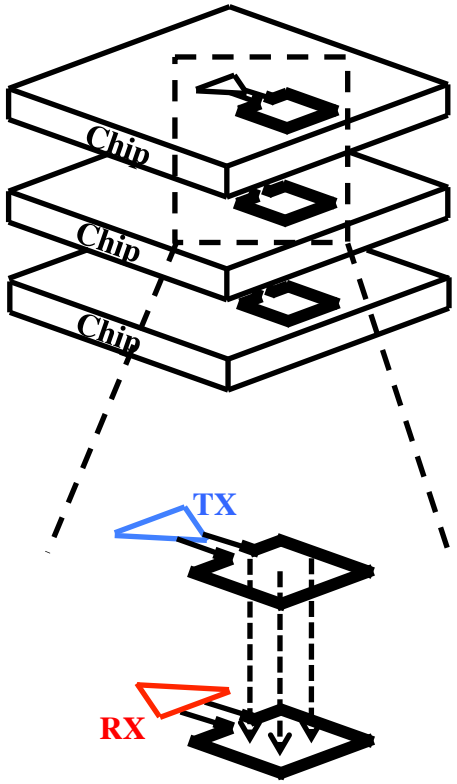
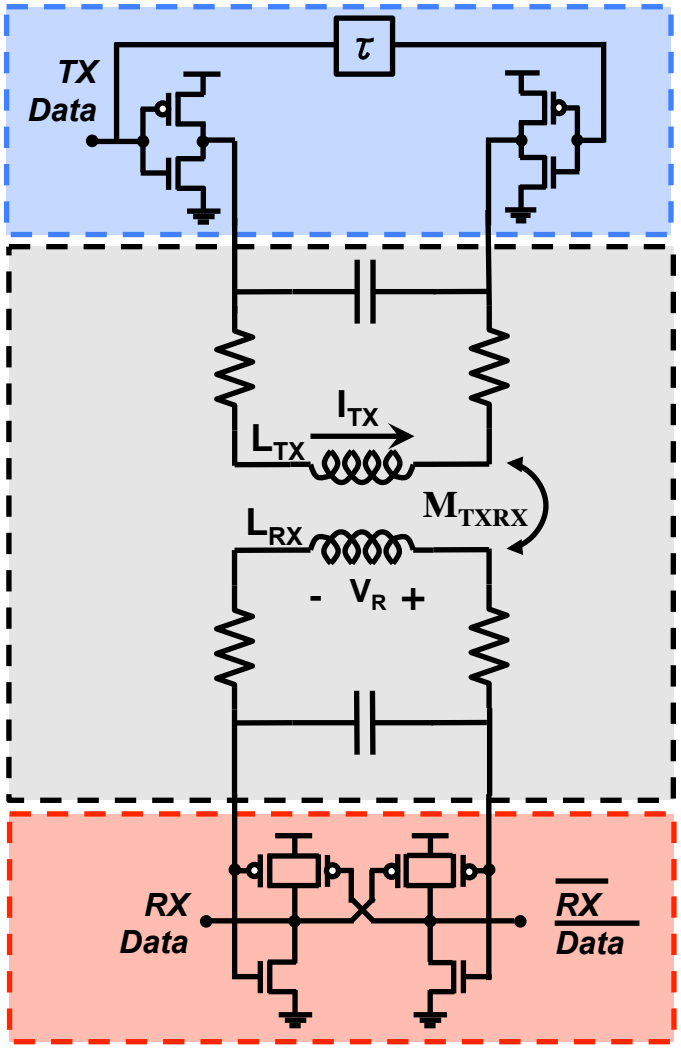
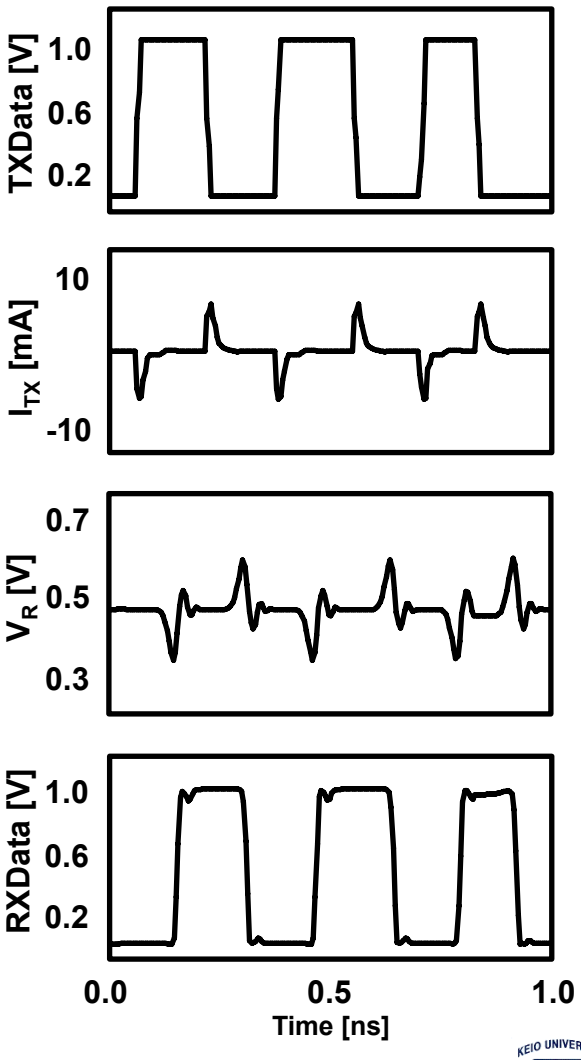
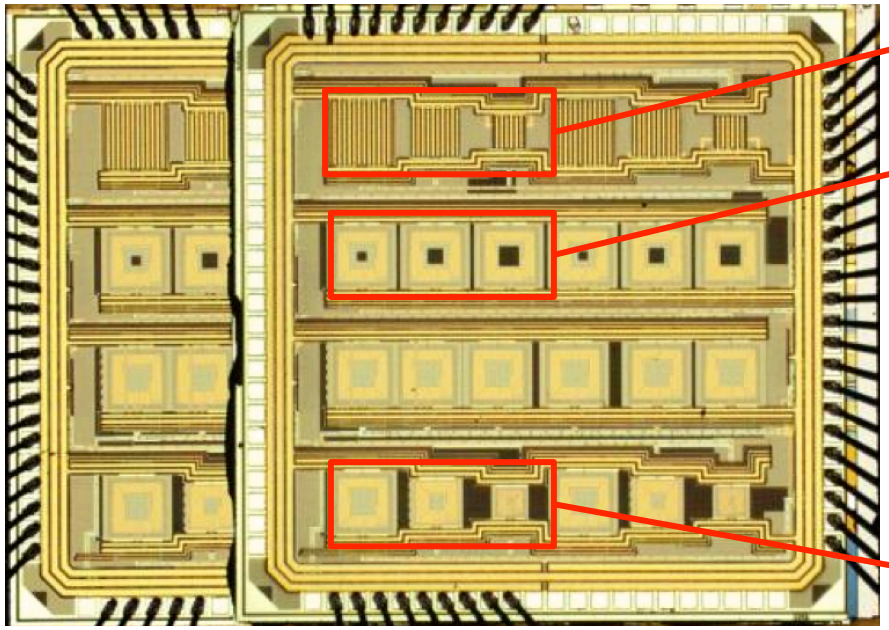
Background - What is ThruChip Interface (TCI)?







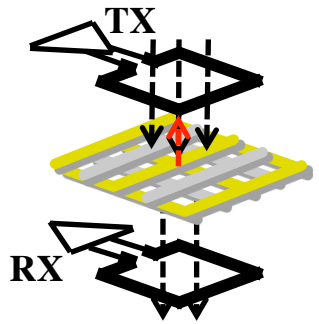
Test Chip Configuration for Exploring DFM Rules

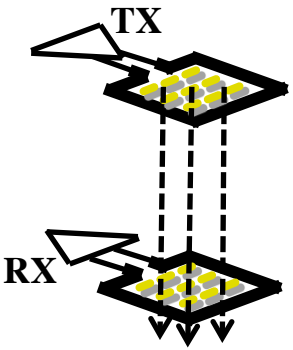


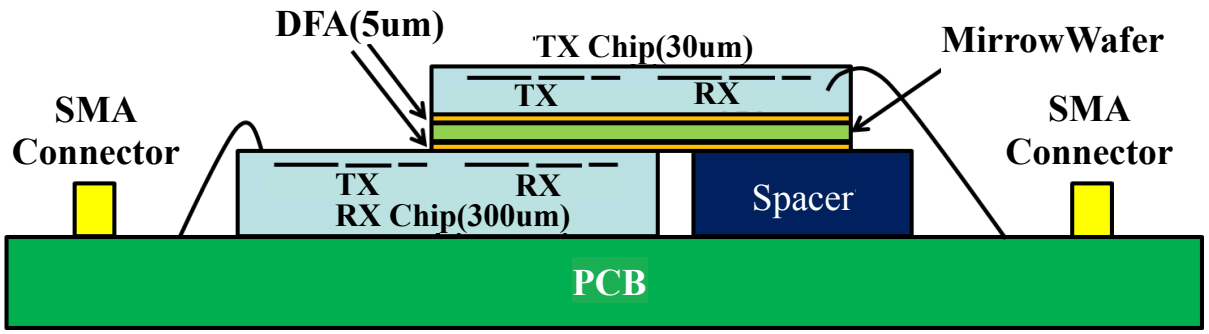
Power mesh

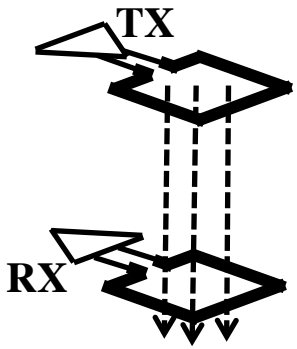
Dummy Metal Fills

Baseline coils

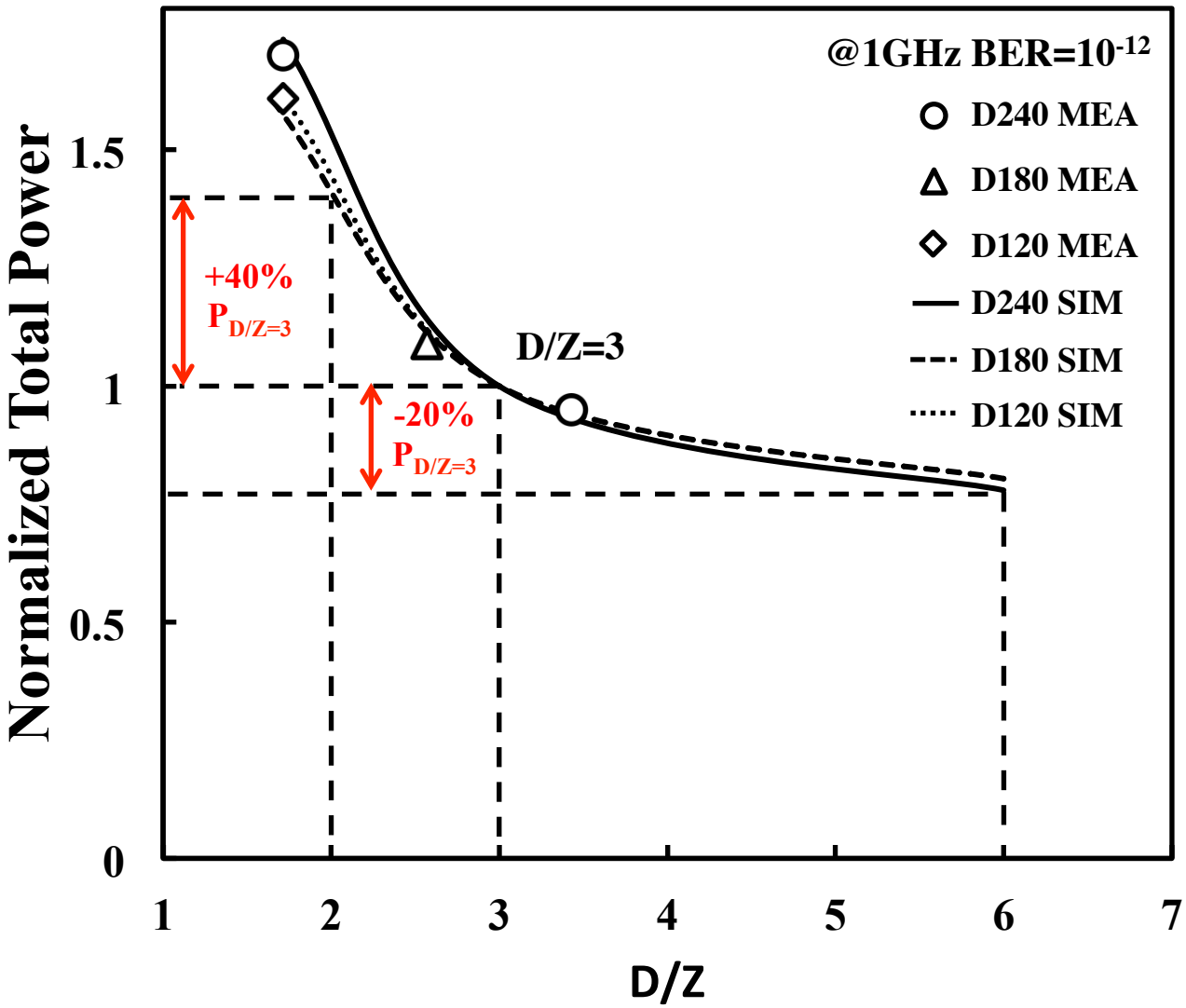


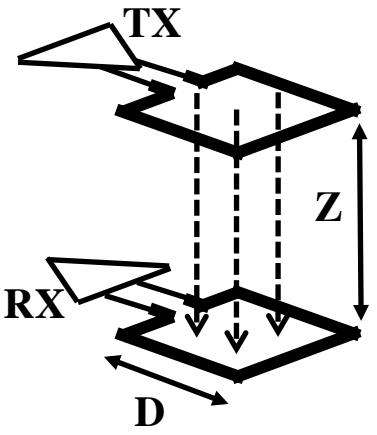






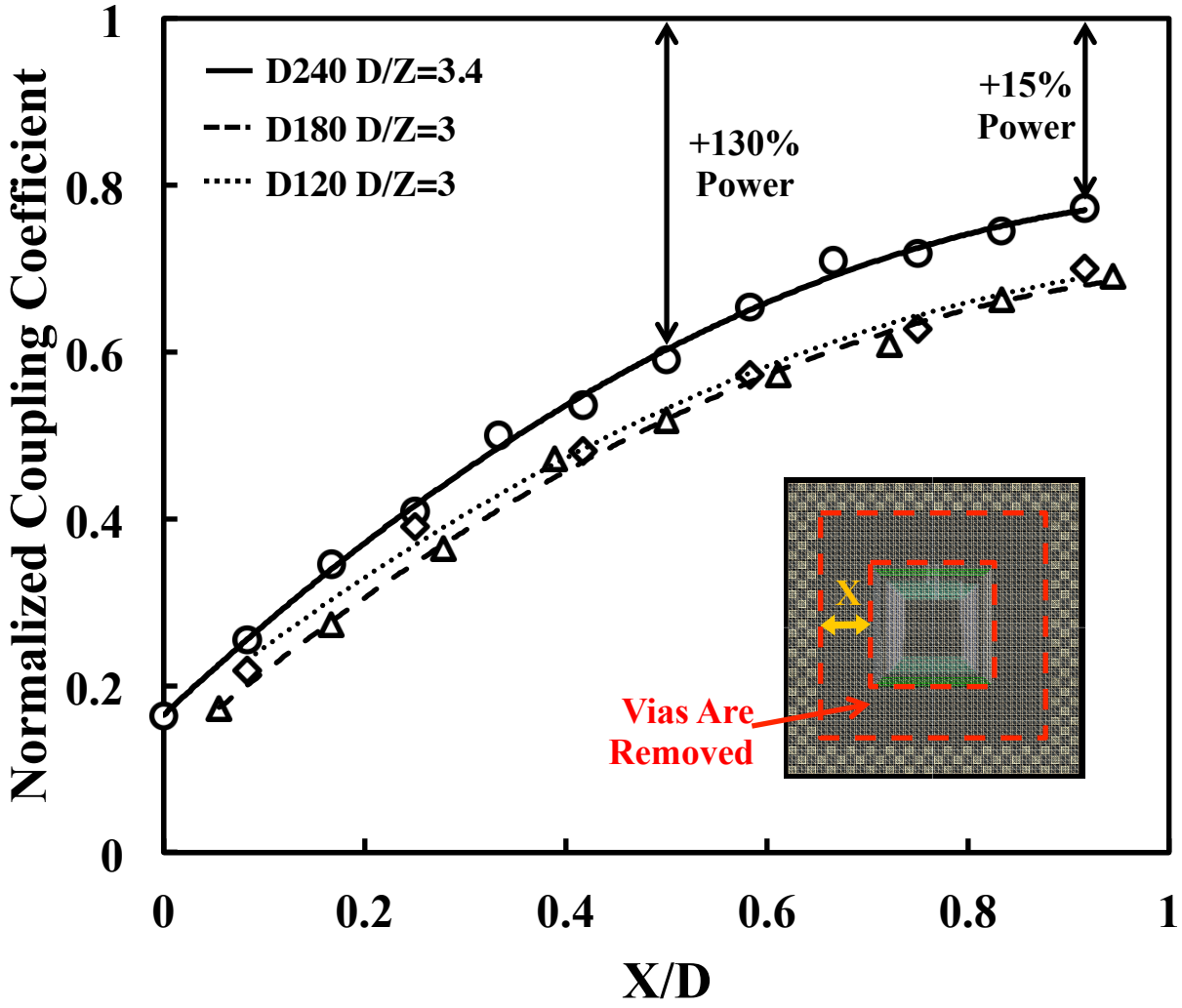
Total Power vs. D/Z

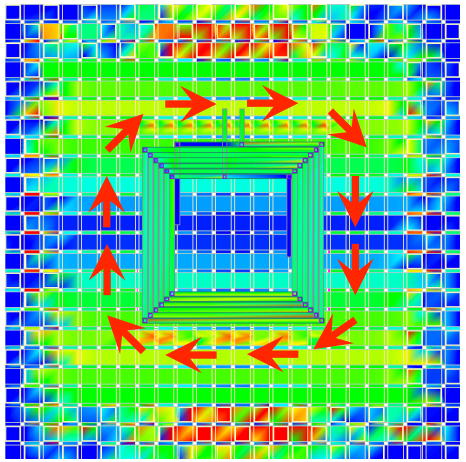




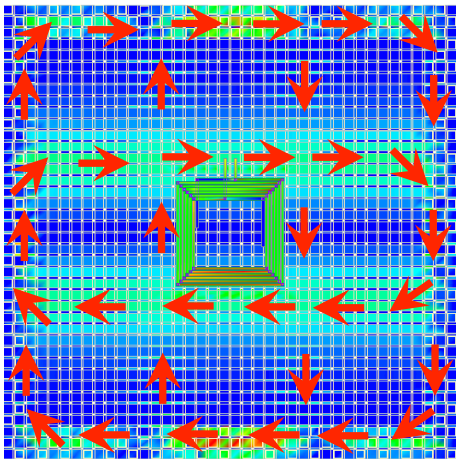
- Enlarging coil size or thinning wafer thickness can further reduce power
- D/Z<2 will become less power efficient and less reliable

Power Mesh Impact





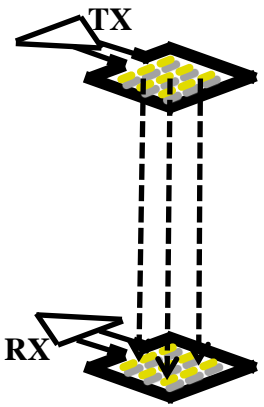
X/D=0.25

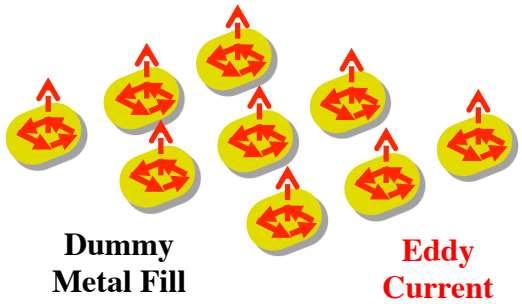


X/D=0.92

*Eddy current is induced on power mesh and may cause TCI to fail

Dummy Metal Impact





*Dummy metal fills have no impact on TCI