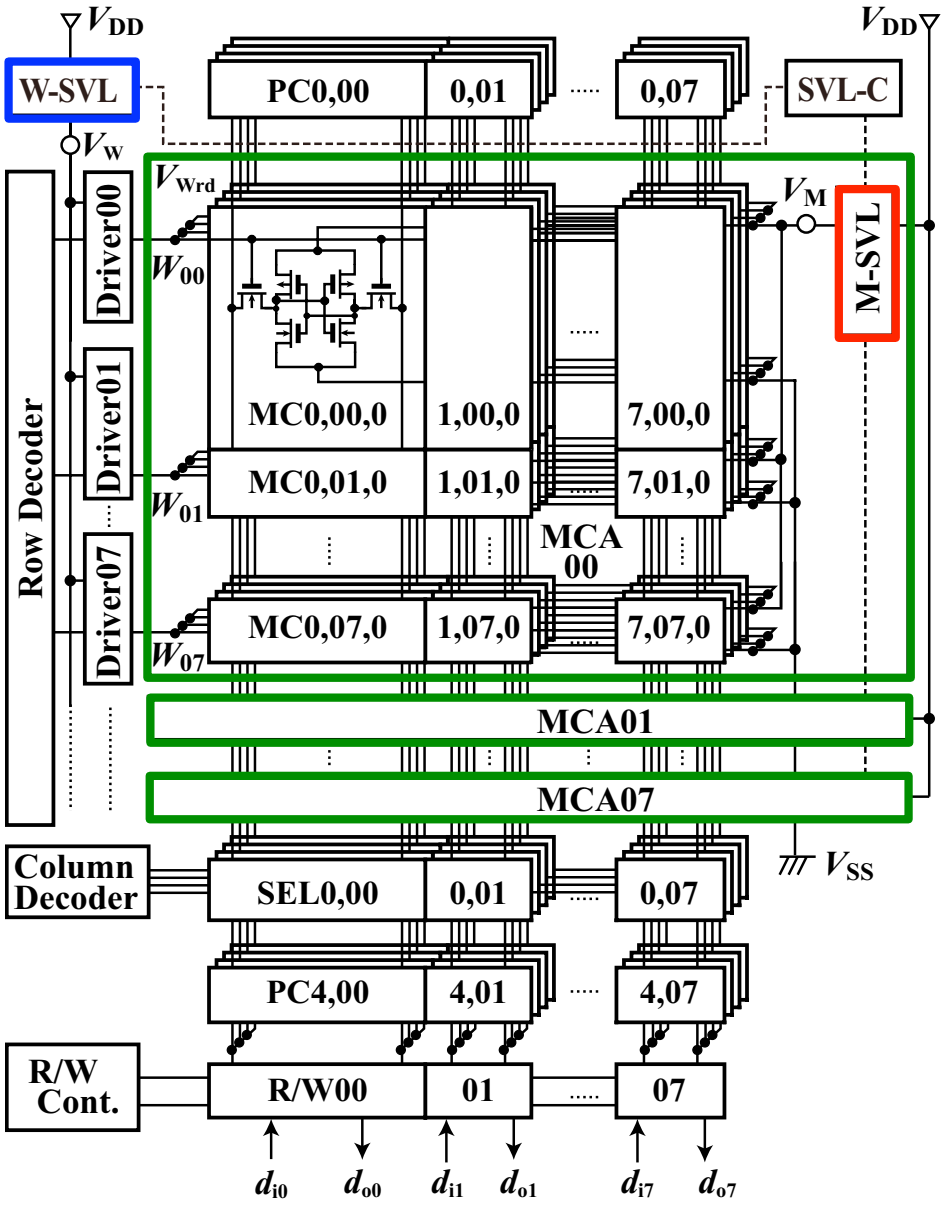
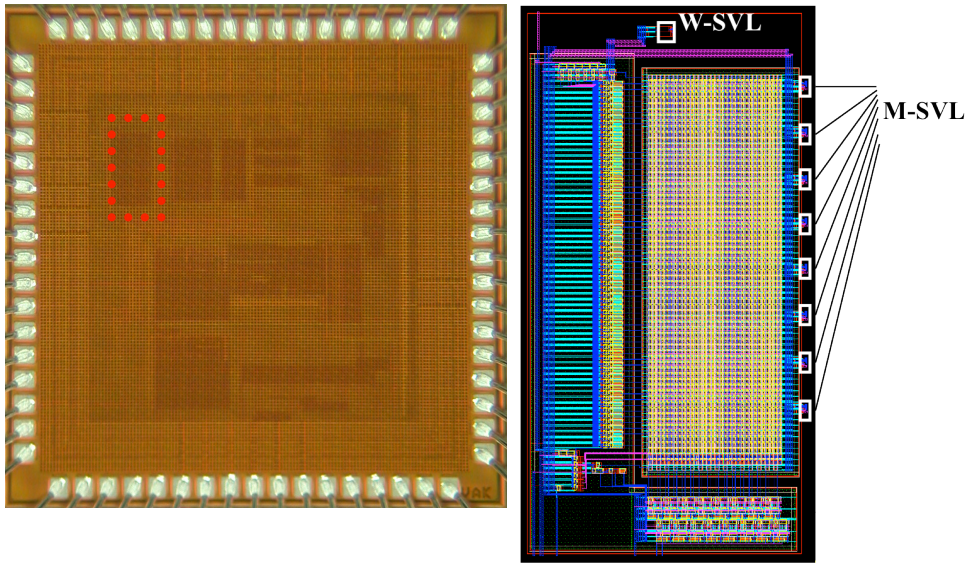
Newly Developed 90-nm 6Tr 2K-bit SRAM





Memory Cell: 8-bit × 64 W × 4 W

W-SVL : 1

(1 SVL/64 Word-line drivers)

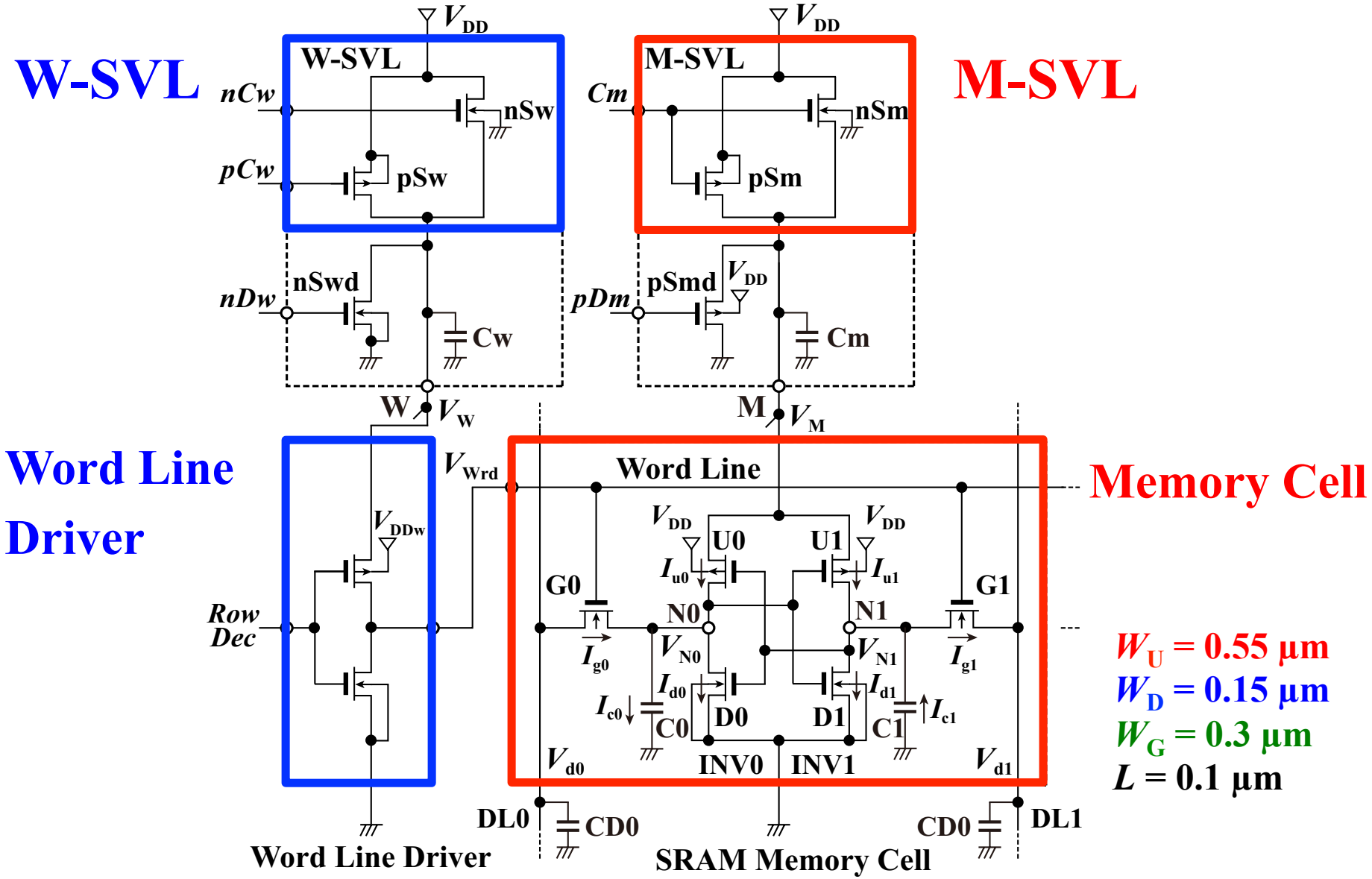
M-SVL : 8

(1 SVL/256 Memory Cells)

Silicon Area: 66,269 µm²

Area Overhead of SVLs: 1.383%

Newly Developed SRAM Memory Cell



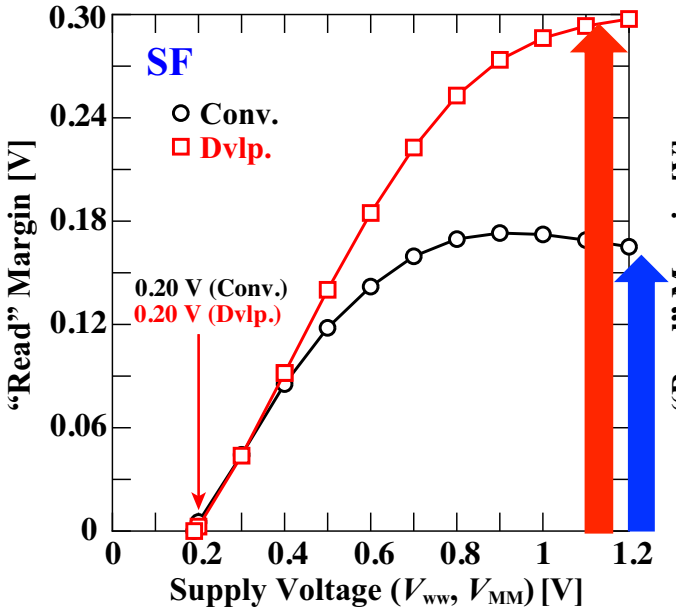
SVL:Self-controllable Voltage Level circuit

“Read” Margin of SRAMs

SF (+6σ)

V_{tn}= 0.275 V (+ 53 mV)

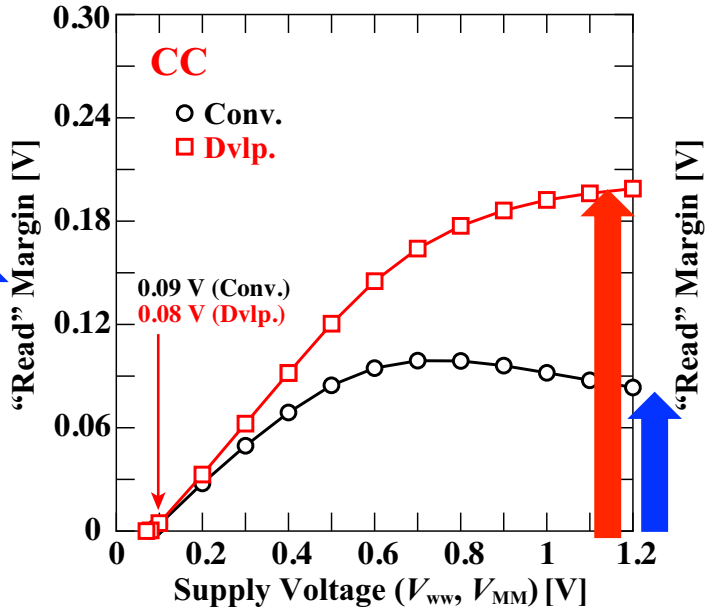
V_{tp}= -0.139 V (+103 mV)



CC (Ave.)

V_{tn}= 0.222 V (0)

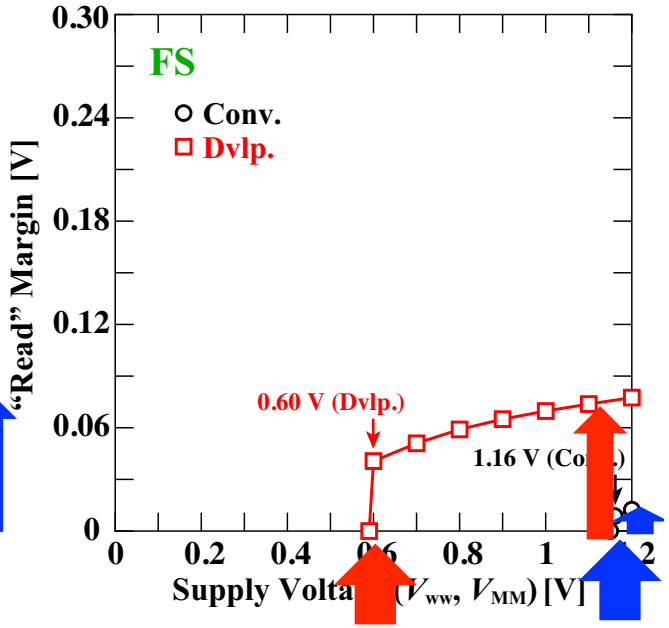
V_{tp}= -0.242 V (0)



FS (-6σ)

V_{tn}= 0.142 V (-80 mV)

V_{tp}= -0.300 V (-58 mV)



V_{WW} = 1.2 V

0.1651 V (Conv.)	100.00 %	0.0834 V (Conv.)	100.00 %
0.2974 V (Dvlp.)	180.13 %	0.1989 V (Dvlp.)	238.48 %

0.60 V 1.16V

0.0124 V (Conv.)	100.00 %
0.0775 V (Dvlp.)	625.00 %

Minimum supply voltage of static “Read” operation

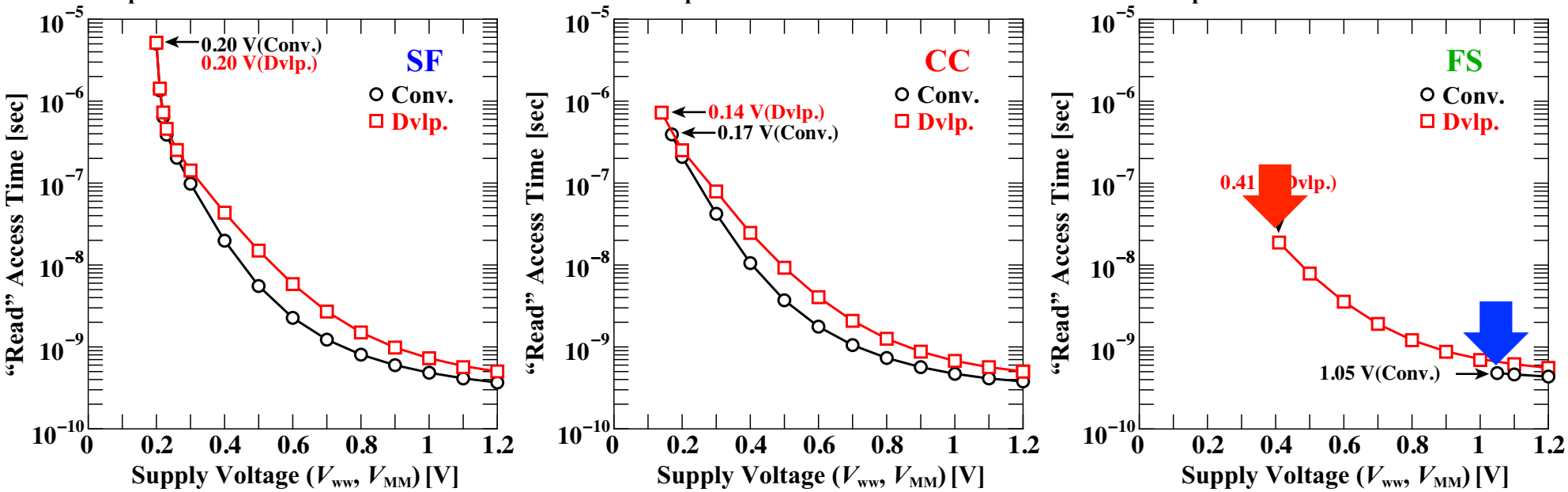
Conv. 0.20 V	Conv. 0.09 V	Conv. 1.16V
Dvlp. 0.20 V	Dvlp. 0.08 V	Dvlp. 0.60 V

“Read” Access Time of SRAMs

SF (+6σ)
V_{tn}= 0.275 V (+ 53 mV)
V_{tp}= -0.139 V (+103 mV)

CC (Ave.)
V_{tn}= 0.222 V (0)
V_{tp}= -0.242 V (0)

FS (-6σ)
V_{tn}= 0.142 V (-80 mV)
V_{tp}= -0.300 V (-58 mV)



V_{WW} = 1.2 V **FS (-6σ : Worst Case)**
Conv. = 435.89 Dvlp. = 556.24 (127.61 %)

Minimum supply voltage for dynamic “Read” operation

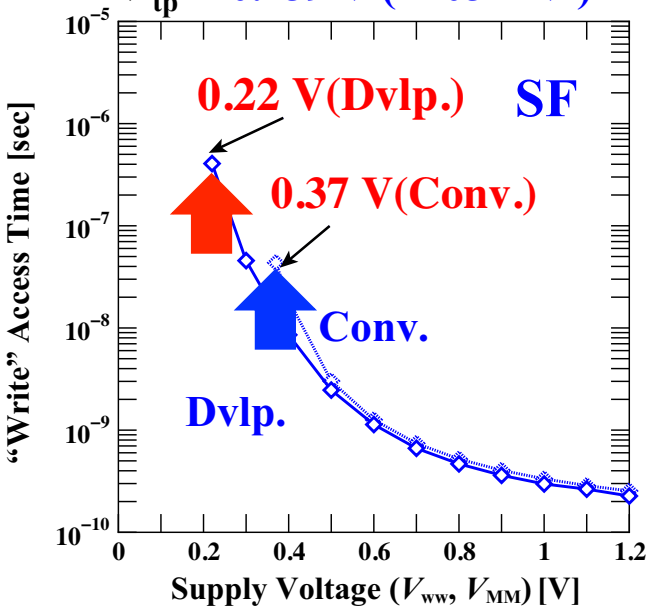
Conv. 0.20 V	Conv. 0.17 V	Conv. 1.05 V
Dvlp. 0.20 V	Dvlp. 0.14 V	Dvlp. 0.41 V

“Write” Access Time of SRAMs

SF (+6σ)

V_{tn}= 0.275 V (+ 53 mV)

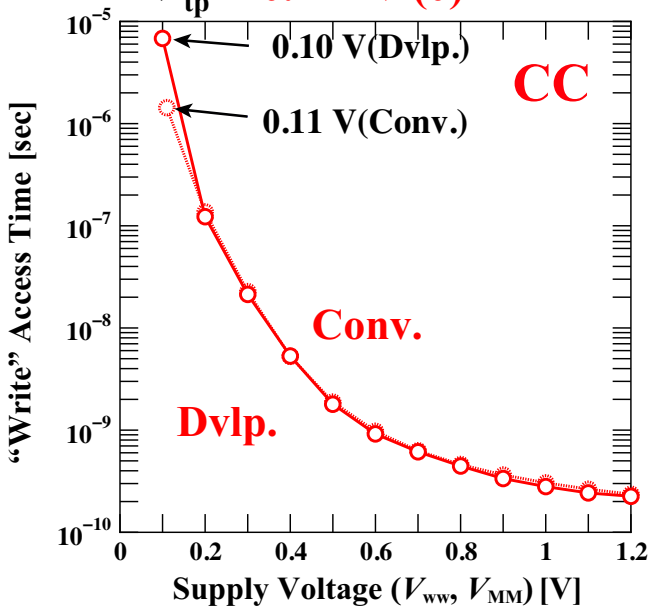
V_{tp}= -0.139 V (+103 mV)



CC (Ave.)

V_{tn}= 0.222 V (0)

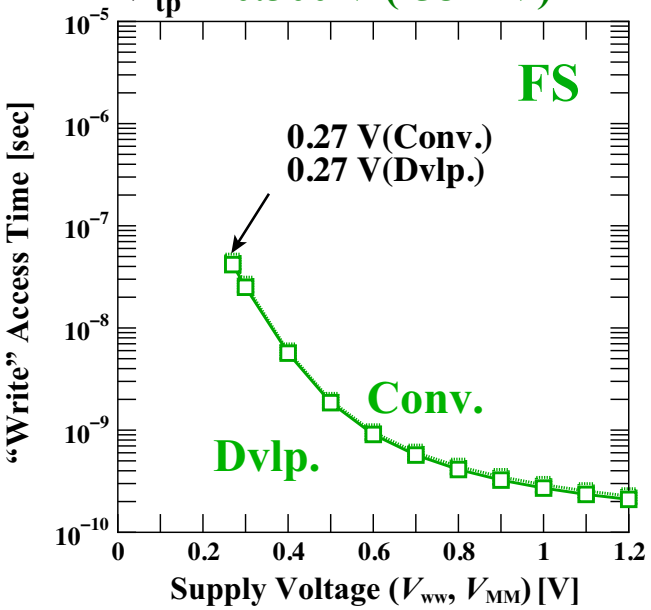
V_{tp}= -0.242 V (0)



FS (-6σ)

V_{tn}= 0.142 V (-80 mV)

V_{tp}= -0.300 V (-58 mV)



V_{WW} = 1.0 **SF (+6σ : Worst Case)**

“Write” Access Time [psec]

Conv. = 333.49 Dvlp. = 297.22 (89.12 %)

Minimum Supply Voltage for dynamic “Write” operation

Conv. 0.37 V	**Conv. 0.11 V**	**Conv. 0.27 V**
Dvlp. 0.22 V	**Dvlp. 0.10 V**	**Dvlp. 0.27 V**

Characteristics of 6Tr 2K-bit SRAM

	"Read" Margin FS V_{DD}=1.2V	Min. Supply Volt. in "Read" FS	Min. Supply Volt. in "Write" SF	Standby Power P_{st} V_{DD}=1.0V	Sillicon Area [μm^2]
Conv. SRAM	0.012 V	1.05 V	0.37 V	25.2 μW	65,365
Dvlp. SRAM	0.078 V	0.41 V (39.05%)	0.22 V (59.46%)	1.17 μW (4.64 %)	66,269 (101.383 %)

SVL :

- Small Area Overhead 1.383%
- Low Voltage Operation, Expand "Read" and "Write" margins