A 128-way FPGA Platform for the Acceleration of KLMS Algorithm

Xiaowei Ren, Qihang Yu, Badong Chen,
Nanning Zheng and Pengju Ren
E-mail: renxiaowei66@gmail.com

IAIR

西安交通大學
XI'AN JIAOTONG UNIVERSITY

Quantized KLMS

Initialization: $C(1) = x_1 \qquad a(1) = \eta d_1$

while $\{x_n, d_n\}$ is available, do

% evaluate the output

$$f(n) = \sum_{j=1}^{size(C(n-1))} a_j(n-1)\kappa(C_j(n-1), x_n) \qquad \kappa(C_j(n-1), x_n) = \exp^{(-\frac{(C_j(n-1)-x_n)^2}{2\sigma^2})}$$

%compute error $e(n) = d_n - f(n)$

%calculate the distance between x_n and current codebook

$$dis(x_n, C(n-1)) = \min_{1 \le j \le size(C(n-1))} \left\| x_n - C_j(n-1) \right\|$$

%update the codebook and corresponding coefficient

if $dis(x_n, C(n-1)) > \varepsilon_X$, then $C(n) = \{C(n-1), x_n\},\ a(n) = \{a(n-1), \eta e(n)\}$

else $\qquad C(n) = C(n-1), \qquad a_{j^*}(n) = a_{j^*}(n-1) + \eta e(n)$

where $\qquad j^* = \arg \min_{1 \le j \le size(C(n-1))} \left\| x_n - C_j(n-1) \right\|$

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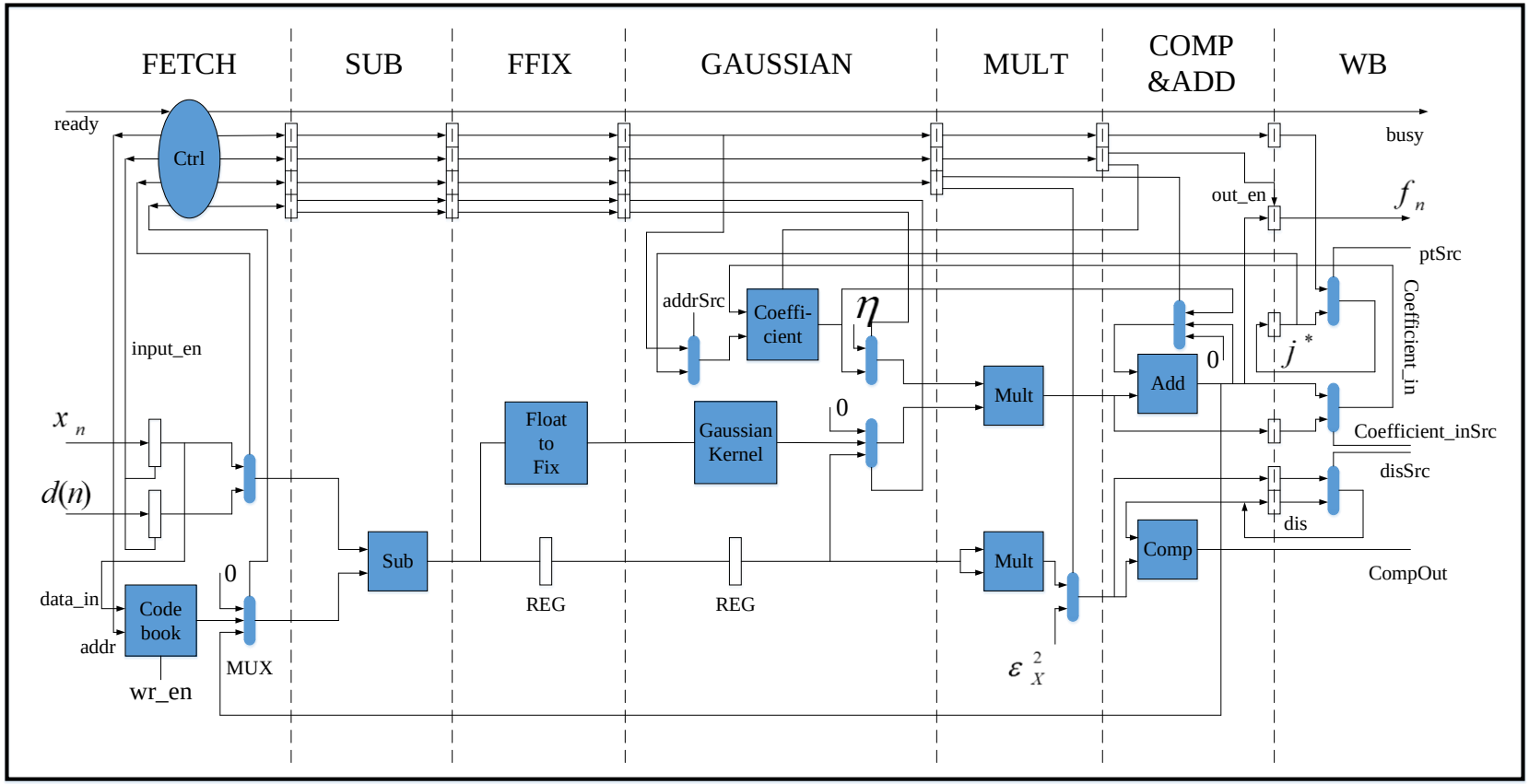
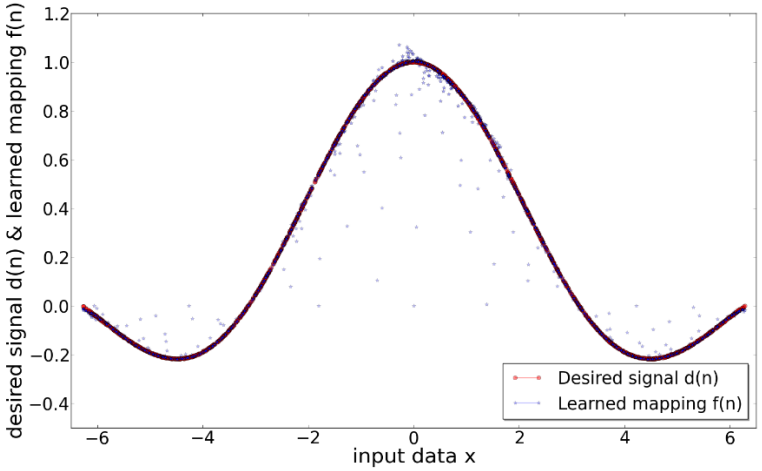
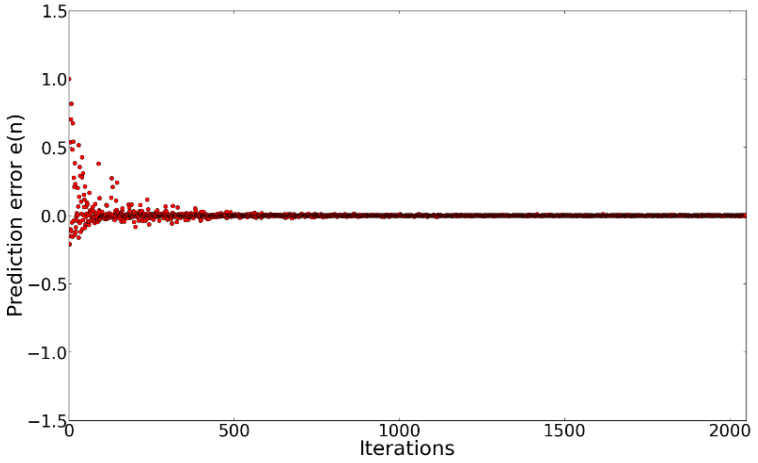
Microarchitecture of PE



Prediction Error



(a) Learned and desired mapping



(b) Prediction error of every iteration

Processing element is tested with the following function:

$$d_n = \frac{\sin(x_n)}{x_n} + v_n$$

Speedup

Number of Iterations	FPGA (ms)	Matlab (s)	Speedup
1024	0.986	2.884	2925
2048	2.384	8.679	3641
4096	5.360	24.346	4542
8192	11.520	66.094	5737
16384	23.971	174.712	7288

Hardware Cost

Resources	Utilized	Available	Utilization Rate (%)
Flip Flop	85248	2443200	3.49
LUT	146816	1221600	12.02
Memory LUT	1280	344800	0.37
I/O	100	1200	8.33
Block RAM	512	1292	39.63
DSP48	1024	2160	47.41
BUFG	2	128	1.562
MMCM	1	24	4.167