ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Call for Papers
ASP-DAC 2015

http://www.aspdac.com/aspdac2015/
January 19-22, 2015
Chiba/Tokyo (Makuhari Messe Convention), Japan

Aims of the Conference:
ASP-DAC 2015 is the 20th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

1. System-Level Modeling and Design Methodologies:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis and optimization
1.3. Model- and component-based embedded system/software design
1.4. System-level formal verification
1.5. System-level modeling, simulation and validation tools/methodologies

2. Embedded System Architectures and Design:
2.1. Cyber physical systems
2.2. Dependable embedded systems
2.3. Storage system architecture
2.4. Domain-specific embedded systems
2.5. Internet of things

3. On-chip Communication and Networks-on-Chips:
3.1. On-chip communication networks
3.2. Networks-on-chips
3.3. Interface and I/O design
3.4. Optical and RF on-chip communications

4. System-on-Chip Architectures and Design:
4.1. Many- and multi-core SoC architectures
4.2. Reconfigurable and self-adaptive SoC architectures
4.3. Application-specific SoC architectures
4.4. IP/platform-based SoC design
4.5. Dependable SoC architectures
4.6. On-chip memory architectures

5. Device/Circuit-Level Modeling, Simulation and Verification:
5.1. Device/circuit/interconnect modeling and analysis
5.2. Device/circuit-level simulation tools and methodologies
5.3. RTL and gate-leveling modeling, simulation and verification
5.4. Circuit-level formal verification

6. Logic/Behavioral/High-Level Synthesis and Optimizations:
6.1. High-level synthesis tools and methodologies
6.2. Combinational, sequential and asynchronous logic synthesis
6.3. Logic synthesis and physical design techniques for FPGAs
6.4. Library mapping, cell-based design and optimization
6.5. Technology-independent optimization
6.6. Technology mapping

7. Analog, RF and Mixed Signals:
7.1. Analog/mixed-signal/RF synthesis
7.2. Analog/mixed-signal/RF testing
7.3. Analog layout verification and simulation techniques
7.4. Noise analysis
7.5. High-frequency electromagnetic simulation of circuits
7.6. Mixed-signal design consideration
7.7. Power-aware analog circuit/system design
7.8. Analog/mixed-signal modeling and simulation techniques

8. System-Level Power and Thermal Management:
8.1. System-level low-power design and thermal management
8.2. System-level power modeling, analysis and simulation
8.3. Cross-layer reliability and aging
8.4. Architectural low-power design techniques
8.5. Energy harvesting and battery management

9. Device/Circuit/Gate-Level Low Power Design:
9.1. Device/circuit/gate-level low-power design and methodologies
9.2. Device/circuit/gate-level power modeling, analysis and simulation
9.3. Device/circuit/gate-level thermal aware design

10. Embedded Software:
10.1. Kernel, middleware and virtual machines
10.2. Compiler and toolchains
10.3. Real-time systems
10.4. Resource allocation for heterogeneous computing platforms
10.5. Storage software and applications
10.6. Human-computer interface
10.7. System verification and analysis

11. Physical Design:
11.1. Floorplanning, partitioning and placement
11.2. Interconnect planning and synthesis
11.3. Placement and routing optimization
11.4. Clock network synthesis
11.5. Post layout and post-silicon optimization
11.6. High-level physical design and synthesis
11.7. Package/PCB/3D-IC routing
11.8. Physical verification

12. Timing and Signal/Power Integrity:
12.1. Deterministic/statistical timing and performance analysis and optimization
12.2. Power/ground and package modeling, analysis and optimization
12.3. Signal/power integrity, EM modeling and analysis
12.4. Extraction, TSV and package modeling
12.5. 2D/3D on-chip power delivery network analysis and optimization

13. Design for Manufacturability and Reliability:
13.1. Reticle enhancement, lithography-related design and optimization
13.2. Resilience under manufacturing variations
13.3. Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
13.4. Reliability, aging and soft error analysis
13.5. Design for reliability and robustness

14. Test and Design for Testability:
14.1. ATPG, BIST and DFT
14.2. Fault modeling and simulation
14.3. System test and 3D IC test
14.4. Online test and fault tolerance
14.5. Memory test and repair
14.6. Analog and mixed-signal test

15. Security and Fault-Tolerant Systems:
15.1. Security modeling and analysis
15.2. Architectures, tools and methodologies for secure hardware
15.3. Design for security and security primitives
15.4. Cross-layer security
15.5. Fault analysis, detect and tolerance

16. Emerging Technologies:
16.1. New transistor/device and process technologies: spintronic, phase-change, single-electron etc.
16.2. CAD for nanotechnologies
16.3. CAD for MEMS
16.4. CAD for 3D ICs
16.5. CAD for quantum computing

17. Emerging Applications I:
17.1. Biological and bioelectronics systems
17.2. Biomedical applications
17.3. Bio-inspired computing systems
17.4. CAD for biosystems
17.5. Big data applications
17.6. Advanced multimedia applications

18. Emerging Applications II:
18.1. Energy-storage/smart-grid/smart-building design and optimization
18.2. Datacenter optimization
18.3. Automotive system design and optimization
18.4. Electromobility

ACM, IEEE, and IEICE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission:	**5 PM JST (UTC+9),**	**July 11 (Fri), 2014**
Notification of acceptance:		**Sep. 15 (Mon), 2014**
Deadline for final version:	**5 PM JST (UTC+9),**	**Nov. 10 (Mon), 2014**

For detailed instructions for submission, please refer to the "Authors' Guide" at:
http://www.aspdac.com/aspdac2015/

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2015-sec@mls.aspdac.com) no later than May 30 (Fri), 2014.

Contact: Conference Secretariat: aspdac2015-sec@mls.aspdac.com TPC Secretariat: aspdac2015-tpc@mls.aspdac.com

Call for Designs

University LSI Design Contest
ASP-DAC 2015
http://www.aspdac.com/aspdac2015/
January 19-22, 2015
Chiba/Tokyo, Japan

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Aims of the Contest:

As a unique feature of ASP-DAC 2015, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

(1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
(2) Designs that report actual measurements from implementations;
(3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
(1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.
Methods or technology used for implementation include:
(a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at **http://www.aspdac.com/aspdac2015/**

Deadline for summary:	5PM JST (UTC+9) Jul. 11 (Fri.), 2014
Notification of acceptance:	Sep. 15 (Mon.), 2014
Deadline for camera-ready:	5PM JST (UTC+9) Nov. 10 (Mon.), 2014

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:
(1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design,
(4) Novelty of application, algorithm, architecture, (5) Others.
Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2015. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2015-udc@mls.aspdac.com

ASP-DAC 2015 Chairs

General Chair:	**Kunio Uchiyama (Hitachi, Japan)**
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	Noriyuki Miura (Kobe University, Japan)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, IEICE ESS, IPSJ SIGSLDM