

# A 15 x 15 SPAD Array Sensor with Breakdown-Pixel-Extraction Architecture for Efficient Data Readout

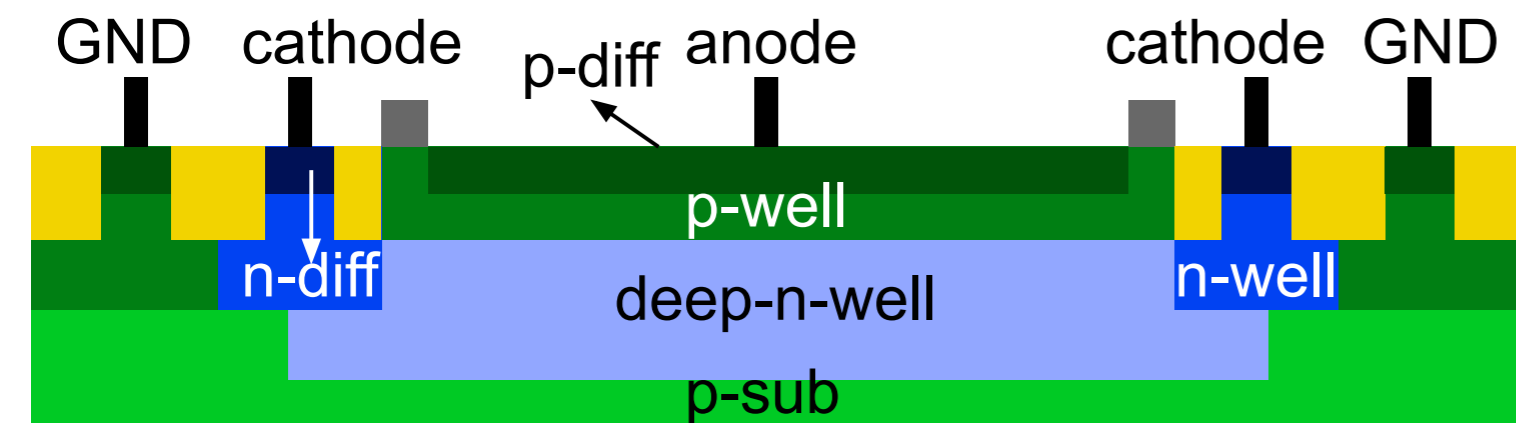
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1. EEIS, Graduate School of Engineering, The University of Tokyo

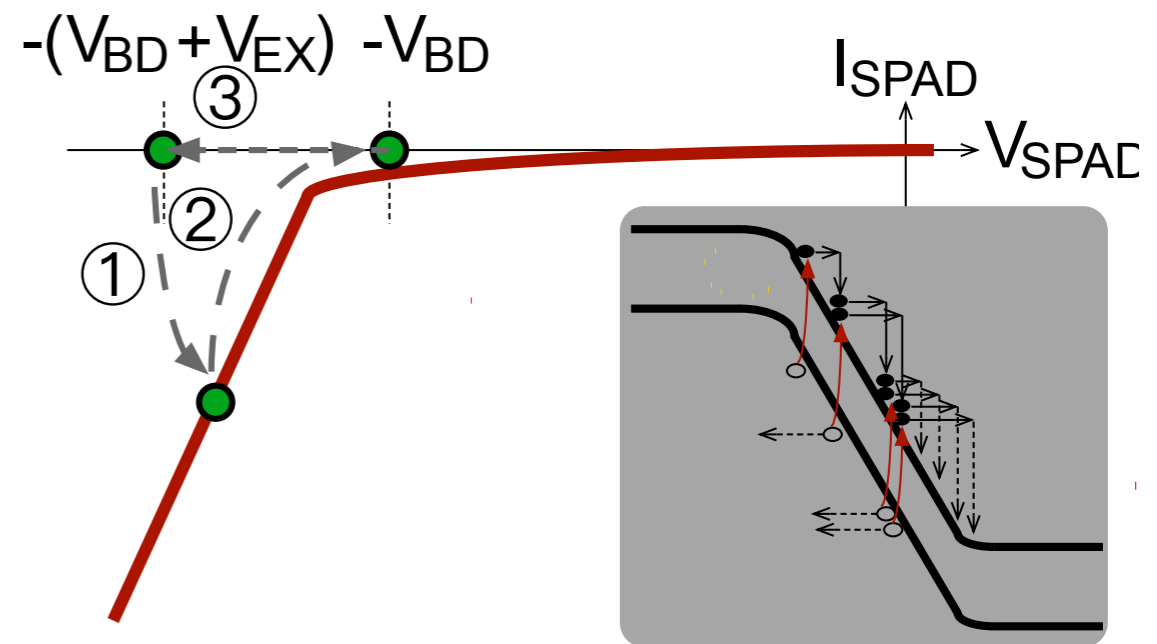
2. VLSI Design and Education Center (VDEC), The University of Tokyo

## Single photon avalanche diode (SPAD)

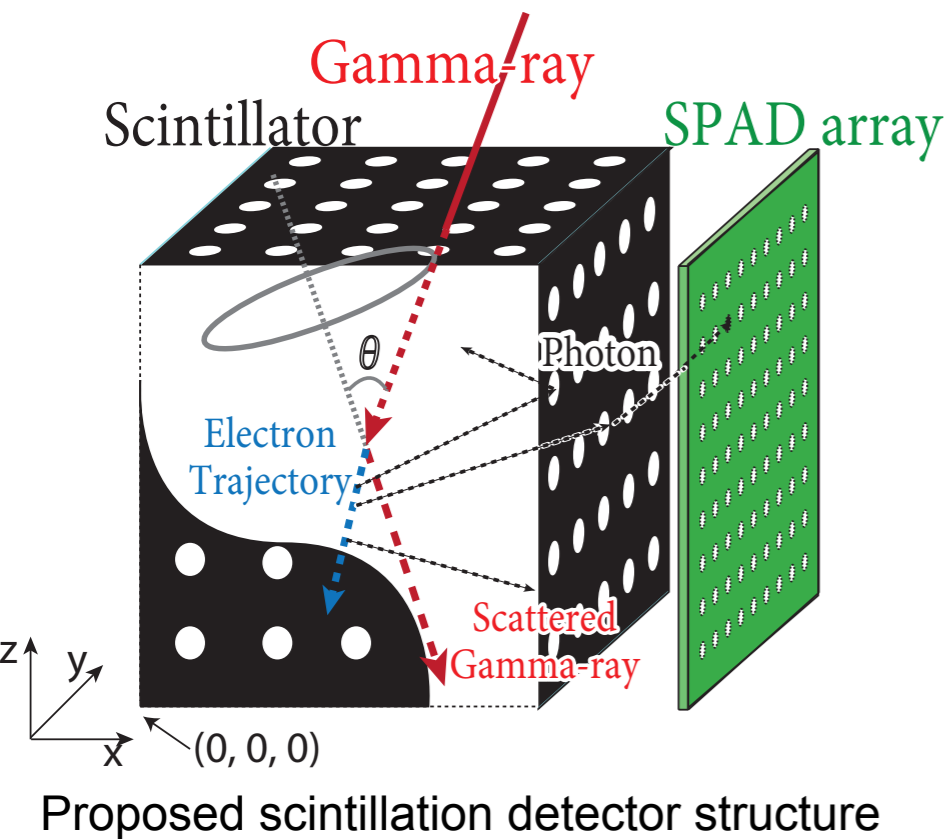
- P-N diode reversely biased above breakdown voltage
- High sensitivity, fine time resolution
- Binary output (stable or breakdown)



CMOS SPAD in our design



# SPAD array sensor for scintillation detector



## Proposed scintillation detector

- Scintillator coated with pinholes array
- Surrounded by SPAD array sensors

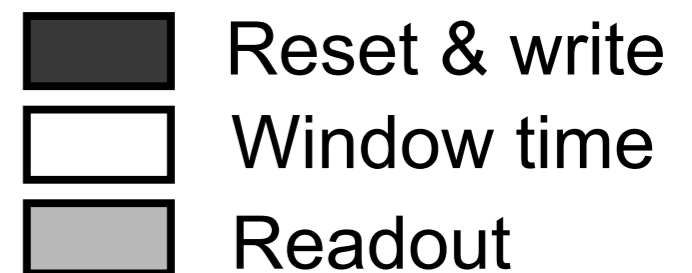
## Scintillation event

- Compton scattering caused by gamma-ray
- Emitting scintillation photons
- SPAD array sensors capture the photons
- Finer spatial resolution

Scintillation light

Window time

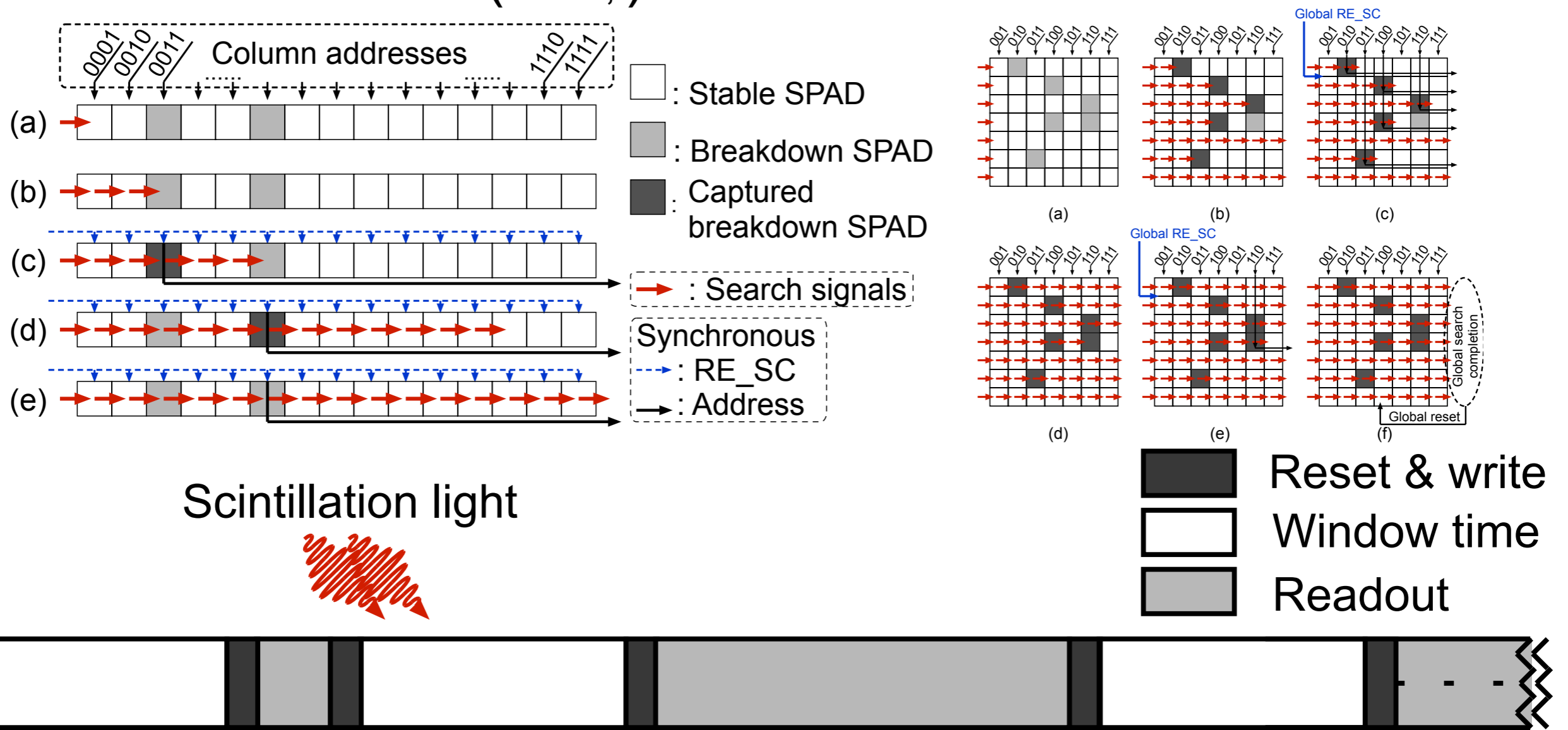
Dead time



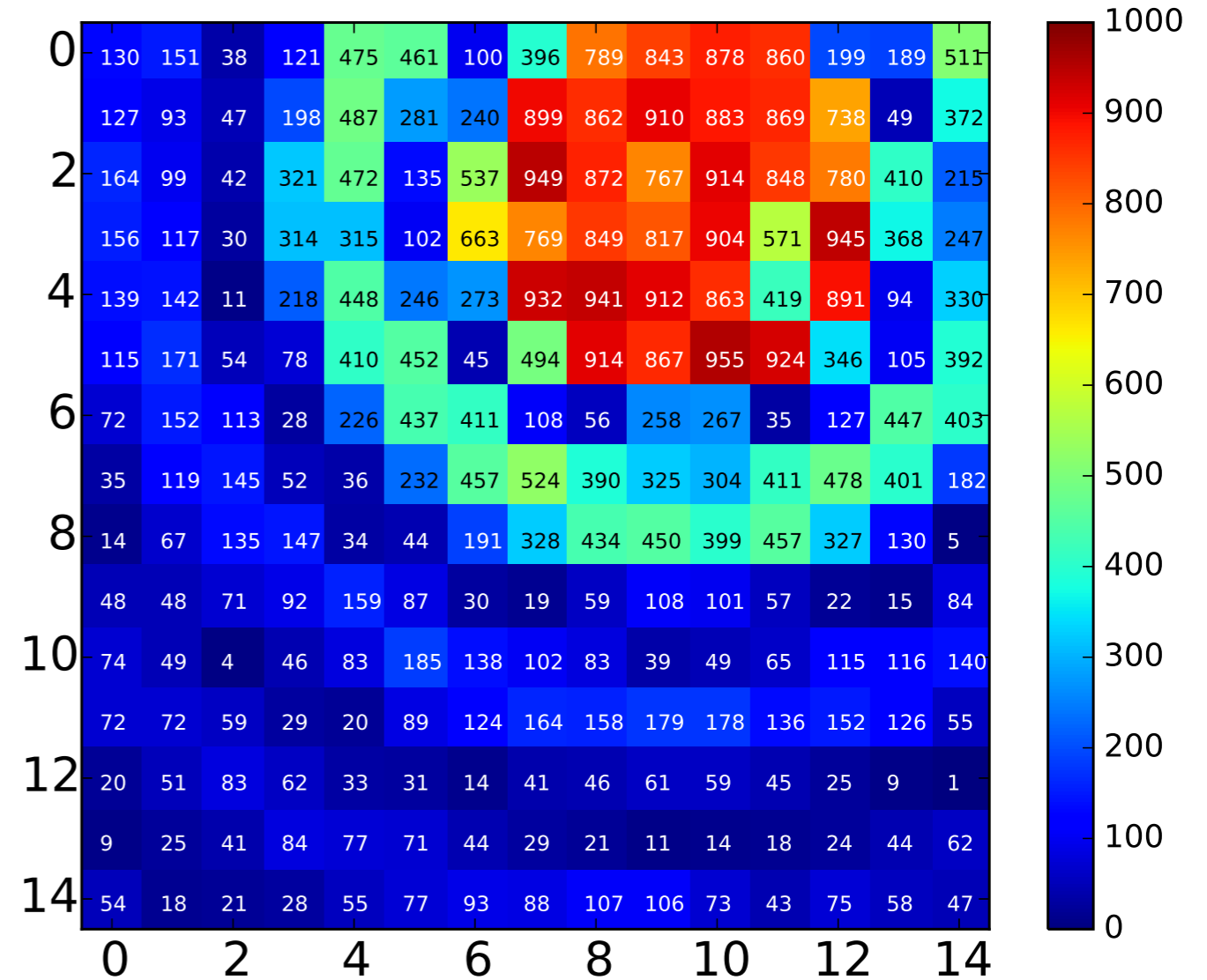
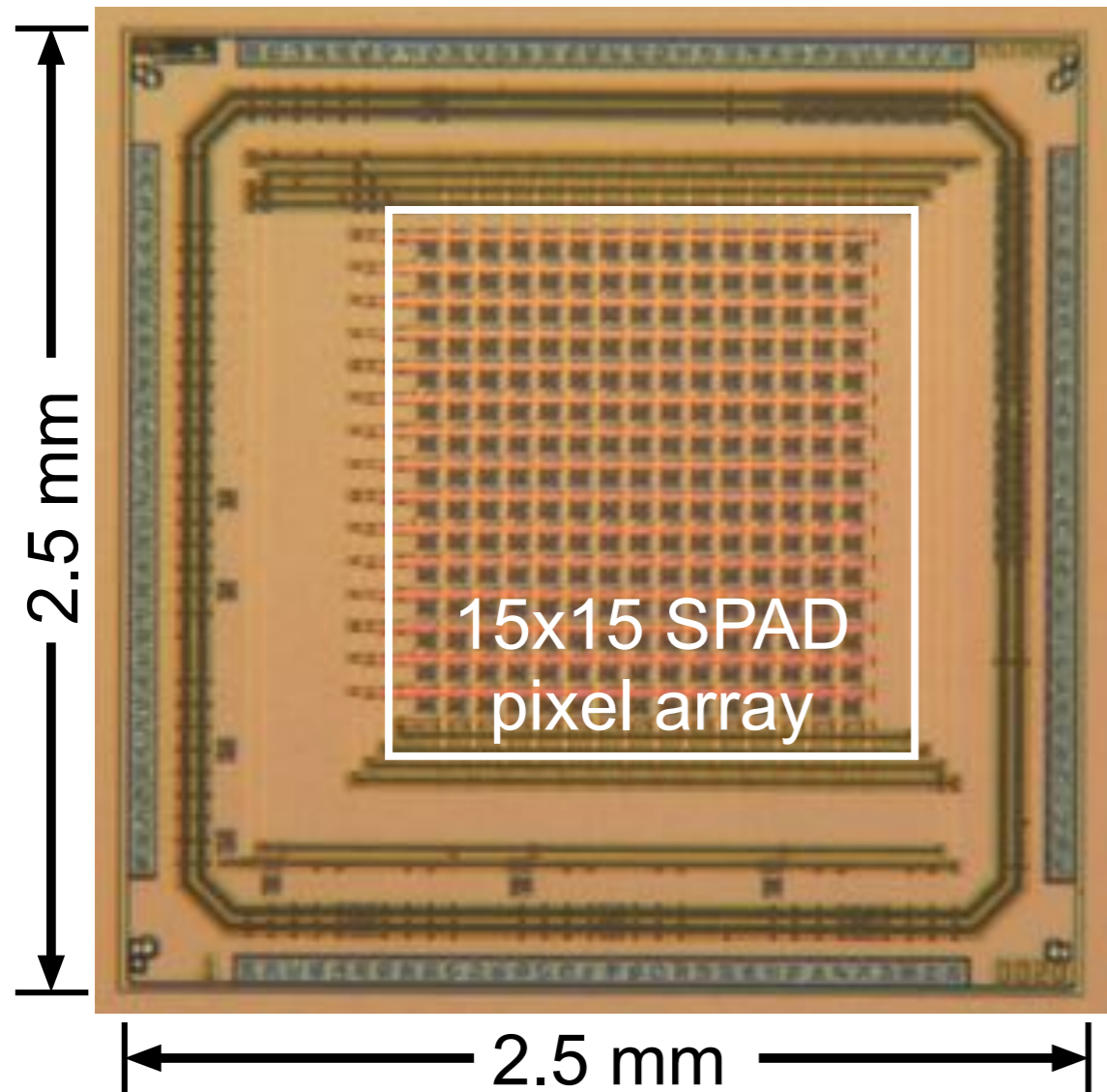
The ratio between **window time** and **dead time** is important

## Breakdown-pixels-extraction (BPE) architecture

- Extraction the addresses of breakdown pixels in row parallel
- Readout cycles:  $1 + \text{Max}(N_{BD,i}) \times (5 + 1)$  (  $31 \times 31$  SPAD array)
- Dark condition:  $\text{Max}(N_{BD,i})$  is small  $\rightarrow$  shorter dead time



$N_{BD}$ : the # of breakdown pixels in the whole chip  
 $N_{BD,i}$ : the # of breakdown pixels in the  $i$ -th row



**Our design is presented at poster session 1S-10.**

**I look forward to a fruitful discussion.  
Thank you.**