A 686Mbps 1.85mm^2 Near-Optimal Symbol Detector for Spatial Modulation MIMO Systems in 0.18μm CMOS

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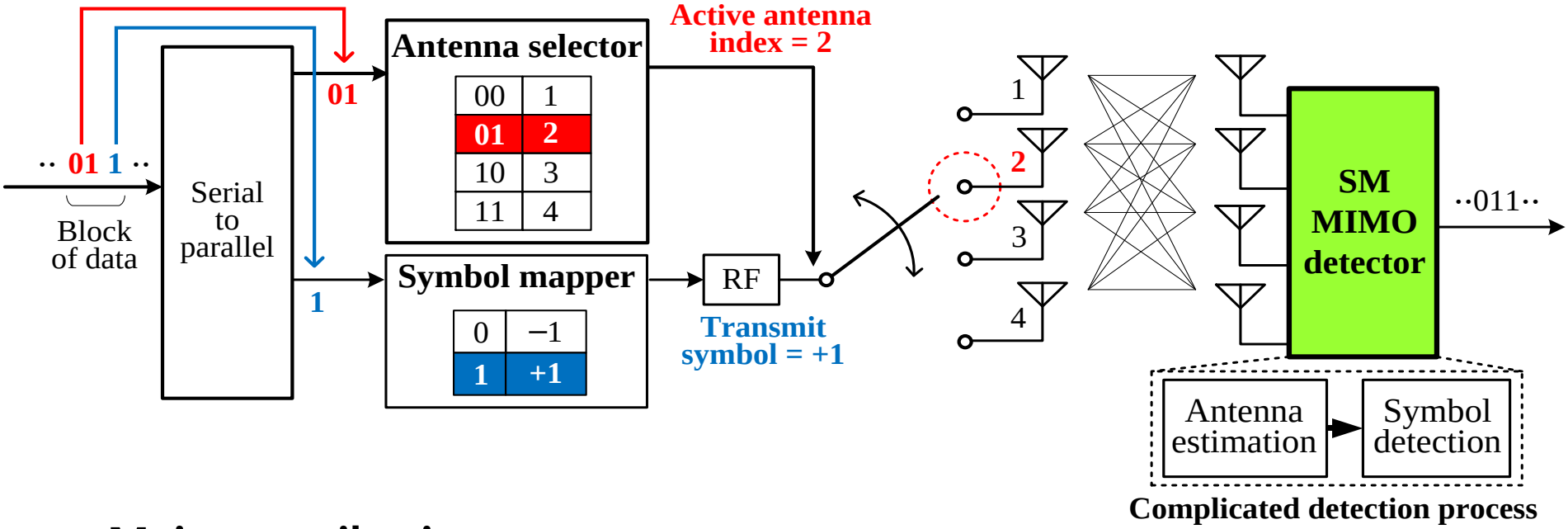
TARGET SYSTEM AND MAIN CONTRIBUTIONS

◆ **Spatial modulation (SM) MIMO systems** [1]



◆ **Main contributions**

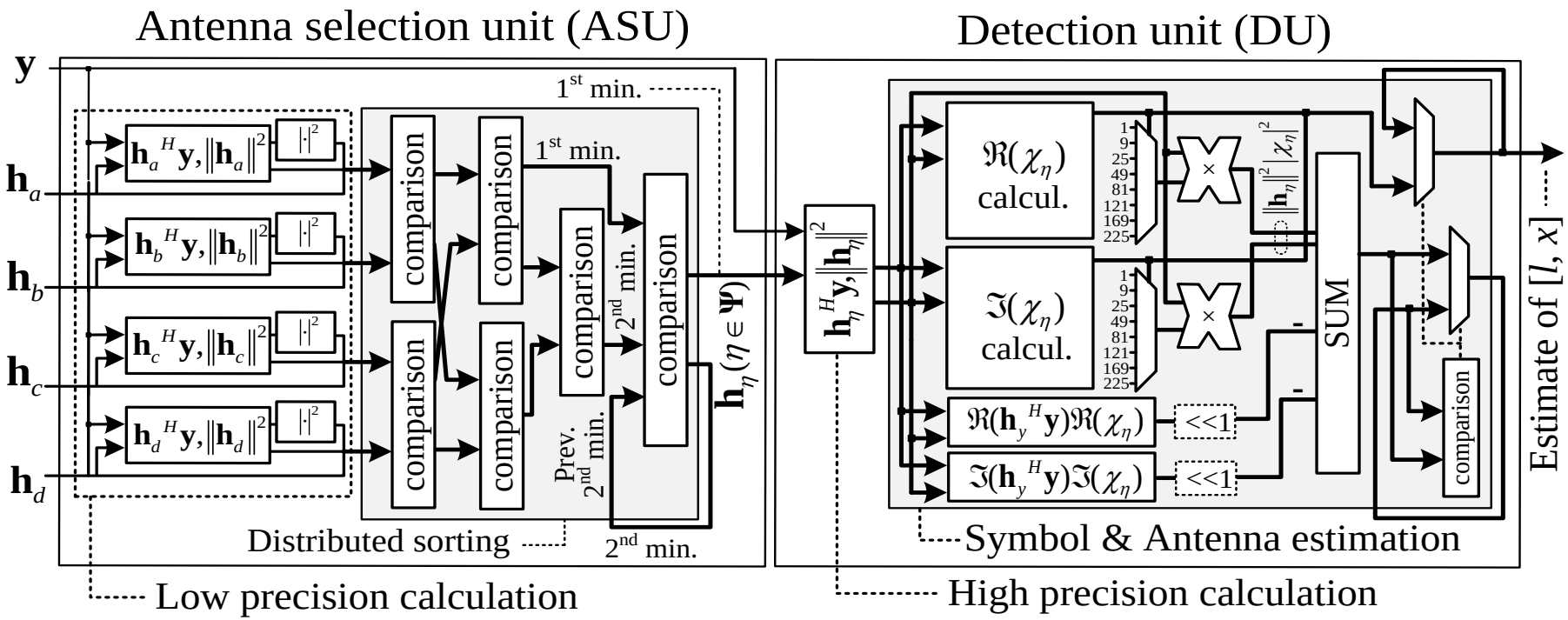
- **Low-complexity** architecture design based on the proposed method
- **Chip level implementation**
  - → Chip I/O measurement using the oscilloscope and the logic analyzer
  - → **Functionality verification** under the '**hardware-in-the-loop**' environment

[1] J. Jeganathan, A. Ghrayeb, and L. Szczecinski, "Spatial modulation: optimal detection and performance analysis," IEEE Commun. Lett., vol. 12, no. 8, pp. 545–547, Aug. 2008.

PROPOSED LOW-COMPLEXITY SM-MIMO DETECTOR

- Distributed sorting based antenna selection
- low-complexity dual-data-path architecture

The interested readers can be referred to our previous paper [2]



[2] G. H. Lee and T. H. Kim, "Implementation of a Near-Optimal Detector for Spatial Modulation MIMO Systems," IEEE Trans. Circuit Syst. II: Exp. Briefs, in press.

IMPLEMENTATION RESULTS

◆ **ASIC with a 0.18μm CMOS technology**

: First hardware implementation of the MIMO detector targeting spatial modulation systems

- **Implementation results**

Target MIMO configuration	N_T x 4 SM-MIMO [a]	
Supported modulation schemes	4, 16, 64, 256 QAM	
Detection modes	Modified SVLD ($K = \{1, \dots, 4\}$)	
Architecture	Dual data path architecture	
Technology	0.18μm CMOS	
Maximum operating frequency	**286 MHz**	
Equivalent gate count	ASU	64.5K
	DU	22.9K
	Total	**87.4K**

a) The proposed detector is configurable to support any number of the transmit antennas ($1 \leq N_T$)

b) This result is estimated for 8 x 4 64 QAM SM-MIMO system when K is configured to 4

- **Throughput and power consumption**

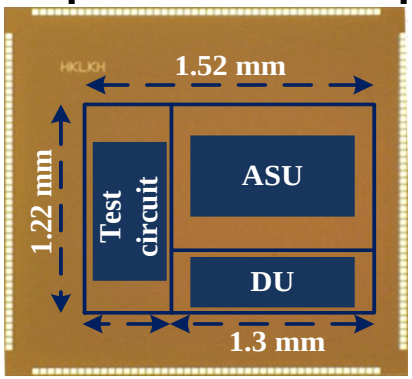
MIMO config.	8 × 4 QPSK	16 × 4 16QAM	8 × 4 64QAM	16 × 4 256QAM
Throughput (Mbps)	286	457	514	**686**
Power (mW)	75.9	119.3	84.4	139.4

MEASUREMENT RESULTS

◆ Chip I/O Measurement

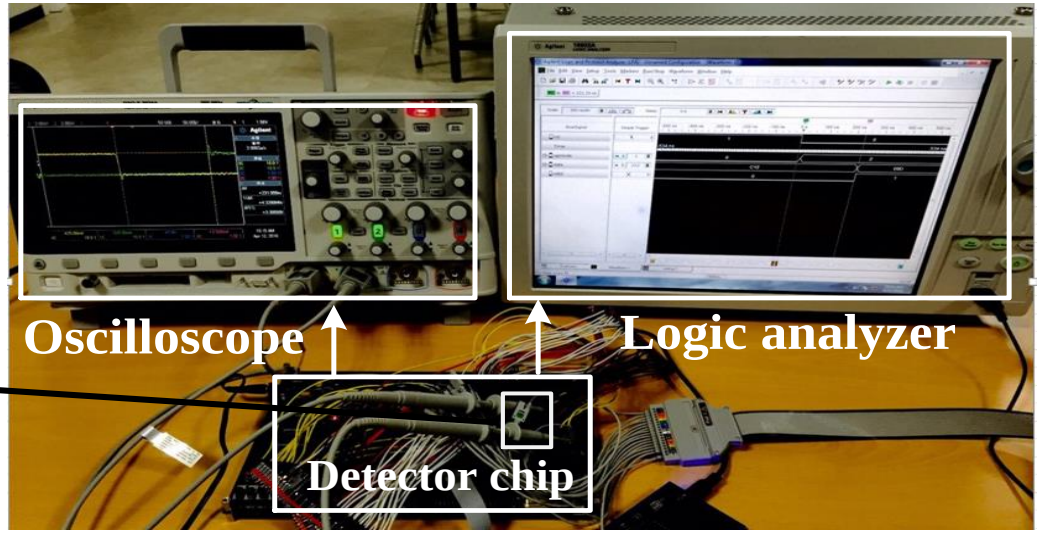
: Functionality verification

Die photo of the chip



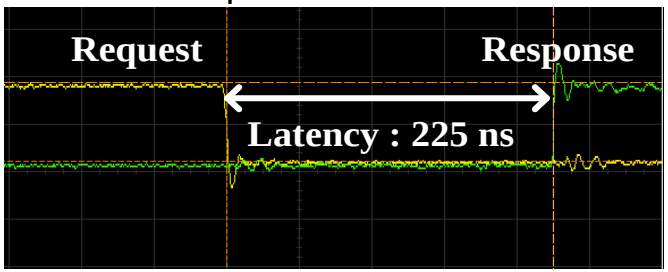
Chip size
:1.586mm^2

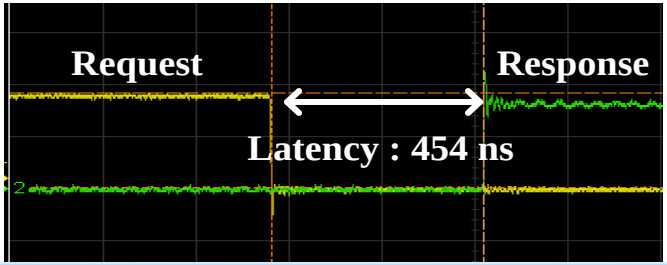
Chip Measurement environment



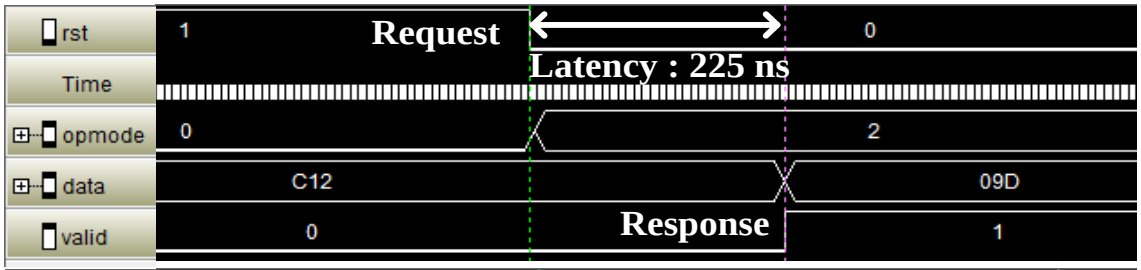
• Measurement results (50MHz,25MHz)

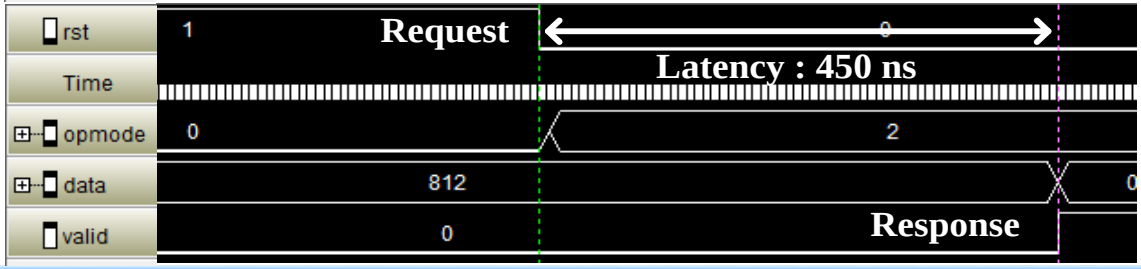
Oscilloscope results





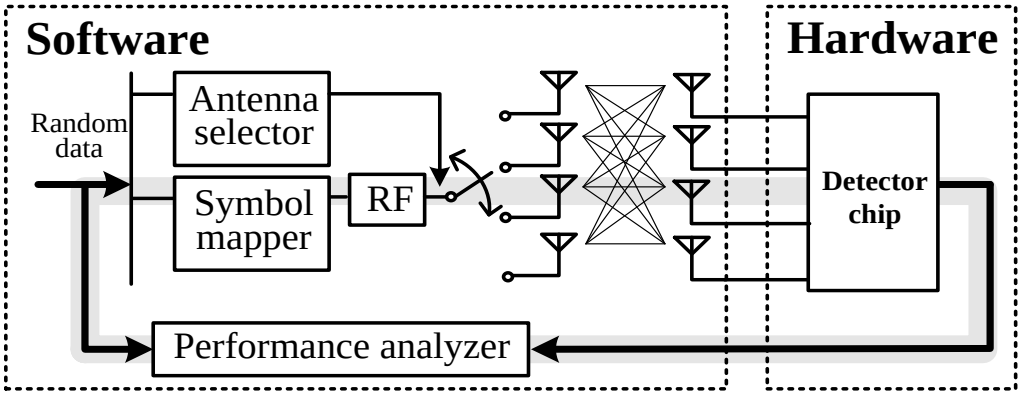
Logic analyzer results

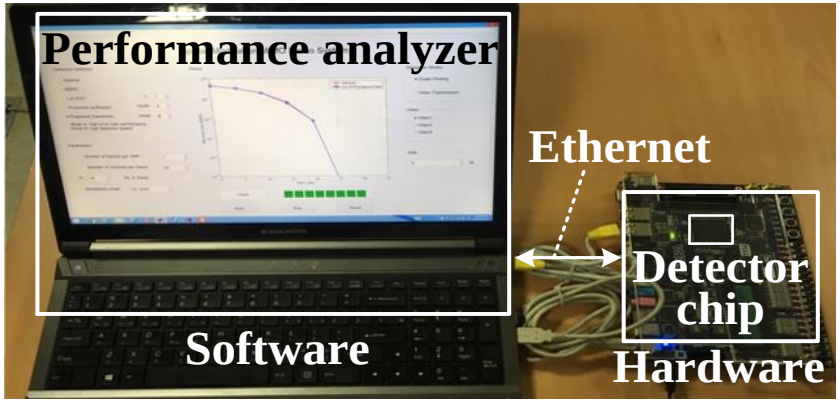




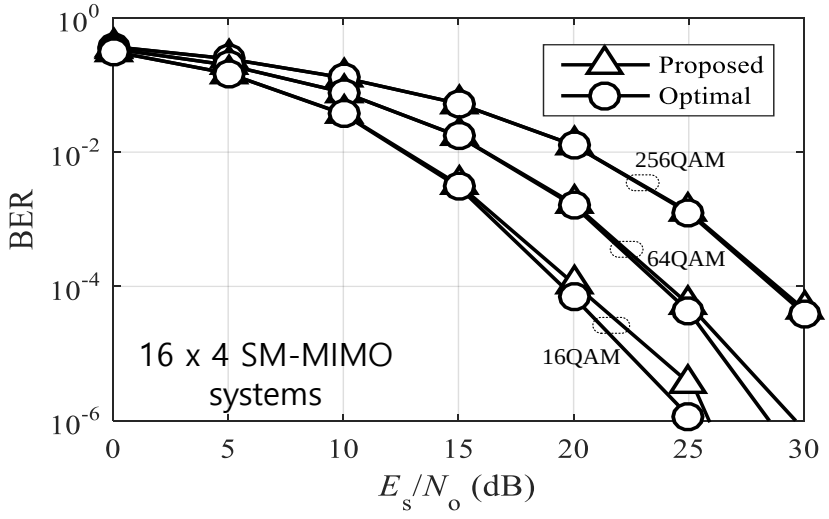
VERIFICATION RESULTS

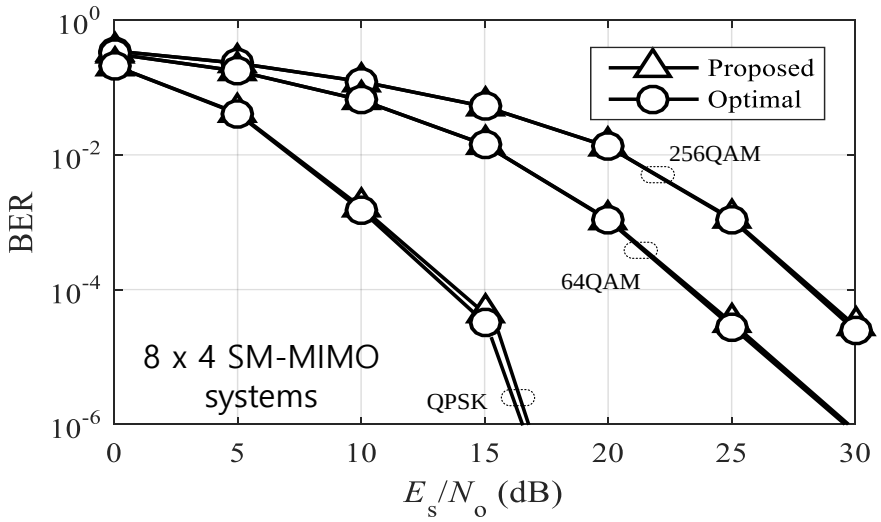
◆ **Hardware-in-the-loop (HIL) environment**





• **Verification results** Near-optimal BER performance





You can find the details of our implementation in the poster.