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Pursuing Excellence

An HDL-Synthesized Injection-Locked PLL Using LC-Based DCO for On-chip Clock Generation

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Synthesizable Analog Circuits

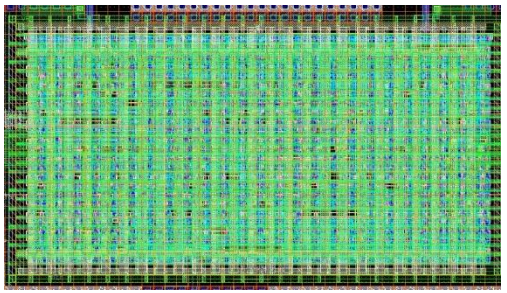
HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

e.g. Encounter, IC Complier, Design Compiler, PrimeTime, Commercial P&R tools…

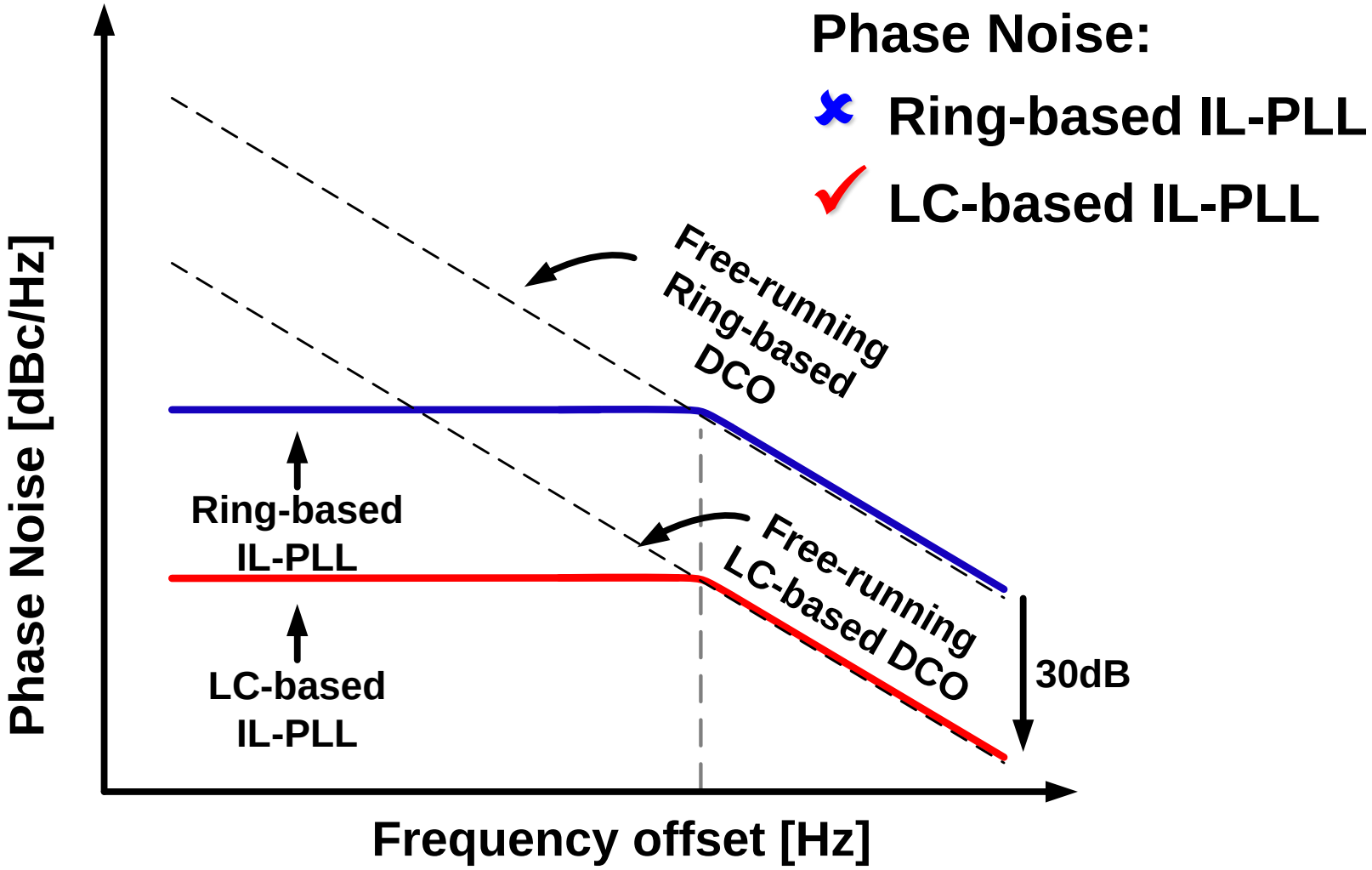
GDS



with a standard-cell library
without any custom-designed cells
without manual placement

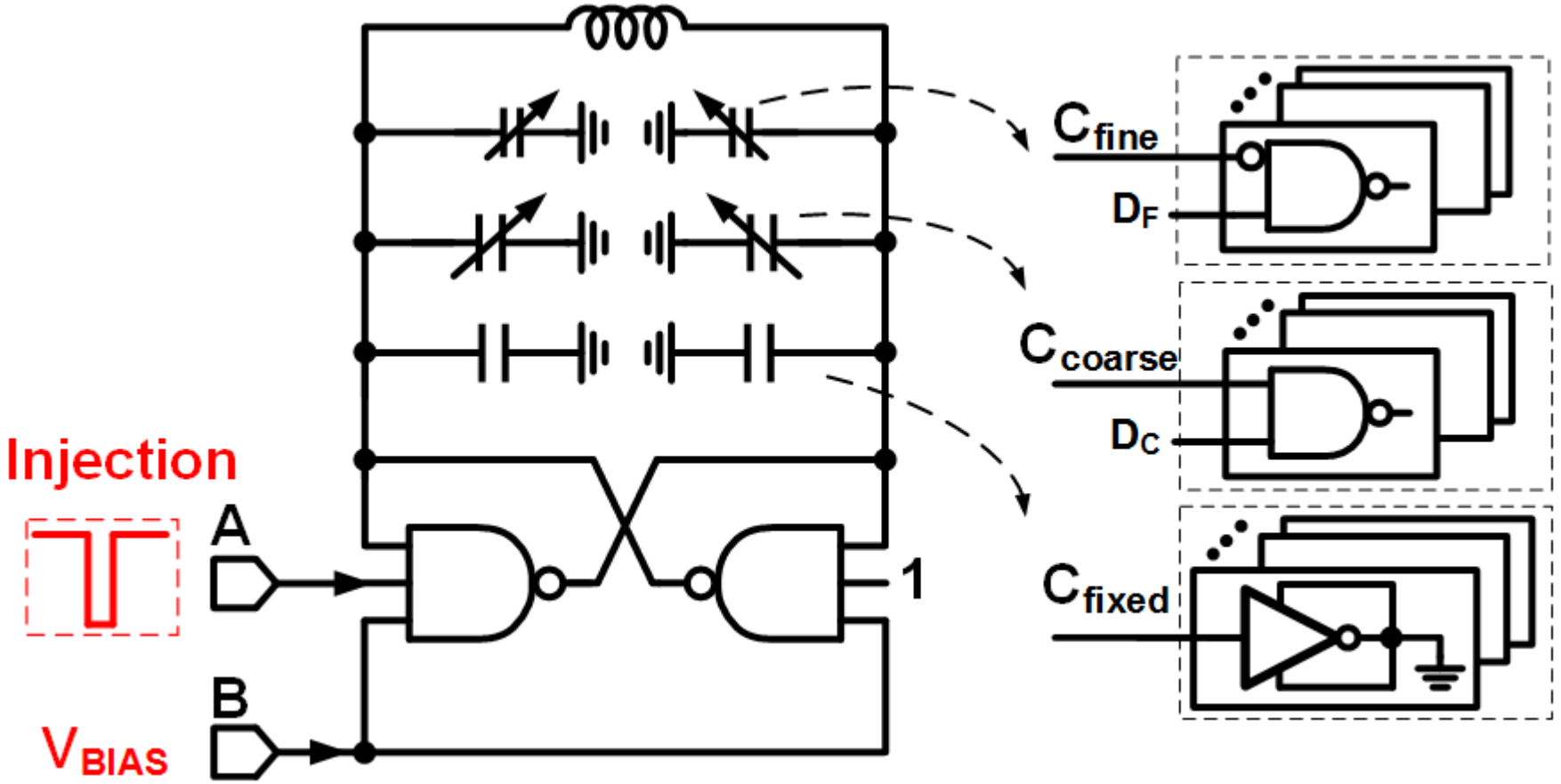
[W. Deng, *et al.*, ISSCC 2014]

Phase Noise Improvement



[D. Yang *et al.*, ESSCIRC 2016]

Proposed LC-DCO Core



1) HDL-synthesized LC-DCO Core
2) Gm-cell using 3-input NAND

Performance Comparison

	[4]	[6]	[9]	This work
Process	65nm	65nm	65nm	65nm
Frequency [GHz]	6.75-8.25	0.96-1.44	0.9	3.0
RMS Jitter [ps]	0.19	0.185	2.8	0.142
FoM [dB]	-251	-244.9	-236.5	-250.3
Circuit Feature	LC-DCO	Ring-DCO	Ring-DCO	LC-DCO
Synthesized?	No		Yes	

$$\mathrm{FoM} = 10\log\left[(\sigma_T/1\mathrm{s})^2 \cdot (P_{DC}/1\mathrm{mW})\right]$$

[4] A. Elkholy, *et al.*,ISSCC2015 [6] S. Choi, *et al.*, ISSCC2016 [9] W. Deng, *et al.*,ISSCC2014