1S-7: Non-Binary Cyclic ADC with Correlated Level Shifting Technique

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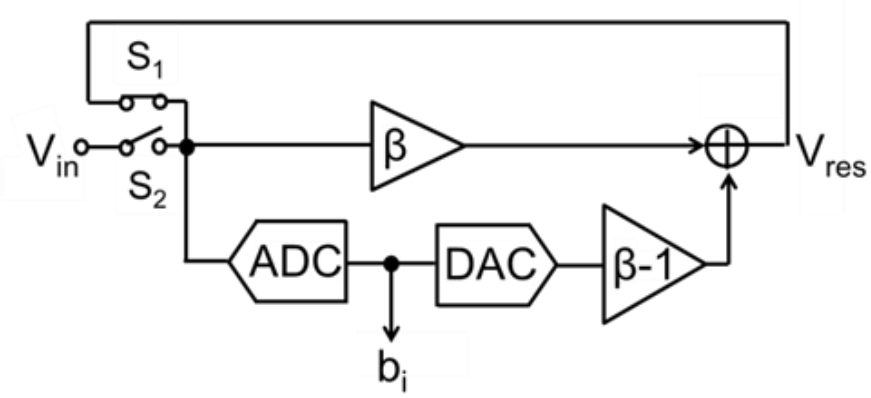
Low cost and PVT robust ADCs are required.



Previous work:

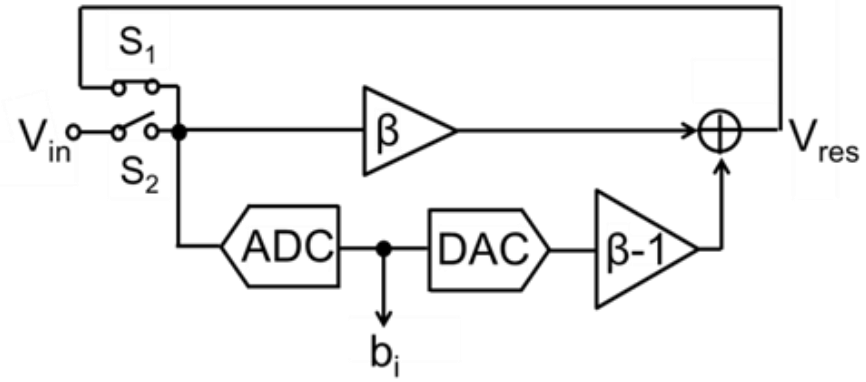
Proposed a non-binary cyclic ADC architecture which is robust to PVT variations.

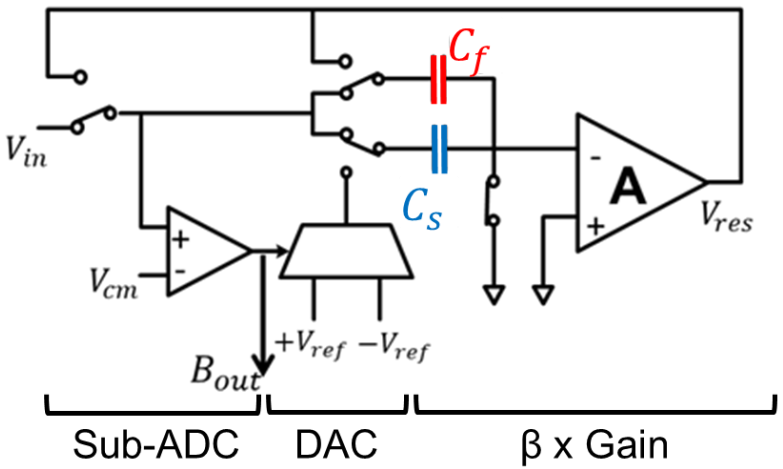
Design challenge of this work:

Propose Correlated Level Shifting(CLS) technique for cyclic ADC

- Extend the output swing of ADC in low supply voltage.
- Achieve higher SNR with small sampling capacitors.

Robustness of Proposed Non-binary Cyclic ADC





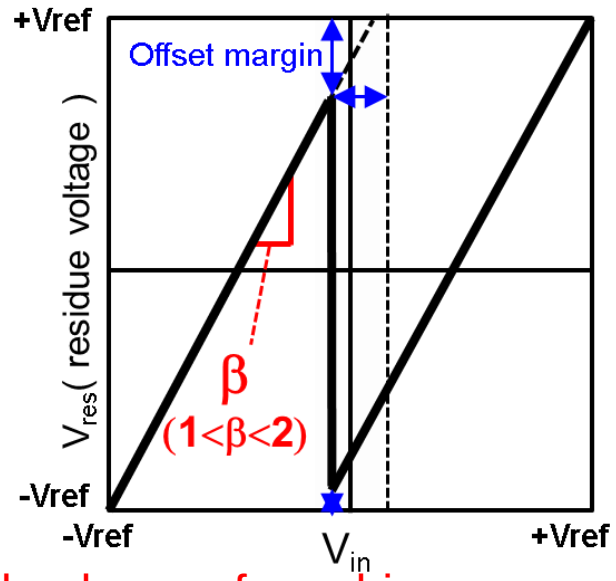
Simple circuit architecture:

- 1-bit ADC/DAC
- Amplifier with gain of β

Radix of ADC can be realized by capacitor ratio. $Radix = (C_s + C_f)/C_f$

$$V_{res} = \frac{C_s + C_f}{C_f} V_{in} \pm \frac{C_s}{C_f} V_{ref}$$

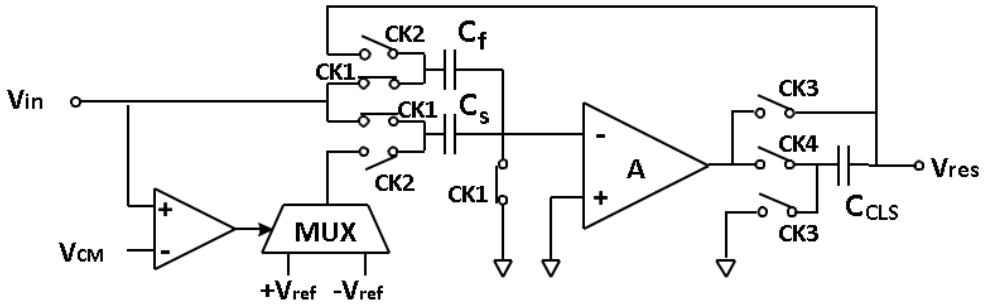
$$V_{res} = \beta V_{in} \pm (\beta - 1) V_{ref}$$



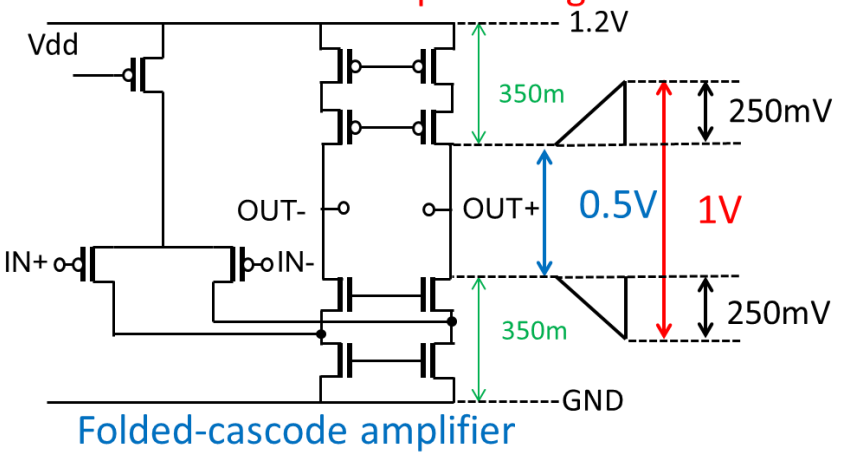
The redundancy of non-binary conversion tolerates the op-amp and comparator offset.

MDAC operation with CLS technique

$$SNR[dB] = 10log_{10}\left(\frac{CV_{FS}^2}{8nkT}\right)$$

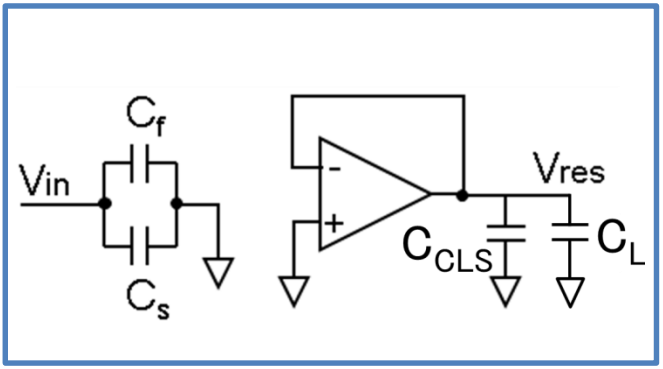


Extension of the output swing with CLS

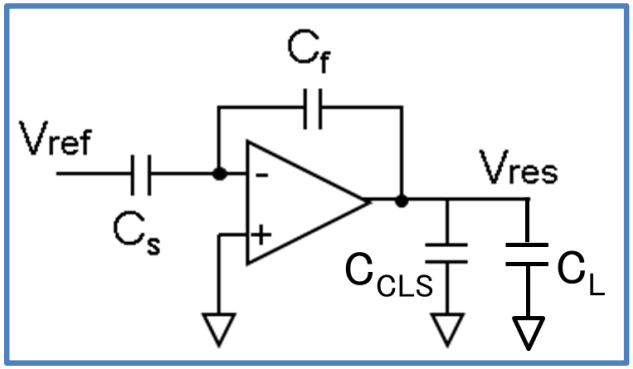


Folded-cascode amplifier

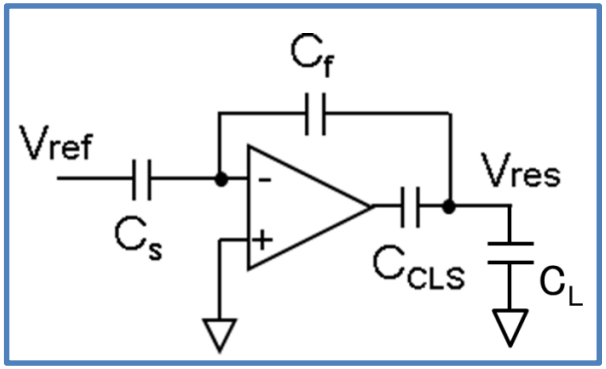
Sampling mode



Estimation mode



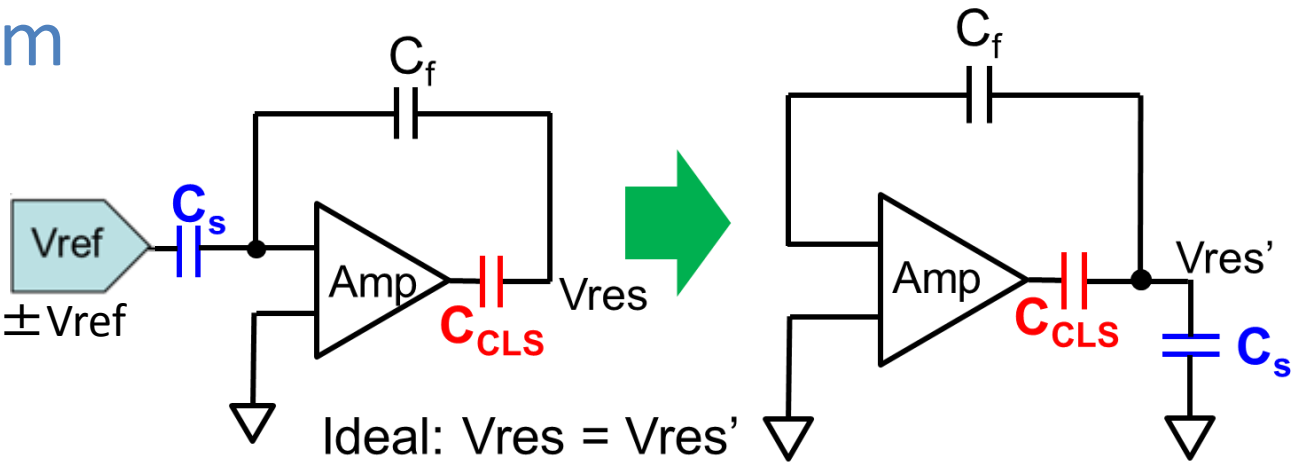
Level shifting mode



The output swing range of the MDAC can be expanded to achieve higher SNR with small C in low supply voltage.

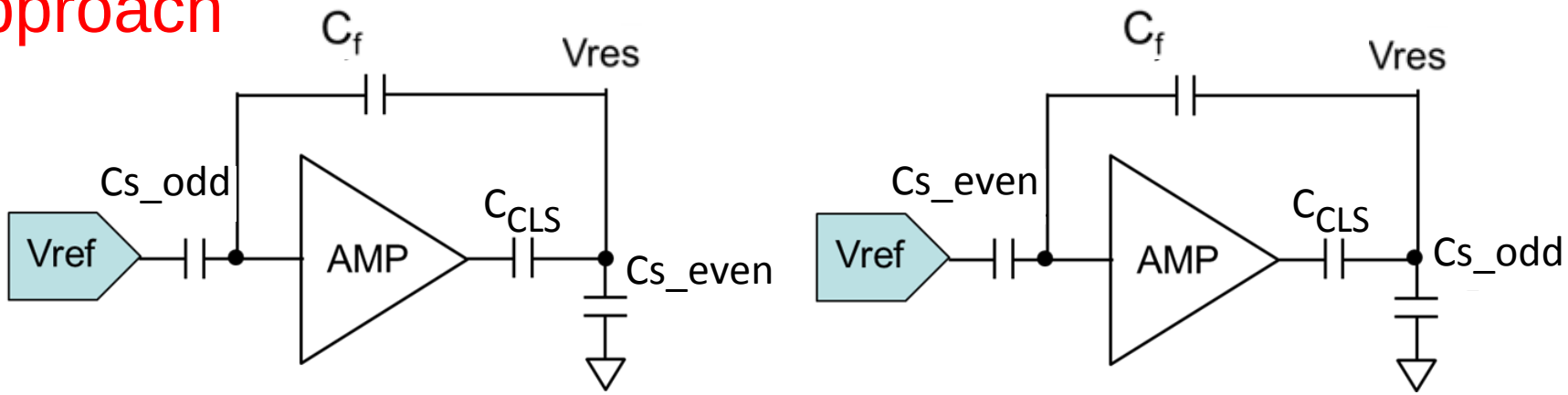
Proposed CLS technique for Cyclic ADC

Problem



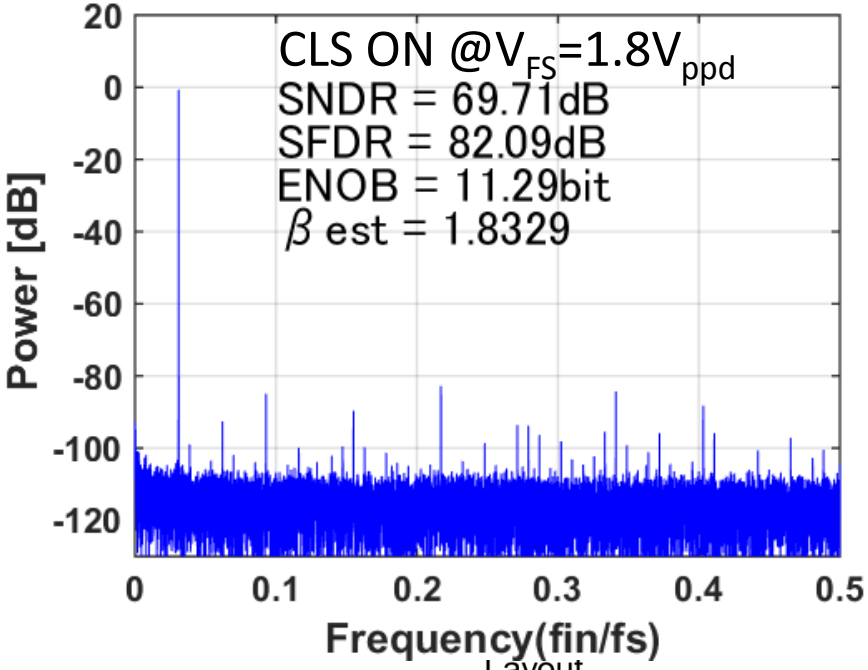
Residue voltage is changed due to charge redistribution.

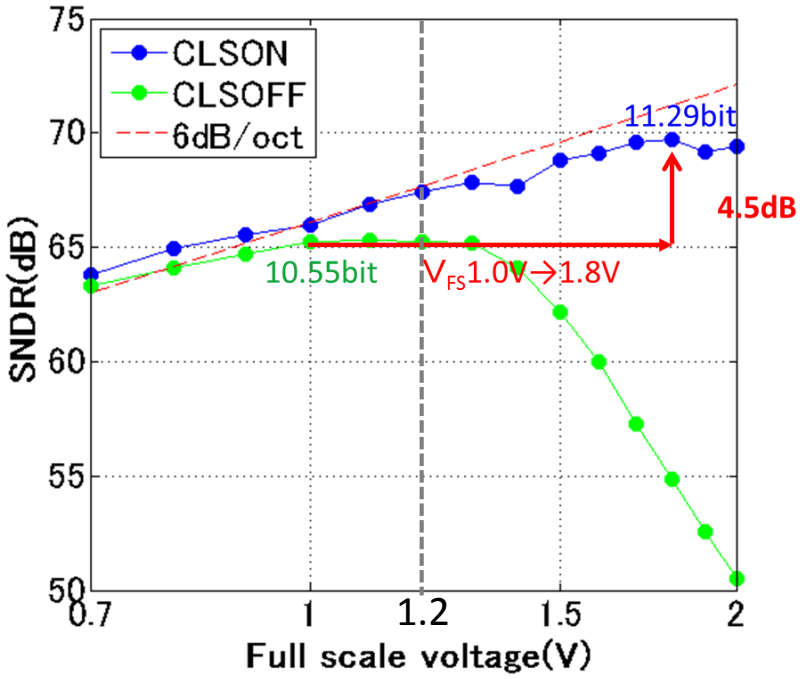
Approach



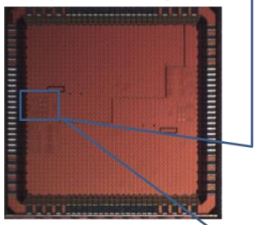
We have solved charge redistribution problem, And the output swing range of the MDAC is extended.

Implementation and Measurement Results

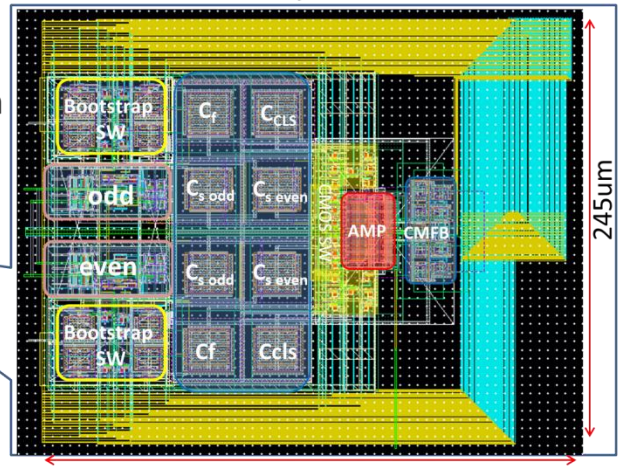




Chip micrograph



Layout



- The output swing of the ADC can be doubled by using CLS technique.
- Measurement results validate the effectiveness of proposed CLS technique.